Construction and development of read-out systems for radiation detection

Bjørn Magne Sundal

Thesis submitted in partial fulfillment
of the requirements for the degree Doctor Scientiarum
at the Department of Physics, University of Oslo

May 1999

Abstract

This thesis decribes the design and construction of front-end read-out electronics for particle detection. Front-end read-out boards for three major experiments have been made; finalized versions used by the RICH detector at CLEO-III (Cornell, US) and the Silicon Vertex Detector at BELLE (KEK, Japan) and prototype hybrids for the Semi-Conductor Tracker in the LHC experiment ATLAS (CERN). In addition has a low cost PC-based read-out system for evaluation of new sensors in technologies like Si, CdTe and CdZnTe been designed and constructed, so far used by more than 20 universities, research institutes and major companies throughout the world.

Acknowledgements

I would first of all thank my tutor S.Stapnes for always pushing me in the right direction when I have been stuck. I owe O.Dorholt a lot for being a good friend and companion in the design and construction of read-out hybrids for the ATLAS experiment, and also in the layout of the VA-DAQ. A.Marshal has been a great help in microscope studies of hybrids. At CERN I would like to thank P.Weilhammer for always being welcome in the lab and to the chip designers J.Kaplon and W.Dabrowski that I have been working closely with for the design of the read-out hybrids. Also D.Macina at the University of Geneva has done good measurements with the Oslo hybrids. At IDE I would especially like to thank E.Nygård, K.Yoshioka, G.Mæhlum, L.Evensen, P.E.Gaarder and J.Straver for interesting discussions contributing to my understanding in the field of particle detection and design of read-out electronics, and also valuable suggestions in the development of the VA-DAQ system.

Contents

List of Figures

List of Tables

Chapter 1

Introduction to particle detection

1.1 History

The first particle detector system was used by A.H.Bequerel as he discovered radioactivity in 1896. He used a photographic plate, and found it was blackened by an uranium salt. By the end of year 1900 three types of radiation were classified, called alpha, beta and gamma radiation, which we today know to be a helium-4 nucleus, an electron or positron and a photon [1].

The earliest methods of particle detection used various types of ionization chambers and scintillating detectors together with photographic methods or photo-multipliers. All these methods however have inherent limitations when it comes to tracking, energy resolution and high particle rates. When the real exploration of solid-state detectors begun in the late 50's, a whole new era was started leading to the semi-conductor detectors of today. Of major importance is the use of electronic readout that together with the semi-conductor detectors give us tracking down to a few μm precision, energy resolution down to few hundred eV FWHM and detectors operating at beam collision frequencies of 40 MHz, as the Large Hadron Collider will do.

1.2 The physics behind particle detection

The physics involved in the particle detection is usually divided into three categories:

- Interaction of charged particles with matter.
- Interaction of photons with matter.
- Other interactions, for instance involving non-charged particles like neutrons.

1.2.1 Passage of heavy charged particles through matter

When a charged particle traverse a material, either gas or solid, it will collide both elastic and inelastic with the atoms or molecules. The dominant elastic scattering is from the nu-

clei and the inelastic from the atomic electrons. Other reactions also occur, but with a very low rate, and can be ignored in the calculations. These reactions involve bremsstrahlung, which is important for light particles, and nuclear reactions.

Inelastic collisions, either soft where the atomic electrons are excited, or hard, where the atoms are ionized, will cause almost the full energy loss. Even though elastic scattering occur often, very little energy is transferred as long as the atoms are heavier than the incoming particle. The effect of the elastic (Coulomb) collisions is seen in the path deviations due to multiple small angle scattering.

The formula for describing the energy loss correctly, including quantum effects, was first developed by Bethe and Bloch. The same formula for the classical case, however was derived by Bohr. The steps in developing the formula for the classical case will be given below [2], because it intuitively explains how the important kinematic and other inherent particle properties, like particle charge and material parameters, enters the formula.

Some starting assumptions are needed:

- The heavy particle has the following properties; speed v, mass M and charge ze.
- The particle is heavy, and assumed to continue its path approximately undeviated when reacting with an electron.
- The atomic electrons are assumed free (small binding energy compared to the energy of the heavy particles), and at rest initially. Throughout the interaction it will move just a short distance.

The momentum impulse transferred to the atomic electron is given by

$$p = mv = \int ma\,dt = \int F\,dt = e\int E_t\,dt = \int E_t \frac{dt}{dx}\,dx = \int \frac{E_t}{v}\,dx, \tag{1.1}$$

where E_t is the transverse component of the electric field of the heavy particle. Only the transverse component contribute because any momentum impulse kick along the path must be cancelled by symmetry (equal contribution from the heavy particle when it is closing in and leaving). The last integral can be calculated using Gauss' law on an infinite long cylinder following the heavy particle track, and with a radius r at the electrons minimum distance from the track. Gauss law states that the surface integral over the electric field inside a closed surface is equal to 4π the charge enclosed (in Heaviside-Lorentz units where $4\pi\epsilon_0 = 1$). In this case this implies

$$2\pi r \int E_t\,dx = 4\pi ze. \tag{1.2}$$

This result is easily inserted in 1.1 resulting in

$$p = \frac{2ze^2}{rv}. \tag{1.3}$$

And the energy gained by the electron is given as

$$\Delta E = \frac{p^2}{2m_e} = \frac{2z^2e^4}{m_e v^2 r^2} \tag{1.4}$$

When traveling a length dx, the heavy particle will sweep a cylindrical volume $V = \pi r^2 dx$. We are for now interested in the volume enclosed by the cylindrical shell at radius r and of thickness dr, $dV = 2\pi r dr dx$. If the density of electrons is N_e, the total amount of particles passed are $N_e dV$. Since the heavy particle will lose ΔE to each of these electrons, its total energy change (loss) is

$$dE(r) = -\Delta E(r) N_e dV = \frac{4\pi z^2 e^4}{mv^2} Ne \frac{dr}{r} dx. \tag{1.5}$$

One could naïvely think that this must be integrated up for all values of r between zero and infinity, but this is wrong. At zero the energy transfer is infinite, which is impossible, and at infinity the momentum impulse transfer could not be over a short period of time, as it is assumed. Instead we integrate from r_{min} to r_{max}, and we motivate our choice of extreme r-values with physics arguments.

The r_{min} must be found from the maximum possible energy transfer. This is given by the head-on collision energy transfer $\frac{1}{2}m_e(2v)^2$, or relativistically $W_{max} = 2\gamma^2 m_e v^2$. The last one we can equal to equation 1.4 giving $r_{min} = \frac{ze^2}{\gamma m v^2}$.

We assume the electrons to be free, which is not exactly true. The energy transfer must take place within a time which is shorter than the orbital period, otherwise no energy is transferred. Since the typical interaction time is $t = r/v$ or relativistically $t = r/(\gamma v)$, and the orbital period is τ, or if given by orbital frequencies $\tau = 1/\bar{\nu}$, we require $r/(\gamma v) < 1/\bar{\nu}$, which gives us $r_{max} = \gamma v/\bar{\nu}$. As $\bar{\nu}$ we use the average over all bound states.

We should now note that the expression for $dE(r)$ was derived classically, whereas the limits for the integration for r have been introduced relativistically. If 1.5 is integrated up with respect to r using the r-values found, the result is

$$-\frac{dE}{dx} = \frac{4\pi z^2 e^4}{m_e v^2} N_e \ln \frac{\gamma^2 m_e v^3}{z e^2 \bar{\nu}}. \tag{1.6}$$

We can introduce $\beta = v/c$, and $N_e = N_a \rho Z/A$. In the last equation N_a is Avogadro's number, and ρ, Z and A the density, charge number and atomic weight of the medium. We can in addition move a constant 2 into the logarithm, thereby squaring the argument of the ln-function, and reintroduce W_{max}. These manipulations give.

$$-\frac{dE}{dx} = 2\pi \left(\frac{e^2}{m_e c^2}\right)^2 m_e c^2 N_a \rho \frac{Z}{A} \frac{z^2}{\beta^2} \ln \left(\frac{2\gamma^2 \beta^2 m_e c^2 W_{max}}{\bar{\nu}^2} \cdot \frac{\beta^2 c^2}{4e^4 z^2} \right) \tag{1.7}$$

Here the squared parenthesis equals the classical electron radius, $r_e = e^2/(m_e c^2)$. If the fine structure constant $\alpha = e^2/(2hc)$, is introduced inside the logarithm, a final version of Bohr's formula can be written as

$$-\frac{dE}{dx} = 2\pi {r_e}^2 m_e c^2 N_a \rho \frac{Z}{A} \frac{z^2}{\beta^2} \left(\ln \left(\frac{2\gamma^2 \beta^2 m_e c^2 W_{max}}{h^2 \bar{\nu}^2} \right) + \ln \left(\frac{\beta^2}{16\alpha^2 z^2} \right) \right). \tag{1.8}$$

The correct quantum mechanical result is the Bethe-Bloch equation, written as

$$-\frac{dE}{dx} = 2\pi {r_e}^2 m_e c^2 N_a \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left(\ln\left(\frac{2\gamma^2\beta^2 m_e c^2 W_{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right). \qquad (1.9)$$

The most important features are the same in both formulas. The energy loss scale by z^2 of the incoming particle and the electron density of the traversed medium. The average orbital frequency, $\bar{\nu}$, in the Bohr formula given as an energy $h\bar{\nu}$ is replaced by the mean excitation potential, I, being essentially the same quantity. It is the main parameter in the Bethe-Bloch equation, but very difficult to calculate. Empirical formulas are most often used.

For low energies, that is $v < 0.96c$, the logarithmic part of the formula contributes very little and $-dE/dx$ goes more or less like $1/\beta^2$. Note that the Bethe-Bloch equation is only used down to about 0.1β, where the assumptions are no longer valid.

If the energy loss (stopping power) is normalized with respect to the density of the stopping medium, the mass stopping power $-\frac{dE}{\rho dx}$ is found. At approximately $\beta = 0.96$ a minimum is reached for the mass stopping power, and this minimum is at about the same value for all traversing particles of the same charge. Above 0.96 the $1/\beta^2$ saturates and becomes more or less constant since it cannot grow above 1. The logarithmic part starts to dominate and a slow growth is found. This is easily seen in figure 1.1. This figure also illustrates the weak dependence of the energy loss on the traversing particle, showing pions and protons to have their minimum at the same relative momentum ($p/(m_0c) = \beta\gamma$) and with approximately the same energy loss. A particle with a momentum placing it in the minimum area of the Bethe-Bloch is usually called a minimum ionizing particle, or a MIP.

Another interesting feature of the figure is the fact that as a first approximation the mass stopping power is equal to $2\,\mathrm{MeV\,cm^2/g}$ independently of the stopping medium and the type of traversing particle, as long as the particle has $\beta > 0.96$.

The added terms δ and C in Bethe-Bloch, are corrections called the density-correction and the shell-correction, which apply at high and low energies, respectively. The density correction is due to the fact that the traversing particle polarizes the atoms, thus shielding remote electrons from the full electric field, and the particle loses less energy. The logarithmic growth is damped by this effect. The shell correction includes low velocity effects, since we no longer can assume the electron stationary with respect to the traversing particle. As long as we stay above $0.1c$ this correction is very small.

Another interesting parameter to measure is the distance the particle will travel before it comes to rest. For heavy charged particles, which more or less travel in a straight line, we can as a first approximation integrate the dE/dx formula, $R(E_k) = \int_0^{E_k} (\frac{dE}{dx})^{-1}\, dE$. For very low energies the Bethe-Bloch is not a good description, and it would be better to integrate from a $E_{k,min}$, where Bethe-Bloch is valid and add a term describing the length traveled for a particle with kinetic energy $E_{k,min}$. For the part of the Bethe-Bloch where β^{-2} dominates we see that R will go as E_k^2, but a fit to actual data gives $E_k^{1.75}$ as a better estimate.

Since the energy loss is not really continuous there exists a spread in range around the mean range, with a typical Gaussian distribution. This spread is called range straggling.

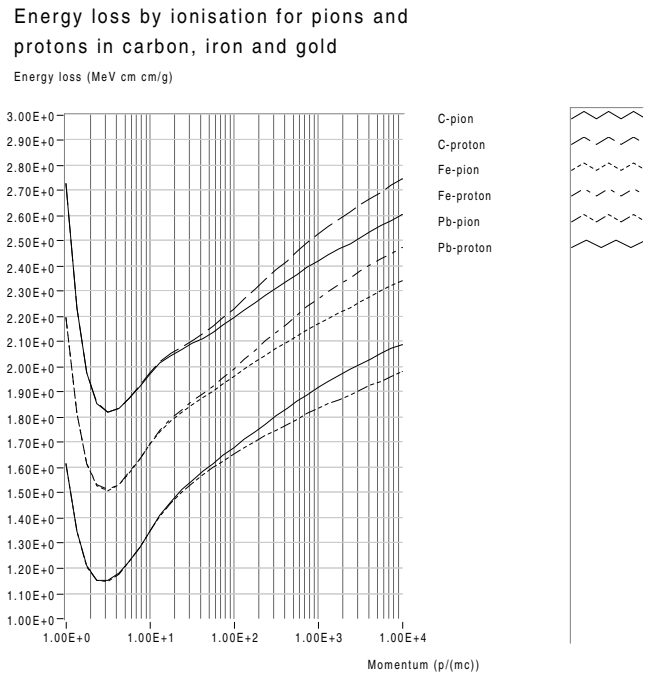


Figure 1.1: The Bethe-Bloch equation for pion and proton projectiles on lead (Pb), iron (Fe) and carbon (C) targets.

1.2.2 Energy loss of charged light particles

The electron and the positron will also lose energy due to collisions, but the assumptions in the derivation of the Bethe-Bloch formula are not correct. The most important factor is their small mass, which will make other effects more important, the dominating effect being bremsstrahlung.

The collision loss of electrons and positrons is described by a modified Bethe-Bloch formula. The particles will now change directions in the collisions due to their low mass. The maximum transferred energy in a collision, W_{max}, is much larger, now being half the kinetic energy of the incoming particle. For electrons there are also effects due to the fact that quantum mechanically the incoming and outgoing electrons are interchangeable. Typical collision loss curves for electrons are shown in the left plot of figure 1.2.

Bremsstrahlung (radiation loss) is the emission of photons by an accelerated charge in an electric field. Since bremsstrahlung emission is proportional to the square of the inverse particle mass, it is only important for electrons and positrons as long as we are not getting close to the TeV region. The acceleration is given by the deflection of the electron or positron by the electric field of the nucleus or the atomic electrons in the traversed material. The effect will therefore depend not only on the electron/positron incident energy, but also on the Z of the traversed material. In fact it is shown that the cross section scales as the square of Z. The two plots of figure 1.2 show separate and summed the collision loss and

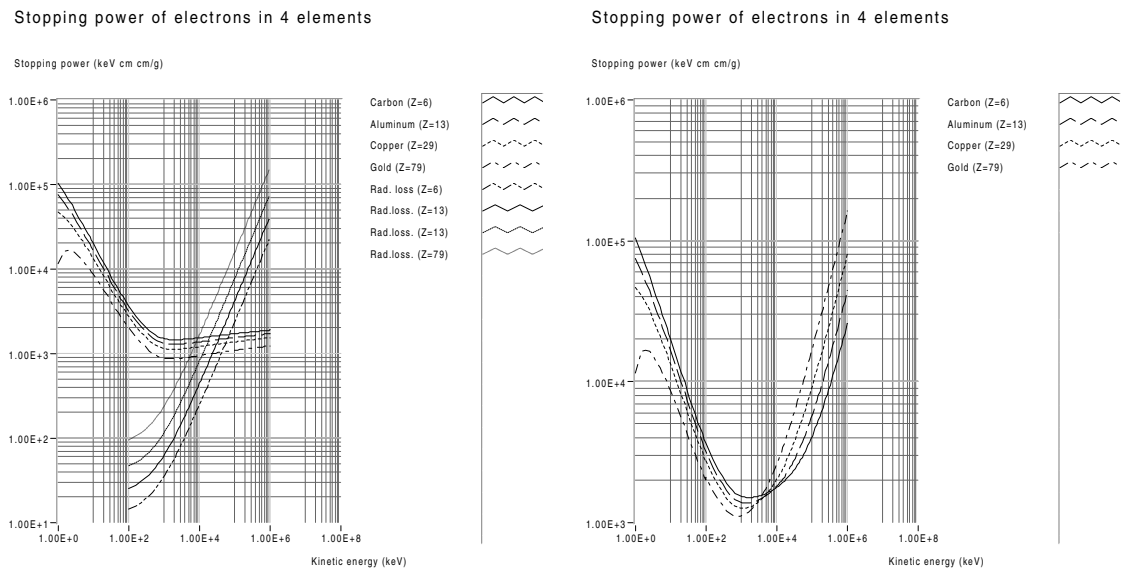


Figure 1.2: Collision loss, radiation loss and total loss for electrons in four elements.

radiation loss for electrons in several elements.

We see that the radiation loss is more or less increasing linearly with energy, at high energies. This introduces the quantity called the radiation length, X_0, defined as the distance traversed before the electron energy has dropped to 1/e due to the radiation loss. This can be written as $\mathrm{E} = \mathrm{E}_0 \exp(-x/X_0)$. Often the radiation length is given in g/cm^2, which means that the distance has been multiplied by the density of the material. We typically define a critical energy, empirically given by $E_c \approx 800\,\mathrm{MeV}/(Z + 1.2)$, to be the energy where the radiation loss starts to dominate the collision loss. The average radiation length (g/cm^2) for a compound, is found from the formula $1/X_0(\mathrm{g/cm^2}) = \sum_i \omega_i / X_{0,i}$, where ω_i is the fraction by weight of the i'th part of the compound. The density of a compound is calculated in the same way, just substitute X_0 with density in the above formula. The radiation length is empirically given by the formula [5]

$$X_0(\mathrm{g/cm^2}) = \frac{716.4\mathrm{mol/cm^2}\, M}{Z(Z+1)\ln(287/\sqrt{Z})},$$

where M is the atomic mass (g/mol) and Z the atomic number. The formula is correct to within 2.5% for all elements except helium.

The range of electrons is very difficult to calculate, and is usually found tabulated. Figure 1.3 shows the mass range and the range of electrons in several elements.

1.2.3 Multiple Coulomb scattering

One can show that the path deviation by multiple Coulomb (elastic) scattering scales with the radiation length, making the radiation length X_0 an important quantity also for

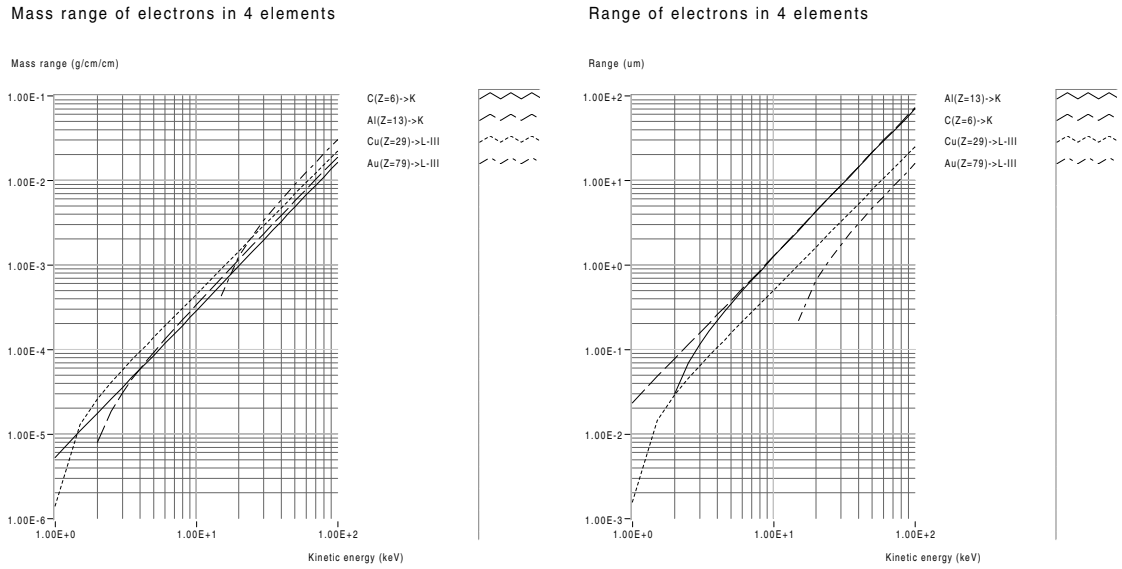


Figure 1.3: Mass range and range of electrons in Carbon, Aluminum, Copper and Gold.

Coulomb scattering. Of course Coulomb scattering and bremsstrahlung have nothing to do with each other, but the expression for X_0 enters in the formula as a simplification. Since Coulomb scattering starts to play a role below 50 GeV, it is obvious that material needs to be minimized in the inner detectors to have good tracking, and also that the radiation length is a suitable quantity to characterize the tracking performance of the inner detectors.

For small angle scattering and not too thin material, the angle distribution is more or less Gaussian in shape, the width being

$$\theta_0 = 13.6\mathrm{MeV}Z^2\sqrt{t}(1 + 0.038\ln t)/(\beta E). \tag{1.10}$$

Here the thickness of the material traversed, T_{material} is measured as a fraction of a radiation length, $t = T_{\mathrm{material}}/X_0$. In fact this formula is better for heavier charged particles than for electrons and positrons since these also experience more violent scattering due to bremsstrahlung, giving a larger tail to the distribution.

For a typical tracking detector system the thickness is of the order of percent. If the parenthesis are evaluated once with $t = 0.01$ and included in the leading constant, a crude formula will yield

$$\theta_0^2 \approx Z^2 \frac{E_{norm}^2}{\beta^4 E^2} t. \tag{1.11}$$

The individual material contributions add up, and since θ_0^2 is a Gaussian width it needs to be summed in quadrature, giving a total scattering due to individual material contributions of: $\theta_{0,\mathrm{total}}^2 \approx Z^2 E_{norm}^2 t_{\mathrm{total}}/(\beta^4 E^2)$. This estimate should not be trusted to more than 30%.

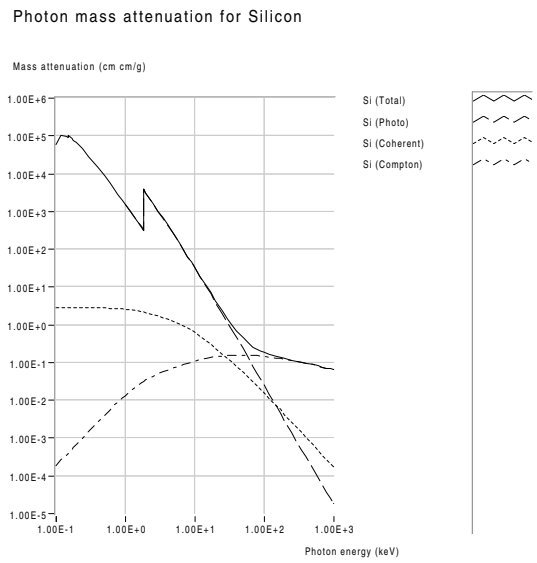


Figure 1.4: Photon mass attenuation for silicon, individual contributions due to photo-electric effect, Compton scattering and coherent scattering shown.

1.2.4 Attenuation of photon beams in matter

The mechanisms in which photons react are mainly through photo-electric effect, Compton scattering and pair production. In analogy with the above sub-sections this sub-section should have been called energy loss of photons. The fact that it is not demonstrates the most striking feature of the above mentioned reactions. The photon will either react and disappear (where disappear means a Compton scattering that alters its direction and energy throwing the photon out of the beam), or continue straight through the matter. This means the photon beam is only attenuated and not shifted and straggled in energy. Figure 1.4 shows the photon mass attenuation for silicon, where the separate contributions from photo-electric effect, Compton scattering and coherent scattering are shown. This figure ends at the energy for the onset of pair-production, which is about 1 MeV. Figure 1.5 shows total mass attenuations in the same energy range for carbon, silicon, germanium and lead. The three first ones are highly interesting as detector materials.

In the photo-electric effect the photon will be absorbed by an atomic electron, which is then ionized. The energy of the outgoing electron will be $E = h\nu - E_b$, where E_b is the binding energy of the electron and ν the photon frequency. The electron must be bound since a free electron reaction could not conserve momentum and energy.

The most important feature is that above the highest binding energies of the atom (K-shell) the photo-electric cross-section drops very rapidly with photon energy. A calculation will reveal that it is proportional to $Z^5/E_{\text{photon}}^{7/2}$. This formula also shows the very strong dependency of photo-electric effect on the atomic number, Z. Below each absorption edge there is a typical drop in the cross section, since a lot of electrons in the atom suddenly are not available for photo-electric absorption.

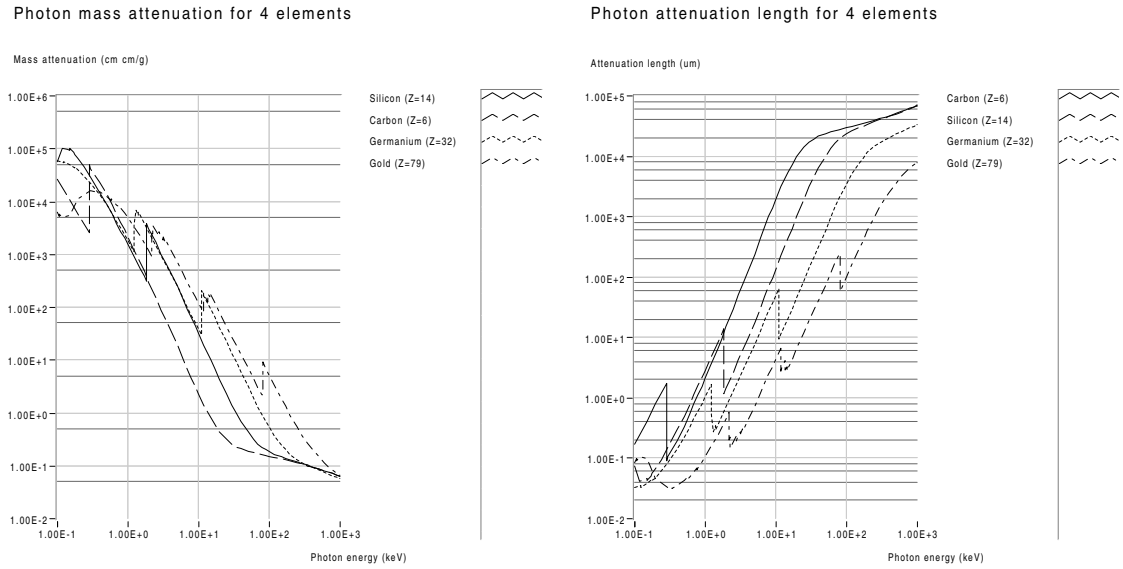


Figure 1.5: Photon mass attenuation and attenuation lengths for carbon, silicon, germanium and gold.

Compton scattering describes the scattering of photons off free electrons. As long as the photon has a high energy, it will be a good approximation to say that the atomic electrons are free. The Compton scattering is often called incoherent scattering, this to show that it is scattering off single electrons of the atom.

For low photon energies there exist a possibility of coherent scattering (Rayleigh scattering), where the photon is scattered off the atom as a whole. The term coherent stems from the fact that the electrons contribute to the scattering in a coherent way. This reaction will change the direction but not the energy of the photon. The coherent scattering cross-section drowns in the photo-electric cross-section at low energies and dominates it at higher energies and low Z, but both are small at high energy compared to the Compton cross-section.

The relation between the energy of the incoming, E_{in}, and the scattered photon, E_{out}, for Compton scattering is

$$E_{out} = \frac{E_{in}}{1 + (E_{in}/E_0)(1 - \cos\theta)}, \tag{1.12}$$

where E_0 is the rest energy of the electron. Of greater interest is the total Compton cross section, which is given by the integration of the Klein-Nishina formula,

$$\frac{d\sigma}{d\Omega} = \frac{r_e^2}{2} \frac{1}{(1 + \gamma(1 - \cos\theta))^2} \left(1 + \cos^2\theta + \frac{\gamma^2(1 - \cos\theta)^2}{1 + \gamma(1 - \cos\theta)} \right), \tag{1.13}$$

where $\gamma = h\nu/(m_e c^2)$. Also of great importance is the energy distribution of the Compton

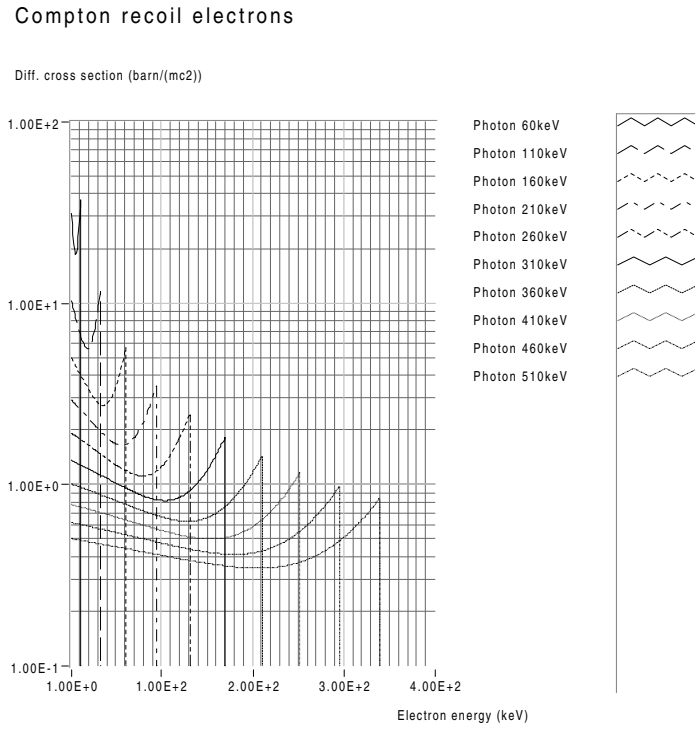


Figure 1.6: Differential cross-section ($d\sigma/dE_k$) for Compton recoil electrons. Measured in barns per mc^2. E_k is the electron energy and m the electron rest mass.

recoil electrons, found by the Klein-Nishina formula to be

$$\frac{d\sigma}{dE_k} = \frac{\pi r_e^2}{m_e c^2 \gamma^2}\left(2 + \frac{s^2}{\gamma^2(1-s)^2} + \frac{s}{1-2}(s - 2/\gamma)\right), \tag{1.14}$$

where s is $E_k/(h\nu)$, and the maximum recoil energy will be, $E_{k,max} = 2h\nu\gamma/(1+2\gamma)$, and is called the Compton edge. Figure 1.6 shows some typical plots. Since the cross-section here is for one electron only, the Compton cross-section for a material will go as the number of electrons, Z.

When the photon energy crosses an energy of 1.02 MeV, pair production of an e^+e^- can occur if a nucleus or an atomic electron are present to ensure momentum and energy conservation. This is the crossed process of bremsstrahlung. At energies past the onset for pair-production, the cross section grows rather fast at first and then slower, and is the dominant reaction process for photons already at 10 MeV, helped by the fact that the Compton and photo-electric cross sections are dropping with energy. The dependence of the pair-production on atomic charge number is Z^2.

The total photon absorption cross section, σ, is used to calculate the mass attenuations as shown in figure 1.4 and figure 1.5. It is given as the sum of the contributions from the photo-electric effect, the Compton scattering and the pair-production, remembering that the expression for the Compton cross section above needs to be multiplied by Z since it

only involved one of the atomic electrons. If σ is multiplied with the atomic density of the material $N = N_a\rho/A$, the probability per unit length for an interaction is found, called the attenuation coefficient, $u = N\sigma$. The mass attenuation coefficient is given as u/ρ. The intensity of the photon beam will go as $\exp(-ux)$. The attenuation length is $1/u$ (the length traversed to reduce the intensity to a fraction of 1/e), but also here the quantity mass attenuation length $1/(u/\rho)$ is more often used since it results in similar numbers over a wide range of stopping materials. The attenuation length is often just referred to as the mean free path of a photon, since the mean traversed length (mean free path) over a probability function $p(x) \propto \exp(-ux)$ will be $\int_0^\infty xp(x)dx = 1/u$.

1.2.5 Summary on interaction processes

It is difficult to give a brief summary for the use of the fore mentioned physics without looking into the application. I will try to divide it into applications for tracking in high energy physics experiments and applications for medicine, being the two most interesting branches.

In the case of tracking of highly energetic particles, which is the case for the ATLAS experiment and other high energy physics experiments, two important points can be noticed from the physics of the previous section.

- All equally charged highly relativistic particles will ionize a material equally. The value of the ionization is most often taken as the MIP value, the minimum of the Bethe-Bloch function, and is in the order of 2 MeV cm^2/g, ignoring the slow logarithmic growth with energy.

- The radiation length is a very useful quantity in the characterization of the tracking quality, since it will give the Coulomb scattering, and also the probability of bremsstrahlung and pair-production.

For applications in medicine, where we are working with 'low' energetic photons and electrons, energy measurements are often just as interesting as position resolution. In detecting a full energy deposition of the photon by means of the photo-electric effect, one should notice that the cross section is larger for lower energies and that the cross section scales by Z^5 above the K absorption edge, thus favoring heavy materials for energy measurements, since the photo-electric effect is the dominant mechanism up to higher energies. Today the gamma camera is most widely used, consisting of a scintillating crystal and a photo-multiplier. A Compton camera, a newly proposed replacement to the gamma camera in applications like SPECT (Single Photon Emission Computed Tomography), will require lighter materials, since the Compton effect here starts to dominate already around 100 keV, which is very favorable since typical radio-nuclides like technetium used in medical imaging emits in this energy range. The Compton camera can, by measuring Compton recoil electrons in the primary detector and the scattered photons stopped in the secondary detector, give both position (confined to a cone) and energy measurements. For machines like PET (Positron Emission Tomography), which will have to detect two opposite going

photons created in an e^+e^- annihilation, even timing resolution is very important, to assure that only two photons from the same annihilation are detected.

1.3 Detector types

Most detector systems are based on measurements of position and ionization of charged particles. Photons are detected through their interaction with matter, transferring their energy to electrons. Three basic detectors are used; scintillators, ionization detectors and solid state detectors. Ionization detectors are usually a reserved term for gas ionization detectors, but it can also be liquid ionization detectors mostly used in calorimeters. In all three cases we are interested in ending up with an electric signal (electrons) flowing in our measuring circuitry, which is related to the properties (inherent and kinematic) of the incoming particle.

1.3.1 Scintillating detectors and photo-multipliers

Scintillation detectors are an important group of detectors for detecting both high energetic photons and charged particles. The process involves an excitation of a transparent material, conversion of the excitation by the ionizing particle into visible light, and the transport of this light to a photo-cathode of a photo-multiplier. By the photo-electric effect the photons can produce electrons on a cathode of a photo-multiplier (photo-cathode). These are accelerated down the photo-tube hitting dynodes thereby releasing more electrons accelerated down to the next dynode. The process continues until the first few electrons released at the photo-cathode are multiplied into a measurable current at the anode. Theoretically one can replace the photo-multiplier by a solid state sensor, like a silicon pad sensor, even though this has not yet been found cost-effective in medical applications like SPECT. When the solid state sensor gain higher popularity, prices should drop. The advantage of the solid state sensor is in size, and the removal of the very high voltage supply that a photo-multiplier need, and not so much in performance.

The scintillator materials are divided into two large group; organic and inorganic scintillators [4]. Inorganic scintillators like NaI and CsI are favored in energy measurements, since the light yield is bigger for the same ionization energy, thereby reducing the statistical fluctuation (shot noise) of the number of scintillating photons. The decay times of inorganic crystals can be very long and usually above some hundred nanoseconds, compared to a few nanoseconds for organic scintillators. This is the reason for use of organic scintillators for timing and in trigger logic.

In the inorganic crystal the ionizing particle produces electron/hole pairs. In the case of an incoming photon, the photon will give an electron by means of the photo-electric effect, Compton scattering or pair-production, where the electron gives ionization and excitation of electron/hole pairs just as if it was any other incoming ionizing particle. The bandgap in inorganic crystals is usually $6 - 8\,\mathrm{eV}$, and the gap contains activator centers or states. The electrons and holes move around in the lattice and can excite the activator states, and

the decay of these activator states give light in the visible range. The long decay time of the scintillating light is due to the rather long lifetimes of the activator states.

In the case of an organic scintillator, the mechanism is completely different. These materials are not crystals, and we have no lattice effects. The ionizing particle can excite molecular energy levels, these decay after a few nanoseconds emitting ultraviolet light. This material called the primary fluorescent material, is only one component of the organic scintillator. The second fluorescent material (also referred to as the wavelength shifter) is chosen such that it easily absorbs these UV photons (typical absorption lengths are a few millimeters for almost all organic transparent materials) and emits visible light matched to the quantum efficiency of the photo-cathode. These two materials are usually mixed in an organic solution capable of polymerisation, such that the final scintillator can be put into the desired shape for the application.

The photo-multiplier tube, which is an evacuated glass tube, receives the incoming visible photons, and by the photo-electric effect on the (photo-)cathode produces electrons. The photo-cathode is a semi-conducting alloy, usually containing two alkali elements and one element from group V. These cathodes are referred to as bi-alkali cathodes. The maximum quantum efficiency (photoelectrons produced per incoming photon) is 27% at 380 nm. The photoelectrons have a most probable energy of 1.2 eV, but for light between $400 - 430$ nm the distribution goes from $0 - 1.8$ eV.

The timing resolution and the time jitter are mostly due to geometrical effects of electrons taking different paths through the dynode chain. The rise time of anode pulses can be in the 10 ns order with time jitter up to half this value. To reduce these times a so called micro-channel multiplier has been introduced, having total transit time of a few nanoseconds and jitter down to 0.1 ns.

1.3.2 Ionization detectors

The earliest method for detecting charged particles was the ionization chambers, which involves putting a high electric field across a gas volume. A charged particle moving in the gas will break up gas molecules into electrons and ions by means of inelastic scattering. This method evolved from current ionization chambers to pulse ionization chambers. By increasing the electric field new physical phenomena are introduced giving us the proportional chamber and for the highest fields, the Geiger-Muller tube. The detection is in all cases by measuring the electronic signal in the anode/cathode loop. In a proportional chamber, typically built with a cylinder cathode and wire anode along the cylinder axis, the strong field around the center wire will accelerate the electrons. The energetic electrons will collide with the gas in the chamber producing new electron/ion pairs ending up with a detectable avalanche. The main part of the signal is by the drift of the positive ions back towards the cathode. The use of these devices are mainly for detecting and counting ionizing particles [1].

From 1968, when Charpak invented the MWPC, the multi-wire proportional chamber, ionizing detectors started to play an important role also in particle tracking. Earlier most tracking was optical, using photographs to record track information either directly in the

emulsion, or in spark, cloud or bubble chambers [2]. The principle in the MWPC is to apply closely spaced anode wires between two cathode planes. This will give a radial field around each wire, in the same way as found in a single wire proportional chamber.

The MWPC (one-dimensional tracking) later developed into two other important tracking devices, the drift chamber (two-dimensional) and the time projection chamber (3-dimensional). In the drift chamber position information is also found by measuring the drift time of the electrons until they reach the anode wire. The TPC is typically built as a cylinder, the end-caps being two-dimensional wire chambers, and employing drift times from the originating electrons to find the position along the cylinder axis. Since the drift volume of the TPC is in a strong magnetic field along the cylinder axis, the traversing charge will ionize a helical path, which will reveal the particle momentum, and as a side effect keeps the ionized path from diffusing while it is drifting towards the MWPC end-caps. With analogue readout the dE/dx will also be known, identifying the particle.

1.3.3 Solid-state detectors

Solid-state detectors are more or less an obsolete term, today replaced by semi-conductor detectors. The first real experiments started in the late 50's and commercial available detectors for high-resolution energy measurements were available already in the 60's, employing nitrogen cooled Germanium diodes for measuring energy spectra of radioactive sources.

The working principle is the same as for the ionization chambers, with the gas replaced by a solid. In a semi-conductor detector the charged particle will ionize the material throwing electrons into the conduction band from the valence band, leaving a positive charged fixed ion in the lattice. Or as this is described in semi-conductor terminology, creating an electron hole pair.

Many advantageous sides are found in comparison with gas ionization chambers. Due to the higher density the mass stopping power is greater, leading to more compact detectors. In addition will the charge collection times be much shorter giving better time resolution. Additional important properties are the possibility of much better energy resolution and spatial resolution.

The improved energy resolution can be attributed to the very low energy needed to form an e-h+ pair, ionizing energies being $w = 3.6\,\mathrm{eV}$ in silicon and $2.9\,\mathrm{eV}$ in germanium. This can be compared to $20 - 40\,\mathrm{eV}$ for ionizing gases, whereas $400 - 1000\,\mathrm{eV}$ is necessary to ensure the production of one photo-electron on the cathode of a scintillator/photo-multiplier system [4]. This has an enormous effect on the energy resolution of the detector, as shown below.

If a well-defined energy is lost, there is a statistical distribution of the number of ionized pairs being produced. One would first think this would be a Poisson distribution, with a standard deviation of $N^{1/2}$, where N is the average number of pairs produced. In fact it was first shown by Fano that the deviation is $(FN)^{1/2}$, where F is called the Fano-factor. This is due to the constraint energy conservation induce on the number of charge carriers produced in the individual ionization processes [3]. For ionizing detectors F is

typically around 0.2-0.3 for gases, whereas for solids like silicon it is in the area 0.12-0.16. For scintillators, however, the Fano factor is close to 1, indicating that it is Poisson distributed.

The energy resolution is thus given by $\Delta E/E = (FN)^{1/2}/N = (F/N)^{1/2} = (Fw/E)^{1/2}$. Since the ionizing energies for scintillators are about a factor 150 higher than for silicon and the Fano factor about 8 times higher the inherent energy resolution of the silicon detector is approximately 40 times better than that of a scintillator/photo-multiplier, at the same deposited energy.

The improved spatial resolution comes first from the geometrical properties of the semi-conductor processing. This process based on photo-lithography and etching allows the fabrication of diode strips on a silicon wafer with a position accuracy in the 1 um range. This technology is a commercial silicon IC production technology developed for consumer electronics.

Of course, solid-state detectors are not without limitations. In position sensitive applications the size of the crystal is limited by the available wafer size. It has steadily been growing from 4 inch wafers to 8 inch, and during the last year the first 12 inch factories are built. The HEP community cannot keep up the rate of consumer electronics, and the most common is 4 inch wafers, though 6 inch wafers are now also used. The most important effect of the size limitation of the wafer is the fact that it leads to tracking devices being divided into building blocks, called modules, in the 100 square centimeter range.

In addition is the cost of the material high, usually limiting the total size to how deep one is willing to dig for money. The biggest experiments being planned, like ATLAS and CMS for the CERN LHC project, are both building silicon tracking devices of about 50 square meters. The most important limitation can however be radiation damage of the sensor itself. Here we find three important effects, being the increase in leakage current, change of the doping concentration and the change of lifetime of charge carriers [6].

To fully understand the working principle of the semi-conductor detector, an introduction is given below. Some items are described in more details later, when it is vital in understanding the reason behind the choices made in specific implementations.

1.4 Semi-conductor materials

The elements Silicon and Germanium from group IV of the periodic system are the most well known semi-conductors. The term semi-conductor stems from the fact that the electrical conductivity is somewhere in between that of metals and that of insulators. It is also possible to produce compound semi-conductors by combining elements from group 3 and 5, the most well known being Gallium Arsenide.

A crystal has an energy-band structure. This consists of allowed energy bands separated by energy levels where the electron can not be. The allowed bands are for all practical purposes continuous, but are in reality formed by discrete atomic energy levels. The reason is that the energy level of a specific atom is split when equal atoms are brought together. This fine splitting of energy levels will contain one level for each atom in the crystal,

resulting in a number of discrete levels within a band in the order of the number of atoms in the crystal.

The uppermost band completely filled with electrons is called the valence band, and represents the loosest bound atomic electrons. The next band is called the conduction band. An electron receiving enough energy can be excited into the conduction band and is free to move within the lattice of the crystal.

In a metal the valence band and conduction band are overlapping, partially filling the latter. This gives metal a very low resistivity. For an insulator the energy gap is in the order of 3.5 to 6 eV with the implication that thermally excitation of an electron from the valence band to the conduction band is virtually impossible, leading to an extremely high resistivity. In a semi-conductor the band-gap is in the order of 1 eV, which means that at room temperature some electrons can be thermally excited to the conduction band, giving some electrical conduction.

In working with the conduction band, we think in case of a 'few' moving electrons, excited from the valence band. We could for the valence band also think in terms of an enormous amount of electrons, in an almost full band. Instead we choose to think in terms of the missing electrons in the valence band, and we visualize a 'few' holes with a positive charge moving around in the valence band. An energy excitation will produce an electron-hole pair, or in older terms the excited electron will leave an unfilled electron position in one of the atoms in the lattice. In an intrinsic semi-conductor, that is in a clean crystal, we understand that the amount of electrons and holes are equal, since they must be produced in pairs.

1.4.1 The statistical mechanics of electrons and holes

The distribution of electrons and holes in the valence and conduction band is given by statistical mechanics, and the electrons in a crystal follow the statistical law of Fermi-Dirac since electrons are fermions. The Fermi-Dirac probability function is given by

$$f_F(E) = \frac{1}{1 + \exp(\frac{E - E_F}{kT})}. \tag{1.15}$$

This gives the probability that a quantum state of energy E will be occupied at temperature T. The two other quantities are Boltzmann's constant, $k = 1.38 \cdot 10^{-23}$ J/K, and the Fermi-energy. The meaning of the latter will soon be apparent. This function is shown in the left plot of figure 1.7 for $T = 0$ and $T > 0$.

If we visualize for ourselves a system at absolute zero temperature, we know that all electrons must be in a quantum state with as low an energy as possible. If the function $g(E)$ describes the density of states as a function of energy for a particular system, we will have the situation in the right plot of figure 1.7 with $T = 0$. Along the y-axis is the amount of electrons found in each state for the particular energy found along the x-axis. Since all electrons are in the lowest possible energy state, the number of electrons follows the density of states function. At a certain energy along the x-axis will all electrons in

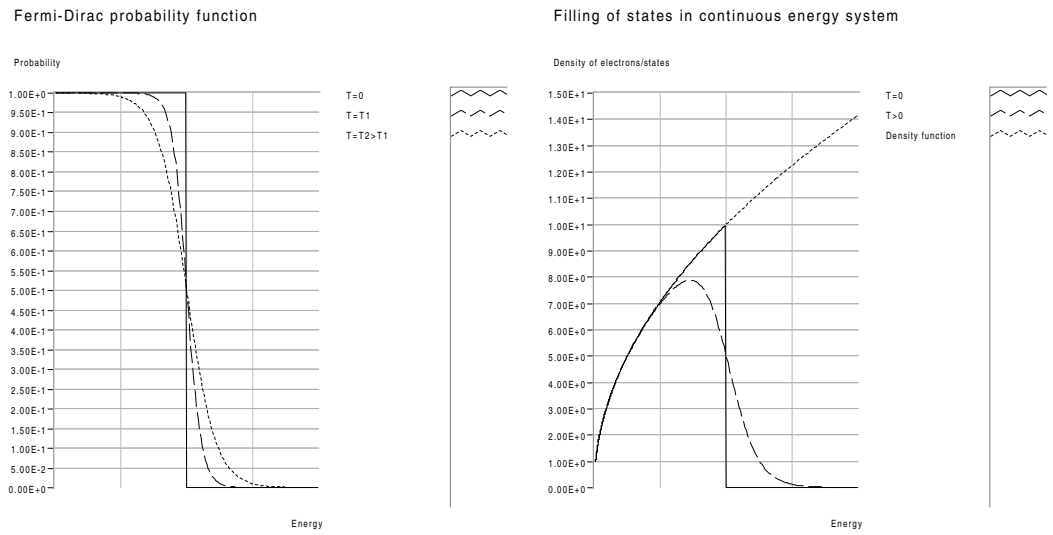


Figure 1.7: Fermi-Dirac probability functions for temperatures $T = 0$ and $T > 0$ are shown in the left plot. Density of electrons at $T = 0$ and $T > 0$ and density of states, both for a continuous energy system are given in the right plot.

the crystal be used to fill up the lower energy states, and no electrons are found at higher energies. This energy will be the Fermi-energy, E_F.

When the temperature is increased (right plot of figure 1.7 for $T > 0$), some electrons will be excited and found in states above the energy possible at zero temperature. Since $g(E)$ is the density of states at a given energy and $f_F(E)$ the probability of it being filled, the product $f_F(E)g(E)dE$ will give the number of electrons in the states at energy E. The area under the graph contains the total number of electrons, or:

$$N_0 = \int_0^\infty f_F(E)g(E)dE \tag{1.16}$$

1.4.2 Intrinsic semi-conductors

In a semi-conductor the situation is as shown in figure 1.8. If we first assume the density of states function, g, to be the same for electrons and holes, we can immediately deduce that the Fermi-energy is in the middle of the band-gap. This follows from the fact that the Fermi-Dirac probability function is symmetric around E_F and we know that the electron and hole concentrations n_0 and p_0 must be the same, since they are created in pairs. The density of states function goes as the square root of the energy difference to the band-edge, except for a constant given by $4\pi(2m)^{3/2}/h^3$, where m is the effective mass of either the electron or hole for the conduction band or the valence band. The effective masses observed for electrons and holes moving in the crystal are not the same as the free electron mass, and they are not even the same for electrons and holes. They are however not more different than that the Fermi-energy is almost exactly in the center of the band-gap.

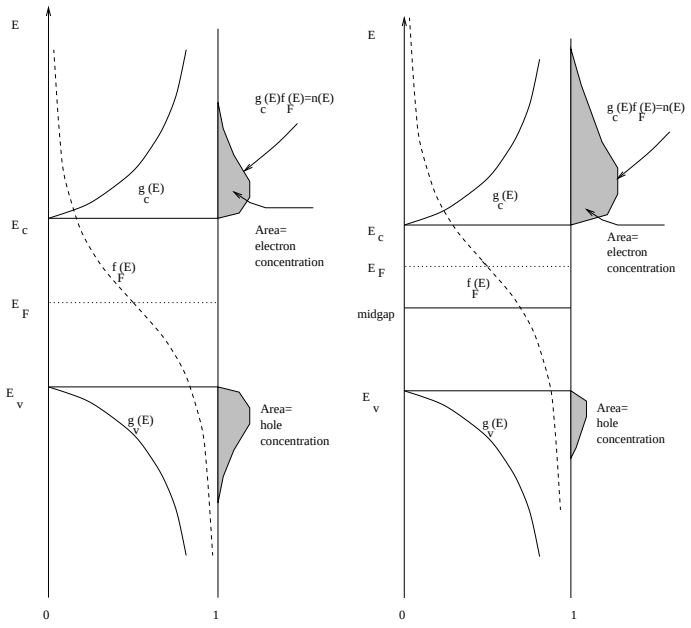


Figure 1.8: Density of states in an intrinsic (left half) and extrinsic (right half) semi-conductor.

As in equation 1.16 we can integrate up to find the electron and hole concentrations:

$$n_0 = N_c \exp\left(\frac{-(E_c - E_F)}{kT}\right) \quad \text{and} \quad p_0 = N_v \exp\left(\frac{-(E_F - E_v)}{kT}\right) \tag{1.17}$$

Here N_c and N_v are two constants, called the effective density of states in the conduction and valence bands, respectively, whereas E_v is the energy at the edge of the valence band and E_c the energy at the edge of the conduction band. In doing the integration the the Boltzmann approximation of the Fermi-Dirac equation is used, assuming the 1 in the denominator to be negligible.

The intrinsic semi-conductor has $n_i = n_0 = p_0$ and we name n_i the intrinsic carrier concentration, n_i. The product of the two equations 1.17 give the the interesting relation

$$n_i^2 = N_c N_v \exp\left(-\frac{E_g}{kT}\right), \tag{1.18}$$

where E_g is the band-gap energy $E_c - E_v$.

1.4.3 Extrinsic semi-conductors

If small amounts of impurities, or dopants, are introduced into the intrinsic crystal, we will have an extrinsic crystal. Usually materials from group 3 or 5 are introduced into silicon, phosphor and boron being by far the most used materials.

In the silicon crystal we replace one atom with a phosphorous atom. Phosphorous has five valence electrons, and only four of these are needed to bind the phosphorous atom

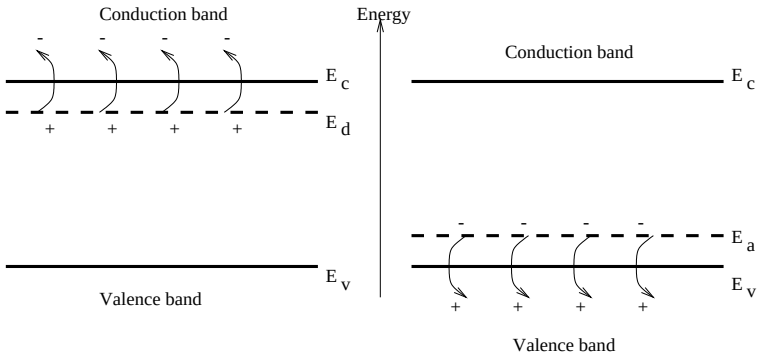


Figure 1.9: Energy band diagrams for donor and acceptor states.

to the silicon lattice, with the last electron rather loosely bound. The extra electron is called a donor electron, to indicate that little energy is needed to lift this electron to the conduction band. The energy states associated with the donor electrons must therefore be located in the band-gap rather close to the conduction band. When the donor electron is excited to the conduction band, it will leave a fixed positively charged phosphorous atom. Since this material is able to donate electrons to the conduction band without creating holes it is called a n-type semi-conductor.

In a similar way will a boron atom be able to create a p-type semi-conductor, creating so called acceptor states close to the valence band. This will leave negatively fixed boron ions when a hole is liberated to the valence band. Both donor and acceptor states diagrams are shown in figure 1.9.

A simple Bohr atom model for the donor electron, using the effective mass of the electron in the crystal and the permittivity of silicon instead of vacuum, will give approximate values for the energy of the donor states, close to the real value of $-45\,\mathrm{meV}$, compared to the band gap of $1.12\,\mathrm{eV}$.

The effect of adding dopant material will be to shift the Fermi-energy within the band-gap. Our formulas for n_0 and p_0 were general relations, and will still hold if the Fermi-energy move. Using figure 1.8 again (right plot), shifting the Fermi-energy upwards, we understand that the area representing the electron concentration must increase, whereas the area representing the hole concentration will decrease, and we have a n-type material.

We can rewrite the expression for n_0 and p_0 from equation 1.17 by introducing the intrinsic Fermi-level E_{Fi},

$$n_0 = n_i \exp\left(\frac{E_F - E_{Fi}}{kT}\right) \quad \text{and} \quad p_0 = n_i \exp\left(\frac{-(E_F - E_{Fi})}{kT}\right). \tag{1.19}$$

The product of these two equations gives the mass-action law of an extrinsic semi-conductor in thermal equilibrium, being the most important relation for semi-conductors,

$$n_0 p_0 = n_i^2. \tag{1.20}$$

1.4.4 Charge drift and diffusion

The electron and holes in a semi-conductor can move due to two different effects, either drift due to the electric field, or diffuse due to the gradients in concentration.

The drift velocity of a charge carrier is proportional to the electric field by the mobility, μ, as long as the electric field is not too strong. For most high purity semi-conductors this limit is around 20 kV/cm. Above this limit the velocity will start to saturate. The mechanisms that affect the mobility are phonon or lattice scattering and ionized impurity scattering.

The former is scattering of electrons and holes on the perturbing potential, set up by the vibrating lattice due to the thermal movement. Above zero temperature a fixed periodic potential model is no longer valid for the crystal. The mobility due to the lattice effect will increase as the temperature decrease, or more specifically $\mu_L \propto T^{-3/2}$.

The ionized impurity scattering is due to the added dopant, which is ionized at room temperatures. The holes and electrons will Coulomb scatter off these charged impurities. The mobility due to ionized impurities will decrease as the ionized impurity concentration increases, but it will increase with increasing temperature since added thermal movement will give less time in the vicinity of the impurities and therefore less probability of scattering. Mathematically we can write $\mu_I \propto T^{3/2}/N_I$.

It is easy to show that mobility is proportional to the mean time between collisions. If τ is the mean time between collisions, then dt/τ will be the probability of scattering in a time dt. The total probability must be the sum of the individual probabilities, such that $dt/\tau = dt/\tau_I + dt/\tau_L$, and since mobilities and mean times are proportional we understand that the total mobility μ must go as $1/\mu = 1/\mu_I + 1/\mu_L$.

In silicon the mobility is 1350 $\mathrm{cm}^2/(\mathrm{Vs})$ for electrons and 480 $\mathrm{cm}^2/(\mathrm{Vs})$ for holes at low doping concentrations, and a factor 3 higher for germanium. Gallium arsenide is special in that the electron mobility is very much higher than the hole mobility, being 8500 and 400, respectively. For silicon the mobility is almost constant up to an impurity concentration of $10^{16}\mathrm{cm}^{-3}$.

The total drift current density, J, is the product of the charge concentration and the drift velocity, with contributions from electrons and holes:

$$J_{\text{drift}} = e(\mu_n n + \mu_p p)E = \sigma E = \frac{1}{\rho}. \tag{1.21}$$

The equation also defines the conductivity, σ, and resistivity, ρ. In an extrinsic semi-conductor is $N_a \gg n_i$ for a p-type and at room temperature all acceptor states are ionized such that $p \simeq N_a$. The mass-action law states $np = n_i^2$ give us $n \ll n_i \ll p = N_a$, leading to $\sigma \simeq e\mu_p N_a$. This shows us that the conductivity depends on the majority carrier parameters only.

Charge carrier transport is also mediated by diffusion. Diffusion is the flow, $\mathbf{F}$, due to the gradient in concentration, c, and is generally stated in Ficks's law, $\mathbf{F} = -D\nabla c$, where D is the positive proportionality constant between the flow and the gradient in concentration. For the diffusion of carriers, we must for electrons have the current density $\mathbf{J}_n = -e\mathbf{F}_n$ and for holes $\mathbf{J}_p = +e\mathbf{F}_p$.

The total current density in a semi-conductor is found by adding the contributions from drift and diffusion, and is given as

$$\mathbf{J} = en\mu_n\mathbf{E} + ep\mu_p\mathbf{E} + eD_n\nabla n - eD_p\nabla p. \tag{1.22}$$

The constants D are the diffusion coefficients for electrons and holes. The Einstein relation relates mobilities and diffusion coefficients

$$D_n/\mu_n = D_p/\mu_p = kT/e. \tag{1.23}$$

1.4.5 Excess carriers

When excess carriers are found in the semi-conductor it will no longer be in equilibrium. If there exist a spot with excess electrons and holes in a semiconductor with an applied external electric field they will start to drift in opposite directions. As they come apart an internal electric field will be set up between the oppositely charged electrons and holes that try to hold them together. The effect of the external field will now be to drift/diffuse electrons and holes together. This phenomenon is called ambipolar transport, and it shows that the excess electrons and holes do not act independently, but will drift, diffuse and recombine with the same effective drift mobilities, diffusion coefficients and recombination life-times.

In equilibrium the direct band-to-band generation and recombination rates for electrons and holes must all be the same. If photons illuminate the semi-conductor, electron-hole pairs can be created, and electron and hole concentrations are increased above the equilibrium values; $n = n_0 + \delta n$ and similar for holes. For direct band-to-band generation and recombination it follows that $\delta n = \delta p$.

There will not be a continuous buildup since a recombination of electron and holes occurs at a rate proportional to both the electron and hole concentration:

$$dn(t)/dt = -\alpha_r n(t)p(t) + \alpha_r n_i^2. \tag{1.24}$$

The last term just ensures zero rate at equilibrium.

In terms of the excess electron (or hole) concentration δn defined above,

$$d(\delta n(t))/dt = -\alpha_r \delta n(t)(n_0 + p_0 + \delta n). \tag{1.25}$$

We introduce a very important condition called low-level injection, which assumes the excess carrier concentration much smaller than the majority carrier equilibrium concentration. This implies for the above equation that only the n_0 term will remain in the parenthesis for n-material and the p_0 term for p-material. The resulting differential equation has an exponential decay solution, with a time constant of $\tau_{n0} = (\alpha_r p_0)^{-1}$. We call this quantity the excess minority carrier lifetime, since it describes the mean time between re-combination of the excess minority carriers.

We can define continuity equations rather easily for electrons and holes by using Stokes law. The net increase of a quantity inside a volume element within a short amount of time

has to be equal to the gradient of the flux of this quantity into the volume element. In addition if there are any sources or sinks for this quantity inside the volume element, these contributions must be added and subtracted, respectively. For the holes we call the flux $\mathbf{F}_p$. There is one source within the volume element, due to the generation rate of holes g_p, and one sink, due to the recombination. The recombination rate must be proportional to the hole concentration and inversely proportional to the lifetime of holes τ_{pt}. This lifetime is for the total hole concentration, and involves both the lifetimes of thermal equilibrium holes and the excess carrier holes.

In total we will have a continuity equation for holes (and similar for electrons) of

$$\partial p/\partial t = -\nabla \mathbf{F}_p + g_p - p/\tau_{pt}. \tag{1.26}$$

We have earlier found the current densities for electrons and holes in equation 1.22, and these are of course just the particle fluxes multiplied by the carrier charge, since a current density is nothing more than a flux of charges. If we insert the current density equation into the continuity equation we arrive at the time dependent diffusion equations for electrons and holes, the one for holes being

$$\partial p/\partial t = -\mu_p \nabla (p\mathbf{E}) + D_p \nabla^2 p + g_p - p/\tau_{pt}. \tag{1.27}$$

In the case of a homogeneous semi-conductor, n_0 and p_0 does not depend on space coordinates, and δp can be substituted for p several places in the above equation.

$$\partial(\delta p)/\partial t = -\mu_p(p\nabla \mathbf{E} + \mathbf{E}\nabla\delta p) + D_p\nabla^2\delta p + g_p - p/\tau pt. \tag{1.28}$$

The electric field in this equation involves both a component from the applied external field and in addition the induced internal field due to the ambipolar transport. It can be argued that the internal component is much much smaller than the external component, because only a very weak field is needed to keep the electrons and holes drifting together. Since the difference in excess electrons and holes is related to the internal field through a Poisson equation, we can write in the one-dimensional case

$$\frac{e(\delta p - \delta n)}{\varepsilon} = \frac{\partial E_{int}}{\partial x}. \tag{1.29}$$

This leads us to the condition of charge neutrality. We can assume as a first approximation that the excess electron and hole concentrations are equal at every point in space. From now on we will write δn for both δn and δp. Equation 1.27 together with the same equation for electrons can now be added together, after the first is multiplied by $n\mu_n$ and the second by $p\mu_p$, and using the fact that $\delta p = \delta n$, and that the generation rates are equal $g_p = g_n = g$ and that the recombinations are equal $R = n/\tau_{pt} = p/\tau_{nt}$,

$$\partial(\delta n)/\partial t = \mu'\mathbf{E}\nabla\delta n + D'\nabla^2\delta n + g - R. \tag{1.30}$$

Here the ambipolar mobility μ' and the ambipolar diffusion coefficient D' are introduced. It must be noted that these are not constants, but functions of the total electron and hole

concentrations n and p. If we consider extrinsic semiconductors ($p_0 \gg n_0$ for p-type and $p_0 \ll n_0$ for n-type) and low-level injection ($\delta n \ll p_0$ for p-type and similar for n-type) we see that D' and μ' are approximated by $D' \approx D_n$, $\mu' \approx \mu_n$ for p-type and by by $D' \approx D_p$, $\mu' \approx -\mu_p$ for n-type. We see that the equation only contains the mobility and diffusion coefficient of the minority carrier.

The generation-recombination term $g-R$ can also be written in terms of excess minority carrier parameters, as $g - R = g' - \delta n/\tau$, where g' is the generation rate for excess carriers and τ the excess carrier lifetime.

By using Shockley-Read-Hall recombination theory one can show that the excess carrier lifetime is more or less a function of the number of defects. In the limit of low-injection it will reduce to the minority carrier lifetime value. The generation rate will be proportional to the defect number and inversely proportional to the excess carrier lifetime.

1.4.6 The diode

A piece of a semi-conductor can be used as a photo-detector, and is then called a photo-conductor. Incident photons will create e/h-pairs, which will increase the conductivity, since the conductivity is proportional to the charge concentration. With an applied voltage over the material the incident photons will increase the DC current and the increase will be proportional to the photon flux. Since the excess carrier concentration will be much less than the majority carrier concentration, the signal is small and easily drowns in the shot noise of the DC current. It is also slow since the current will die out exponentially after the photon flux stops, with a time constant of the mean carrier lifetime, which is in the order of a μs.

Instead the most used photon and charged particle sensor is a reverse biased diode, having superior performance compared to that of a photo-conductor. The diode is the simplest structure containing both n- and p- semi-conductor material in the same device, being formed out of a single crystal. The interface between the surfaces is called the metallurgical junction.

We think in terms of two pieces of semi-conductor materials brought together to understand what will happen at the junction. At first large diffusion gradients will exist, and majority carrier holes will diffuse into the n-material and vice versa for electrons. This will soon leave behind fixed negatively charge acceptor atoms in the p-area and fixed positively charged donor atoms in the n-area. In between these two regions, called space charge regions, an electric field is formed. This field tends to stop the diffusion and an equilibrium state is reached where diffusion and drift due to electric field cancel each other. This is schematically shown in the upper part of figure 1.10.

In thermal equilibrium the Fermi energy level must be constant throughout the diode. The Fermi-level in n- and p-material is situated in opposite ends of the energy gap and electrons in the conduction band of the n-material will see a potential barrier stopping it from entering the conduction band of the p-material. The height of this barrier is equal to the sum of the difference between intrinsic and actual Fermi level in each of n- and p-material, or $V_{bi} = (E_{Fi}(n) - E_F(n)) + (E_F(p) - E_{Fi}(p))$. The expressions in each of the

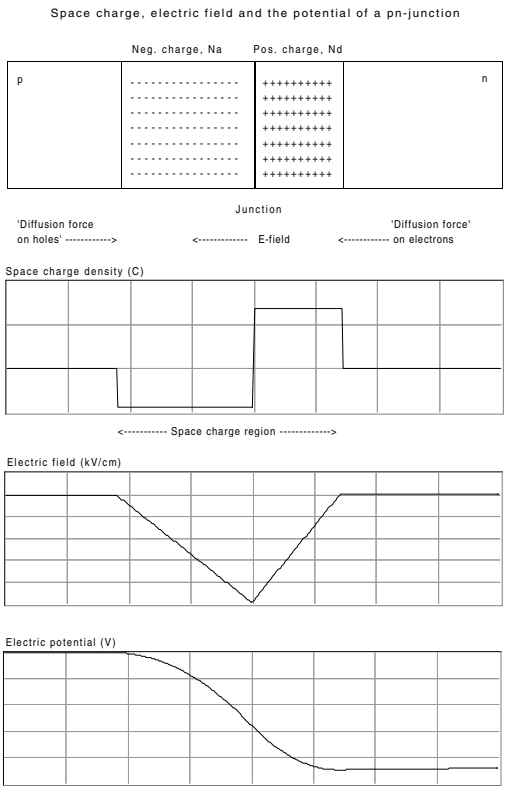


Figure 1.10: A pn-junction, its space charge, electric field and potential.

parenthesis are familiar from equation 1.19. If we also assume full ionization ($p_0 = N_a$ in p-region and $n_0 = N_d$ in n-region) we find that the barrier, also called the built-in voltage is

$$V_{bi} = \left(\frac{kT}{e}\right) \ln\left(\frac{N_a N_d}{n_i^2}\right). \tag{1.31}$$

Assuming an abrupt junction at $x = 0$, and also that the space charge region ends abruptly at x_n and $-x_p$ for n- and p-material, we can write the charge density

$$\rho(x) = \begin{cases} -eN_a & -x_p < x < 0 \\ eN_d & 0 < x < x_n. \end{cases} \tag{1.32}$$

The electric field and the potential are found using Poisson's equation,

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{dE(x)}{dx} \tag{1.33}$$

performing two integrations the first gives the electric field and the second the potential. The resulting space charge, electric field and the potential is shown in figure 1.10. Since E is continuous at $x = 0$ and also zero outside the space charge region, the equation for E leads to

$$N_a x_p = N_d x_n, \tag{1.34}$$

which is the same as saying that the area limited by $\rho(x)$ (the charge concentration in cm^{-2}) is the same for x above and below $x = 0$ (in n and p regions).

Using the expression found for ϕ one finds the built in potential to be

$$V_{bi} = \phi(x_n) - \phi(x_p) = \frac{e}{2\varepsilon_s}\left(N_d x_n^2 + N_a x_p^2\right), \tag{1.35}$$

and also the width of the space charge,

$$W = x_n + x_p = \left(\frac{2\varepsilon_s V_{bi}}{e}\left(\frac{N_a + N_d}{N_a N_d}\right)\right)^{1/2}, \tag{1.36}$$

where the last step in this equation is performed by using equations 1.34 and 1.35 to eliminate x_p and x_n in favor of the built-in potential.

When the diode is reverse biased, it is no longer in equilibrium, and the total barrier seen for electrons trying to move from the conduction band in n to the conduction band in p will be the sum of the built-in potential and the applied reverse bias, or $V = V_{bi} + V_R$. In the above equations this implies that we have to replace V_{bi} with V. The effect of the reverse bias will be to increase the depletion width.

The capacitance of the pn-junction is defined as $C = dQ/dV_R$, where Q is the charge and V_R the applied reverse voltage. A reverse biased diode can be looked upon as a capacitor with an associated leakage current. When operating at V_R, the effect of an incremental voltage, dV_R, will be that the junction will grow dx_n on the n-side and dx_p on the p-side. Since the space charge densities are known to be N_d and N_a in these areas, respectively, the incremental charge in the p and n regions will be (opposite signs) $dQ = eAN_d dx_n = eAN_a dx_p$, where A is the area of the junction. The junction capacitance is therefore

$$C = dQ/dV_R = eAN_d dx_n/dV_R. \tag{1.37}$$

Our earlier equations will allow us to write x_n as a function of V_R so that the derivative dx_n/dV_R can be found. The final equation is thus

$$C = A\left(\frac{e\varepsilon_s N_a N_d}{2(V_{bi} + V_R)(N_a + N_d)}\right)^{1/2} = A\varepsilon_s/W \tag{1.38}$$

The last step shows the similarity to an ordinary parallel plate capacitor, where the capacitance drops inverse proportional to the plate distance.

1.4.7 The diode as a sensor

Our main motivation when using the diode as a particle sensor is to reduce its inherent noise, or more clearly to increase its signal to noise ratio. This will immediately gives us some constraints to the type of diode we want to build.

An analysis of the sensor and front-end input step will show that the noise will decrease with the input capacitance seen by the front end amplifier. This immediately implies from 1.38 that the diode should be fully depleted since this maximizes W, and minimizes C.

We also choose to have an one sided junction, which means we usually select a very low n-doping (in the $5 \cdot 10^{12}\mathrm{cm}^3$) and a high p-doping ($10^{15}\,\mathrm{cm}^3$). Since the depletion widths into the different charge regions are inversely proportional to the doping, we will have to choose a p^+n-junction. For a $300\,\mu$m thick diode, 100 V reverse voltage will assure full depletion, with the junction extending $300\,\mu$m into the n material and less than a μm in the p+ material. The n-material is the detector volume where the passing particles can create eh-pairs.

For a given thickness, the signal can be calculated. A minimum ionizing particle will lose on the average 117 keV in $300\,\mu$m Si, with 78 keV as the most probable value, due to the asymmetric Landau distribution explained later. The ionization needed for an energy/hole pair is known, about 3.62 eV at 300 K and increasing to 3.81 eV at 77 K, where Germanium has 2.96 eV. This gives us 32400 eh-pairs on the average (108 pairs/μm) and 21600 (72 pairs/μm) as the most probable in $300\,\mu$m of Silicon. For a required minimum signal-to-noise of a system, the maximum noise acceptable can be calculated, with the limitation this puts on the front-end, the read-out electronics and the sensor capacitance.

To have a very low doped detector material can be motivated in several ways:

- The low doping give high mobilities, giving short collection times for the electron and holes, leading to fast detectors.

- It is also practical from the biasing point of view, since only biasing voltages in the few hundred volt range are necessary to fully deplete the sensor, whereas for higher doping several thousand volts would be necessary. With the given practical operating voltages of a few hundred volts up to about a thousand volt, typical thicknesses will be from $200\,\mu$m up to about one millimeter.

- The most important factor however is again the lower noise, since low doping gives a much lower reverse current in the diode. The shot noise effect of the reverse DC current is a noise contribution to the signal from the traversing particle. The current in the reverse biased diode has two components. The first is given by the diode equation and it goes exponentially with the applied diode voltage. Since we choose to operate the diode in extreme reverse direction this current is essentially immeasurable. Instead our dominating reverse current will be the generation current.

The generation current is given by Shockley-Read-Hall recombination theory, which gives the recombination rate of excess electrons and holes. In our low doped n-material where electrons and holes have been swept out to give us a bare space charge region, the excess charge concentrations are virtually zero, and we will have a negative recombination rate. The negative rate implies that eh-pairs will be generated, and we call this the generation current of a reverse biased junction. The electrons and holes originate in the trap states inside the band gap, and are immediately swept out of the space-charge region. In equilibrium the rate for capture and emission into these states would be equal, but with an applied bias we are no longer in equilibrium and the goal of this process is to reestablish the equilibrium situation within the space charge area.

SRH-theory gives the generation rate to be

$$G = \frac{n_i N_t C_n C_p}{C_n + C_p} \tag{1.39}$$

as long as the trap states are in the middle of the band gap. The constants C_n and C_p describes the electron and hole capture cross sections. We see that the generation current increases with the trap concentration, N_t, which is the reason for choosing a low doped material. The generation current is found by $J_G = eAWG$, since AW is the volume where we have the rate G. The most important factors to note are that the generation current is temperature dependent, through n_i, which is approximately doubled for a $7-8\,\mathrm{K}$ temperature increase.

1.4.8 Silicon strip sensors

If we want to build a position sensitive sensor we need to segment the diode. This is the origin of the silicon strip sensor, where we typically divide the thin p+material into narrow strips, usually somewhere between 3 and $20\,\mu$m. The low doped n-material is usually around $300\,\mu$m thick.

The fabrication process [11] contains more or less the steps shown in figure 1.11;

- We start with the low doped n-wafer, with a very high resistivity of $1 - 10\,\mathrm{k\Omega cm}$, and a $< 111 >$ lattice orientation. The thickness is typically $280 - 500\,\mu$m.
- The n-material is passivated, by heating to above $1000^o\,\mathrm{C}$, oxidizing the surface, covering it by SiO_2.
- Photo-lithography and etching opens windows in the oxide on the top layer and exposes the back side, where we want the doping of the semi-conductor.
- The doping of the n-material to form p+ strips and the n+ backside can either be done by ion implantation or by diffusion. The ion implantation of the p-strips is usually done with low energetic boron atoms ($15\,\mathrm{keV}$ and exposure to $5 \cdot 10^{16}\mathrm{cm}^{-2}$) to make a very shallow p+ strip. The backside is usually exposed with more energetic astatinum, but to a lower dose ($30\,\mathrm{keV}$, $5 \cdot 10^{15}\mathrm{cm}^{-2}$). This will ensure a good ohmic contact to the backside. In the case of diffusion, the p+ strips are formed by depositing boron atoms all over by gaseous boron. This boron glass is then stripped away. The boron atoms that diffused into the silicon during the gas deposition phase, are further diffused into the material by heating the whole wafer to more than 900 degrees. This gives a p+ region of approximately $1\,\mu$m depth. The heating will also form a new layer of silicon oxide on top of the strips.
- The strips and the back side are metallized with aluminum to ensure good contact suitable for wire bonding. In the case of doping by diffusion one can either etch away the oxide on top of the strips, before applying the metal, thus giving DC coupled

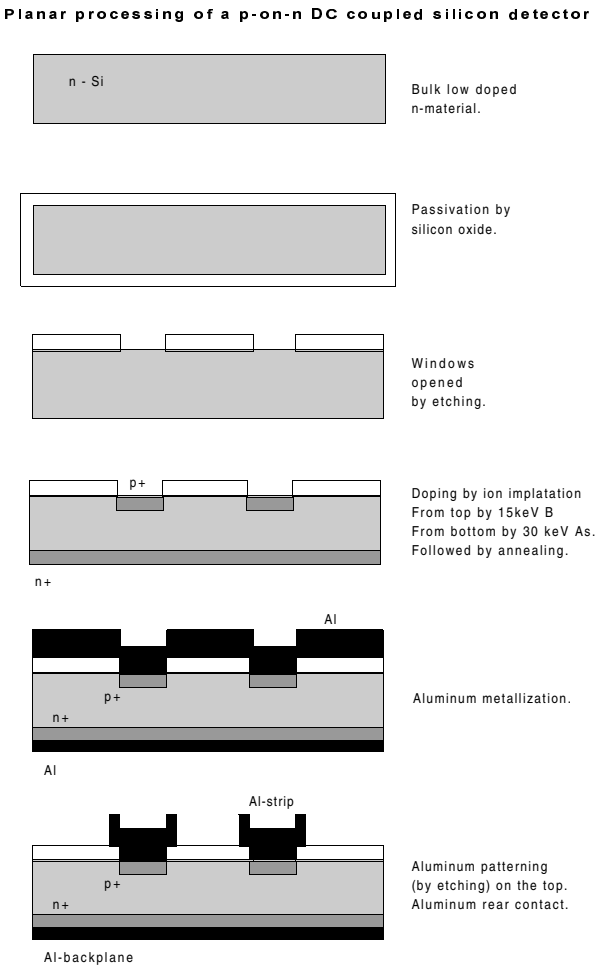


Figure 1.11: Planar processing of a DC-coupled single sided p-in-n silicon detector. The view is a cut through the detector. The p+ and Al-strips can easily be 6 cm long if the detector is manufactured on a 4 inch wafer.

detectors, or one can put the metal strip on top, forming an AC coupled detector. In the last case the capacitor is a parallel plate capacitor, with the aluminum strip being one plate and the p+ strip the other.

The described detector in figure 1.11 is a single sided DC-coupled device. During operation a large positive voltage is applied to the backplane to fully deplete (reverse bias) the detector diodes. The aluminum strip must be connected to the input of the charge amplifier. The amplifier is required to sink the leakage (reverse) current in the diode strip. This is acceptable as long as the leakage current is small. By radiation damage leakage current grows fast, and DC coupling is hence used for low radiation applications. Biasing schemes for DC-coupled, AC-coupled and double sided detectors are shown in figure 1.12.

If a silicon dioxide layer is put in between the aluminum strip and the p+ strip, forming an integrated capacitor, we have an AC-coupled detector. Shorts/holes in the oxide of the

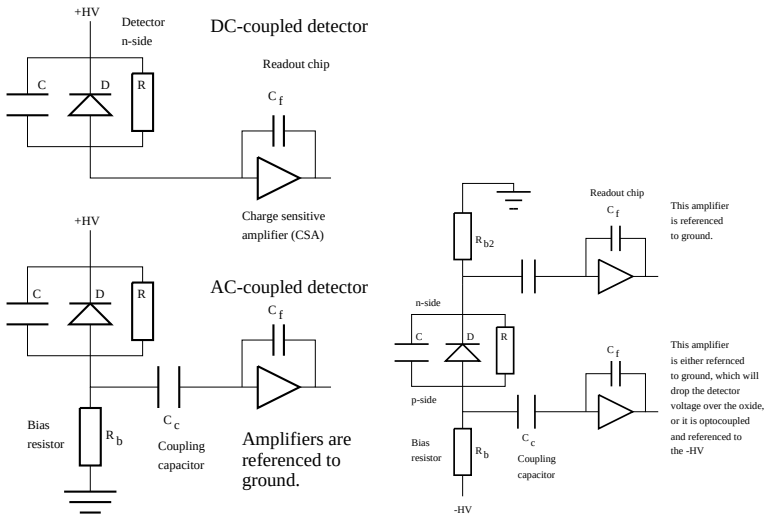


Figure 1.12: Biasing of single sided DC-, AC and doubled sided silicon strip detectors.

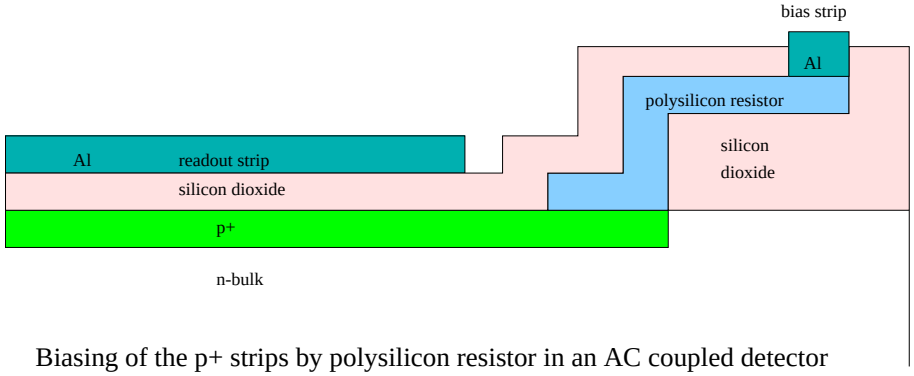


Figure 1.13: Biasing of silicon strip detector by poly-silicon resistors.

integrated capacitor will ruin the AC-coupling, creating so called pin-holes. One often adds a layer of silicon nitride as an extra insulator on top of the silicon dioxide, greatly reducing the probability of pin-holes.

Since the p+ strips are not connected to the aluminum strips in this case, a separate way of biasing the strips is needed. Several methods exist, the simplest called poly-silicon biasing [13]. In this case a separate resistor in poly-silicon is made for each strip, the other end of the resistor being connected to a common bias strip. This is shown in figure 1.13. Unfortunately there are two competing goals. A high resistance is needed because it reduces the S/N-ratio, discussed in a later sub-section. In addition, signal will be lost if the DC resistance in between the p+ strips are too low. Radiation damage will increase the leakage current in the diode, requiring a modest resistance value otherwise the voltage drop will be excessive. Usually a value in the $1 - 30\,\mathrm{M}\Omega$ range is used.

Two other methods have been developed to obtain the goal, which is a low DC resistance (avoid voltage drops due to the leakage current) and a high dynamic resistance (to avoid

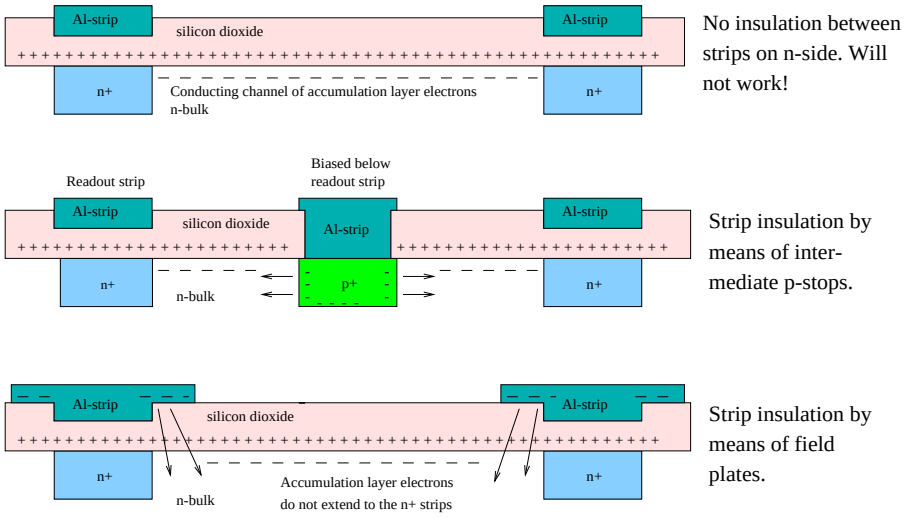


Figure 1.14: N-side strip insulation in double sided detectors by p-stops and by field plates. Both detectors are AC coupled devices.

signal loss). These are punch-through biasing [14] and FOXFET (Field OXide FET) biasing [15]. Studies have shown that poly-silicon biasing is the most robust solution, the other methods being more vulnerable to radiation damage manifested as excess noise [17] [18].

It is also possible to segment the n-side, thereby building a double sided detector. Typically the n-side strips are angled, often 90 degrees, relative to the p-strips. This achieves 2D-positioning of the particles. Figure 1.14 shows the AC coupled n-side of a double sided detector. The n+ is segmented into strips and the backside covered with silicon dioxide. The oxide is opened over the strips to allow for the connection to the aluminum strips. One big problem exists, however. During passivation positive fixed ion charges in the silicon oxide, will attract electrons to the surface of the n-material. This electron accumulation layer forms a conducting channel between the positive biased n+ strips, reducing inter-strip resistance to a few kΩ [12] [14]. Two methods to resolve the problem exist, insulation by p+ stops [19] and insulation by field plates [20], both illustrated in figure 1.14.

The p stop solution introduces a p+ stop line in between the readout lines. This line is supplied at a slightly lower voltage than the p+ strips. A depletion zone is formed between the p+ strip and the n bulk, with a negatively space charge in the p+ on the border to the n bulk. This space charge repels the mobile electrons of the surface accumulation layer, thus blocking the leakage path. The field plate solution is even more intuitive. If the readout aluminum strips are widened (given wings) such that they extend well outside the n+ implant and in addition are put at a voltage well below the n+ (as it would be if the HV is put on the n+ and the readout amplifier for the n side is at ground), a strong electric field will extend from the wings to the n bulk, repelling the electrons in the accumulation layer.

In many applications it is impractical to read out a double sided detector where the strips are angled at 90 degrees. Typically one is interested in placing the readout electronics in one end, as described in the detector ladders for BELLE discussed in chapter 3. This has been solved by introducing a second metal layer (giving the name double metal layer or DML-detectors) on one side of the detector. This extra layer has the aluminum strips angled at 90 degrees and connects to the underlying strips by holes in the oxide. A side effect is increased coupling between strips, which will increase the total capacitance and hence the noise.

1.4.9 Spatial resolution

The spatial resolution of a silicon strip sensor is influenced by several parameters. The first ones are the geometrical factors, including the etching accuracy of the sensor, the strip width, the strip pitch and the readout pitch (if we do not read out every strip). The outer operating conditions such as the angling of the detector plane and the application of an external magnetic field can both be a problem and an advantage. In the case of analogue read-out and a rather good signal-to-noise ratio, it can improve resolution by charge sharing over several strips.

Other factors are given by the inherent properties of the sensor, and its operating conditions. The eh-pairs created by the traversing particle is confined within a tube of approximately $1\,\mu$m around the track. As they drift, the electrons toward the backplane and the holes towards the strips, the charge clouds will diffuse out in the direction perpendicular to the drift, forming a Gaussian distribution of width $(2Dt)^{1/2}$, where t is time and D is the diffusion coefficient, related to the mobility via the Einstein relation. The smearing out of the charge cloud is not necessarily bad, it will depend on the readout pitch and the noise. This is easily understood since a spread of the charge cloud can give signal on several neighboring strips, and we can use a center of gravity method to localize the position to much better precision than the strip pitch. (A binary readout with pitch d, will have a resolution of $\sigma = d/12^{1/2}$). As the charge is divided onto more strips, less signal is found in each strip, and it will be more difficult to separate the signal from the noise in the strip. As long as the S/N of the system is good it is advantageous to use charge sharing to improve spatial resolution. In this case we use a bias voltage just above full depletion. A higher voltage would just give a higher drift field resulting in shorter charge collection time. This will give a lesser smearing and higher probability of single strip events, reducing the resolution.

Remaining factors are related to the statistical nature of the ionization. The energy loss in a relatively thin material like the silicon sensor is not Gaussian in shape, which it would have been if the sensor was much thicker. The exact distribution is very difficult to calculate since we have the possibility of large energy transfers in single collisions, due to production of high energetic primary electrons by hitting them more or less head on. This is worst for incident electrons that can transfer as much as half its initial energy. This comes in addition to the more or less quasi-continuous ionization energy loss giving low energetic electrons. A first approximation to the loss distribution is the Landau distribution, seen in figure 1.15.

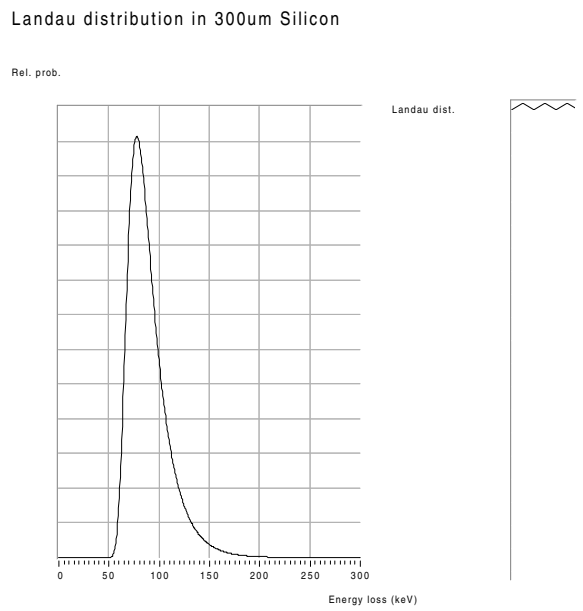


Figure 1.15: Landau distribution for energy loss in a thin absorber. In this case 300 μm of Silicon.

The plot is based on a closed form approximation of the Landau distribution [40] given by

$$p(E_p) = \sqrt{\frac{e^{-\lambda - e^{-\lambda}}}{2\pi}}, \tag{1.40}$$

with $\lambda = R(E - E_p)$, where R is a material dependent constant, E is the energy loss and E_p the most probable energy loss. In evaluating the Landau distribution one assumes infinite maximum energy transfer, free electrons and constant traversing particle velocity. The distribution looks Gaussian but has a long tail towards higher energy loss, resulting in an average energy loss much higher than the most probable energy loss. The actual loss distribution is even broader than the Landau distribution. Corrections by Vavilov [2] taking into account a finite maximum energy transfer, results in a distribution that better fits experimental data.

The probability of ejecting a primary electron (δ-electron) with energy above a certain threshold is given in figure 1.16. The figure contains an additional plot that shows the effect on the displacement of the centroid (error in position due to the ionization of the δ-electrons). A little example [12] will illustrate the effect. Figure 1.16 shows us that the probability for ejecting a $> 100\,\mathrm{keV}$ e^- is around $2 \cdot 10^{-4}/\mu$m, and for a 300 μm sensor this is around 6%. If this electron moves perpendicular it will reach in average 40 μm, depositing around 30000 secondary e^- along its way. We can think of this as around 30000 e^- created 40 μm/2 away from the incident track which deposited about $33000\,\mathrm{e}^-$. The displacement from the true position will be given by the centroid of the two charges separated by 20 μm, where the incident track is taken to be at $x = 0\,\mu$m, or in this case

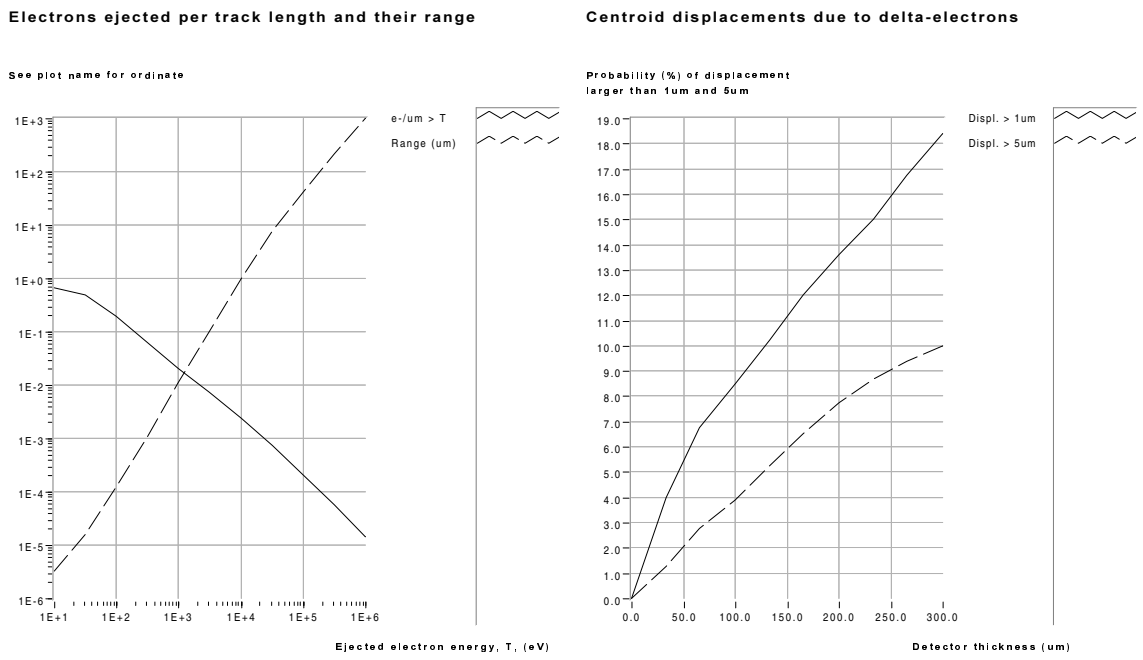


Figure 1.16: δ-electron ejection probability and its position displacement effect.

$(33000 \cdot 0 + 30000 \cdot 20\mu\text{m})/(33000 + 30000) \approx 9.5\,\mu$m. A check on the total charge released could indicate if there is excess ionization due to δ-electrons. This is however seldom implemented, except maybe from test-beam measurements.

1.4.10 Noise of the sensor and pre-amplifier system

In the case of a well designed silicon sensor and a good charge sensitive pre-amplifier, the capacitance of the sensor as seen by the pre-amplifier is the most important design parameter of the sensor to control noise. This is seen from the formula for the equivalent noise charge of the pre-amplifier

$$\text{ENC}_{\text{amp}} = k_0 + k_1 C_l. \tag{1.41}$$

It should be stressed that this formula give the only the ENC due to the pre-amplifier, and depends only on the capacitive load of the sensor, C_l. In addition the detector has its own noise sources and these will add in quadrature:

$$\text{ENC}^2_{\text{TOT}} = \text{ENC}^2_{\text{amp}} + \sum_{i=\text{det.sources}} \text{ENC}^2_i \tag{1.42}$$

The ENC gives the noise as a charge referred to the input of the pre-amplifier. This has the advantage of an easy direct comparison with the input signal charge, making the S/N calculation very easy. The constants k_0 and k_1 describes the pre-amplifier-shaper chain and

CMOS chips with $k_0 = 40\mathrm{e}^-$ and with $k_1 = 0.7\mathrm{e}^-/\mathrm{pF}$, like the VA3 and the VAHDR3 [21], exist for peaking times around a few microseconds.

The capacitance of a sensor strip has several components [27], one part is the capacitance between the strip and backplane, C_s, the next part is the capacitance towards the backplane via neighboring strips. We can think of the total capacitance to all neighboring strips, C_i, as measured by a capacitance meter connected between the wanted strip and in the other end to all other strips connected together. In practice a good enough accuracy is reached by measuring to the two closest neighbor strips (inter-strip capacitance). In the case of an AC coupled detector there is also the coupling capacitance in series, C_c. The total capacitance seen by the pre-amplifier is thus the sum of the strip capacitance and inter-strip capacitance, and this sum in series with the coupling capacitor. For the pre-amplifier to receive most of the charge the coupling capacitor should be much higher than the two others, since the fraction of charge ending on the coupling capacitor will be, $C_c/(C_c + C_s + C_i)$, which is closest to one for large C_c. The effective capacitance seen by the pre-amplifier is in this case $C_s + C_i$. It is also obvious why the pre-amplifiers are usually called front-end amplifiers. If these were to be placed further away the wiring capacitance would increase and the S/N go down.

The noise sources inherent in the sensor itself are the shot noise, the thermal noise and the series resistance noise. The two first ones are parallel noise sources, the latter is a series noise source. The shot noise is due to the leakage current of the diode strip, I_l. This current has several sources as mentioned earlier. First the ideal diode current equation gives a negligible contribution. The contribution from the generation current, originating from trap centers serving as intermediate states for recombination as given by SRH-theory, is much bigger. In addition there are surface effects, which are very hard to calculate. These effects depend on surface states, the smoothness of the cut edge, guard rings, contaminations, surrounding atmosphere and mounting [2]. Under mounting an important consideration is the type of glue used on the sensor and stresses introduced.

The contribution to the ENC by the leakage current (lc) is given by,

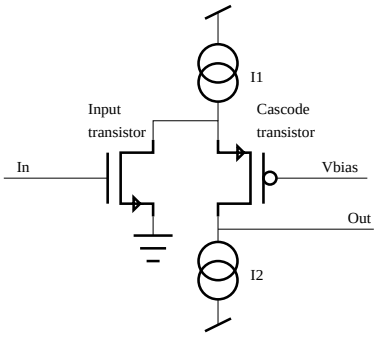
$$\mathrm{ENC_{lc}} = \frac{1}{2}\frac{e}{q}\sqrt{qI_lT_p}. \tag{1.43}$$

The constant $e \approx 2.7183$ is the base of the natural logarithm, and $q \approx 1.6022 \cdot 10^{-19}\,\mathrm{C}$ the electron charge. The peaking time of the pre-amplifier-shaper is given by T_p. The temperature enters this formula through the leakage current.

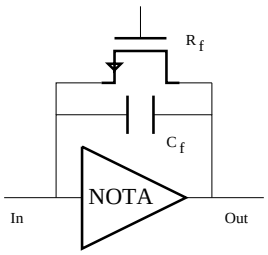
The thermal noise is contributed by the parallel of the strip bias resistor and the amplifier feedback resistor, denoted by R_p. The latter usually being so large, above $50\,\mathrm{M\Omega}$, that this is essentially the bias resistor value itself. The bias resistors are typically in the range $1 - 30\,\mathrm{M\Omega}$, and the noise contribution is usually negligible compared to the shot noise for values above $20\,\mathrm{M\Omega}$. The expression for the ENC contribution by the parallel resistor (pr) is given by,

$$\mathrm{ENC_{pr}} = \frac{1}{4}\frac{e}{q}\sqrt{kTT_p/R_p}. \tag{1.44}$$

Here $k \approx 1.3807 \cdot 10^{-23}\,\mathrm{J/K}$ is Boltzmann's constant and T the temperature.



NMOS input type OTA (NOTA)



NOTA configured as
integrating CSA

Figure 1.17: An operational transconductance amplifier (OTA) in a CMOS process. It is also illustrated how to configure it as a charge sensitive amplifier (CSA).

Series resistance noise is due to the thermal noise in the strip resistance. In ATLAS one motivation to choose readout in the middle of the 12 cm long strips, is that it reduces the series resistance to one fourth. The expression for the series noise (sr) is given by,

$$\mathrm{ENC_{sr}} = \frac{1}{4}\frac{e}{q} C_t \sqrt{kT R_s / T_p}, \tag{1.45}$$

where C_t is the total input capacitance, which is the sum of the detector load capacitance, C_l, and the gate capacitance of the input transistor, C_i, in addition to the feedback capacitance and stray capacitances.

The remaining noise sources are due to the pre-amplifier. We could envisage three types of amplifiers, current sensitive, voltage sensitive and charge sensitive. The first is only useful with low impedance signal, which is not the case with diode sensors. The voltage sensitive amplifier will amplify the input signal, V that is built up on the total capacitance seen by the pre-amplifier input, C_{TOT}, by means of the input charge, $V = Q/C_{TOT}$. This capacitance is built up by stray capacitance in the circuit, sensor capacitance and input capacitance on the input transistor. Neither of these are stable over temperature or time. The best solution will be to use a charge sensitive amplifier (CSA), integrating up the charge from the eh-pairs produced by the particle interaction. This is illustrated in figure 1.17. As long as the gain in the amplifier is high, the inverting input node is forced to a constant voltage, and the input charge will accumulate fully on C_f, the voltage on the output being $V_o = -C_f Q$. The response to a fast current spike in the sensor will be a voltage step on the CSA output, making the circuit an integrator.

The charge accumulated must be removed, otherwise the voltage would just pile-up. This is normally done by placing a resistor in parallel with C_f. This means that the step pulses piling up on each other for each new particle will have an exponential decay, usually with a rather long time constants compared to those of the following shapers. Another solution would be to use optical feedback, allowing pile-up to a certain level before a reset is performed, to restore the starting DC level [2]. We need to use a FET input transistor,

which has an extremely low input current, since we would like to bias it with a very big feedback resistance. Pulse shaping in the pre-amplifier stage is avoided, since the filter action of a smaller feedback resistor and C_f is more than ruined by the higher parallel noise.

The amplifier most often used to build the CSA is an OTA, or an operational transconductance amplifier. A special way of building an OTA is to use a configuration based on a single-ended folded cascode (SEFC). The SEFC OTA was first proposed by Veljko Radeka and is also known as the Radeka-star. Since the pre-amplifiers are often built in CMOS technology, figure 1.17 shows an OTA based on NMOS input transistors, and its configuration as a CSA [8].

In analyzing the effect of the pre-amplifier noise sources, we need to take into account the following filtering circuitry. The goal of the filtering circuitry is to limit the band-width, and in such a way as to optimize the circuit for the best possible S/N. The most common pulse shaping is CR-RC pulse shaping, consisting of a CR differentiator and a RC integrator. The frequency response of this filter will be

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{sC_dR_d}{1+sC_dR_d} \cdot \frac{1}{1+sC_1R_1}. \tag{1.46}$$

We choose component values such that $\tau = R_dC_d = R_1C_1$, and the filter response reduces to

$$H(s) = \frac{s\tau}{(1+s\tau)^2}. \tag{1.47}$$

This will assure minimum noise. It can be shown theoretically that the minimum noise would occur for Gaussian-shaping. CR-RC shaping is often called semi-Gaussian shaping, since the limit of CR-$(RC)^n$ shaping (several RC integrators in a row) as n increases towards infinity, will be the Gaussian shaping. Usually n does not need to be more than four or five. The disadvantage is that the pulse is much wider than the single CR-RC shaping, making it impractical. In addition one can show theoretically that the S/N for Gaussian shaping is only 18 percent lower than for CR-RC shaping.

In practise the shaper is built as a CSA like the pre-amplifier, but with other values for R_f and C_f. In between the pre-amplifier and the shaper a coupling capacitor is required, providing the nominator s in the CR-RC transfer function in equation 1.47. The denominator comes from the R and C in the shaper OTA feedback, providing an $1/(\tau s)$. The other factor, to square the denominator, comes from the low-pass effect of the band-width limited shaper OTA. Reducing the current in the OTA will limit its band-width. These two time constants are tuned by biasing and design parameters of the OTA.

The only important part of the pre-amplifier contributing to the noise is the input transistor [9]. There are three main sources of this noise. Two of these sources are white, being the channel thermal (ct) noise and the bulk series resistance (br) noise in the input transistor. The latter is usually unimportant, since it by careful design will be much less than the first. There exist also a Flicker-noise (1/f) in the input transistor having a spectral density with an $1/f$ dependency. The Flicker component is usually larger in MOS devices

compared to bipolar devices and it originates due to fluctuations of charge in the gate-channel interface, which will modulate the conducting channel [10]. The fluctuations come from trapping-detrapping in the silicon oxide. The ENC due to the amplifier is given as;

$$\mathrm{ENC_{amp}} = \frac{e}{q} C_t \sqrt{\overline{V_{\mathrm{on}}^2}}. \tag{1.48}$$

Here the $\overline{V}_{\mathrm{on}}^2$ denotes the noise voltage relative to the output of the preamp-shaper.

The noise voltage contains three terms,

$$\overline{V_{on}^2} = \frac{\mathrm{n}kT}{mT_p g_m} + \frac{R_{\mathrm{bulk}}\eta^2 kT}{2T_p} + \frac{F_k}{2WL_{\mathrm{eff}}}, \tag{1.49}$$

corresponding to the channel thermal noise, the bulk series resistance noise and the Flicker noise in this order. The W and L_{eff} are the width and length of the input transistor and g_m its transconductance, which depends on the width, length and drain current. Typical values of g_m are around 3 mA/V for dimensions of W/L_{eff} = few mm/one μm and drain current in the few hundred μA range. The constant n is called the slope factor, and is more or less an excess noise factor being in the order 1 to 1.5. Depending on whether the input transistor works in strong or weak inversion, the parameter m should be 3 or 4. Typically we are somewhere on the edge and a value in between is suitable. The bulk resistance is given by R_{bulk} and is typically in the order of 2 kΩ, whereas $\eta \approx 0.15$ and is typically lowest for the highest possible bulk-to-source voltage. The Flicker noise coefficient, F_k, is typically around $7.6 \cdot 10^{-22}$. The values quoted are typical values of the Mietec 1.5 μm CMOS process [9].

To minimize the noise voltage spectral density of these three noise sources we will have to:

- Maximize the transconductance, g_m, of the input transistor. Since in strong inversion the transconductance is approximately $(I_d W/L_{\mathrm{eff}})^{1/2}$, we should have a large transistor width, W, a short effective transistor length, L_{eff}, and a high drain current, I_d.

- Minimize the g_{mbs}/g_m, g_{mbs} being the bulk-to-channel transconductance. This is usually achieved by having a high source-to-bulk voltage.

- Empirically it seems to introduce excess noise to have sub-micron effective channel length, which means that L_{eff} should not be to small.

If we expand the C_t of equation 1.48 into $C_t = C_l + C_{rest}$, the familiar equation 1.41 is obtained with

$$k_0 = \frac{e}{q} C_{rest} \sqrt{\overline{V_{on}^2}}, \tag{1.50}$$

and

$$k_1 = \frac{e}{q} \sqrt{\overline{V_{on}^2}}. \tag{1.51}$$

The noise spectral densities for the Flicker noise and the channel thermal noise contain the gate capacitance itself, since the capacitance is given by the dimensions of the transistor. This means that for a given detector capacitance, C_d and feedback capacitance, C_f, it will be possible to select a gate capacitance that minimize either the Flicker noise or the channel thermal noise. The optimal gate capacitance is $C_d + C_f$ in the first case and $(C_d + C_f)/3$ in the second case. The optimal choice is somewhere in between depending on the relative strength of the two noise types. For peaking times around $1\,\mu$s the channel thermal noise is usually dominant. Since we use a L_{eff} as small as possible allowed by the CMOS process (as long as it is not sub-micron), we can calculate the transistor width as soon as the optimal gate capacitance is known.

1.4.11 Radiation damage

Irradiation of semi-conductors produce the wanted signal (electron-hole pairs) by means of transient ionization. The degradation of the semi-conductor can be divided into two categories [22] [23]:

- Bulk damage by displacements. Atoms are dislocated from their normal positions in the lattice, producing less ordered structures.
- Surface damage by long term ionization. Charged regions are induced in the insulators when electrons and holes produced are fixed and do not return to the initial state. This will change the electric field close to the interface. Silicon/silicon-dioxide interface levels are also induced.

Displacements are progressing through several steps:

- The particle hits an atom and displaces it. Interstitials and vacancies appear. At high energies nuclear reactions can occur creating fragments (secondary particles).
- Fragments migrate and creates further displacements.
- Thermal motion will rearrange lattice defects at room temperature. This is an important effect called annealing. The annealing is partly influenced by the initial impurity level of the material.
- The thermal stable defects will permanently alter the semiconductor properties, and therefore also the detector parameters.

For silicon detectors the most important effects are in the increase of capture, generation and recombination rates. This will among other effects increase the leakage current. The low doped n-material will during irradiation turn less and less n and will at a certain radiation level go through a type inversion, ending up like a p-doped material. This is the result of radiation induced deep level defects turning out to be of acceptor type. This will change the internal field in the detector, and the ohmic and junction side will swap

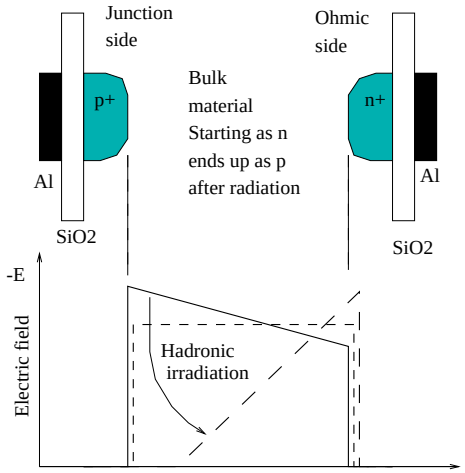


Figure 1.18: Changes in electric field through irradiation of a double sided micro-strip detector [13, page 32].

position. This is illustrated in figure 1.18 for a double sided detector. When starting out with a strongly over-depleted detector, the electric field is more or less uniform. The field is decreasing towards the n-side (ohmic side). After type inversion the resistivity will steadily decrease, and at a certain level a fixed operating voltage will not manage to fully deplete the detector and the hole signal will be lost. The electron signal will still be collected, but from an active detector thickness (depletion width) steadily decreasing [25]. As a consequence the detector will have to be operated at higher bias voltage to ensure full depletion.

After irradiation the annealing will reduce the leakage current with time. Both short and long term annealing effects exist, which can be described by a sum of exponentials. There is also a substantial non-beneficial annealing effect, usually called anti-annealing. This effect causes serious concern since the depletion voltage increases with the square of the doping concentration. Only 30% anti-annealing can exceed the safe operating voltage of the detectors. Anti-annealing is very temperature and fluence dependent. Low temperature reduces the effect of anti-annealing strongly. Great care must however be taken since maintenance and warm-up periods must be expected during the life-time of a detector.

1.5 Description of a general detector system

This thesis will focus on the assembly of silicon micro systems and on the electronics and read out of these systems. In most cases such a system will be modular, dividing it into front-end modules connected with long cables to a back-end read-out system. The most critical steps in the construction of such a front-end system (module) are design, processing and testing of:

- The sensors and the read-out chips.

- The finished readout boards/hybrids/modules.

1.5.1 Sensors and front-end chips

The importance of careful **design**, **processing** and **testing** of the sensors and the individual read out chips is:

- For the most important **design** parameter, noise, is it easily motivated. As long as the rest of the read out chain is carefully designed (engineered) the noise is only dependent on the inherent noise sources of the detector itself (which cannot be removed) and on the input stage of the front-end amplifier. This requires a good low noise front end design, as explained in the previous sections.

- The choice of the actual **process** for the front-end, like CMOS, bipolar or BiCMOS, and the material like silicon or GaAs, relies on the requirements to speed, S/N and radiation hardness.

- Single chip **testing** on wafer is essential since very high yield is seldom found. To assemble and rework read-out boards/hybrids with several bad chips are much more time consuming and costly than testing the individual chips. It must be proved that wafer testing gives results that are very close to what are measured on assembled boards/hybrids. This requires very low noise test methods.

My work has mainly been concerned with the last point. A very low noise read-out and test system for VA chips has been developed, called VA-DAQ. The VA-DAQ system can be configured for testing single chips on wafer with a probe card, or the finished read out boards. Automatic testing measuring all vital parameters exist, which will produce a data sheet containing the result. Cuts can be defined on all these parameters to locate bad channels or overall chip parameters that are not acceptable. Results from probe testing and assembled boards are given and compared, to show the validity of the probe testing and also typical spread in parameters for VA-chips. The example chip used is VA1 and the board is the readout board designed by the author to read-out the Silicon Vertex Detector (SVD) in the Belle experiment.

In addition it should be mentioned that the VA-DAQ system is a full readout system that can be used in experiments where the front-end is based on VA/TA-type of chips. Full software exist to dump data from a system under test and to later analyze them off-line. Examples of results with the VA-DAQ readout system are presented.

1.5.2 Readout boards

The importance of careful **design**, **processing** and **testing** of the readout boards is:

- The **design** of the read out hybrid requires good knowledge of low noise electronics, and all the techniques necessary to avoid noise sources to couple into the signal read-out chain, thereby reducing the inherent signal-to-noise ratio of the sensor/front-end

stage. Items that needs careful engineering are grounding schemes, which needs extreme considerations since its vital to have good performance. Other important factors are low impedance supply/grounds paths usually achieved by planes or fat tracks to minimize resistivity part and decoupling close to chips to have low impedance return path. Other key issues are the use of differential low swing digital signals to minimize capacitive couplings to sensitive analogue parts.

- The **processing** selected for the readout board depends on several factors. The most important mechanical constraint is usually to minimize the total material since this improves the tracking , which otherwise are worsened by multiple Coulomb scattering in the module material. This constraint needs to be balanced against the need for material to assure the wanted mechanical stability (especially if the module is itself a part of the alignment of the sensor) and need for good thermal transport of the heat produced by the sensor and the readout chips. For the electrical properties, one must select a process that gives the necessary resistivity of tracks (Cu, Au, Ag), the required minimum track separation (chips are bare silicon and must be bonded at small pitches), bondable and solderable/gluable conductors and the necessary minimum permittivity (to reduce capacitive couplings).

- The **testing** is needed to confirm that the full board fulfills all the specifications given. The same test system can usually be employed for both chips on wafer and for finished boards.

On the board/hybrid/module level I have been involved in all three phases. In the design phase I have constructed boards covering a wide range of experiments. The experiments used to exemplify designs of read-out boards are the RICH-sub-detector at the Cleo-III experiment at Cornell CESR (US), the SVD-sub-detector at the Belle experiment at KEK-B (Japan), and the SCT-sub-detector at the ATLAS experiment at LHC (CERN). This will show the difference between systems with very different requirements in terms of speed, size, radiation levels, material radiation thickness and thermal transport.

The processing techniques used depend on the experiment. In Cleo-III a 4-layer PCB in FR4 was used. In this case the PCB has no function in the support of any critically aligned part. They are just plugged into the backside cathode plane of the RICH-cylinder.

For Belle two different versions were made. Both are based on an AlN substrate, which is a rigid ceramic with good thermal properties. The silicon sensors are attached to the hybrid and which is thus important in the mechanical stability and alignment of the sensors. A good heat conductivity is needed since several read-out chips are fitted in a small area. The first version had a 300 μm AlN substrate with one thin film gold layer on top. On top of this a 300 μm FR4 two-layer PCB was glued, with a polyimide film in between to ensure isolation where this is wanted. This is a rather fast and cheap way to make a multi layer module with much better mechanical and thermal properties than achievable with only FR4.

In ATLAS even more extreme solutions are required. Two approaches are tried, the first one is the baseline solution for ATLAS and is a thick film hybrid, where the substrate is a

BeO ceramic and the conducting and insulating layers are printed on top. The conductor is gold and the insulator is based on aluminum-oxide. Another solution tried as an RD is a flexible thin film hybrid based on conducting layers of aluminum and insulating layers of polyimide.

The test results of the produced boards for Cleo-RICH and Belle-SVD are presented, which show typical values and spreads in parameters for the front-end chips. A DSP based read-out system was used to test all 2200 boards delivered, and statistics on the first 1000 are given. The Belle-SVD boards were tested using the VA-DAQ system, and statistics on more than half the delivered boards are presented (120 5-chip boards). Results obtained by more or less finished CLEO-RICH and Belle-SVD detectors are also presented. Results from fully equipped (6 chip) BeO hybrid prototypes for ATLAS are given, as found in a paper presented at the 1997 IEEE Nuclear Science Symposium in Albuquerque.

1.6 Outline of thesis

The introductory remarks in the previous section summarize the subjects treated and the work done. Below follows an outline of how the following chapters are organized. Each chapter can be read as a separate part and has its own summarizing remarks. The last chapter, chapter 5, summarizes and concludes on the results obtained in this thesis.

- **Chapter 2** summarizes the VA-DAQ read-out and test system for VA-chips. Motivation for such a system, description of its usability and performance is given. The VA-DAQ system is now sold as a product of Integrated Detector & Electronics, the commercial vendor of the VA/TA/XA type of front-end chips.

- **Chapter 3** treats readout boards developed for Belle at KEK-B and Cleo-III at Cornell CESR, which are similar physics experiments. They are both B-factories with clean e^+e^- beams at the $\Lambda(4S)$ peak, but the boards are used in very different sub-detectors, a Ring Imaging Cherenkov detector in Cleo-III and a Silicon Vertex Detector in Belle. The choice of read-out chips and readout-boards are motivated from the difference in the signal generated in a MWPC and a silicon detector and the location of the sub-detector within the full detector. Instead of just listing results, a comparative study of the two experiments is done in some cases, since it usually better illustrates the choices made. Two examples can illustrate this already at this stage. The SVD is the innermost detector, and in order not to ruin the performance of other detectors it should have very little material to minimize Coulomb scattering. This is not so critical for the RICH, which sits further from the beam. In the RICH detector, where the charge signal for the input chips are taken from the cathode pads of a MWPC, the signal due to a charged particle crossing the gas is typically 20 times bigger than the signal generated in a pad due to converted photons from the Cerenkov light. This will require a very high dynamic range front-end chip for the RICH. In the SVD we are always interested in detecting just the position of charged

particles, which all have enough energy to give a signal in the 1 MIP range. A high dynamic range chip is therefore not necessary, and one can use a lower noise chip.

- **Chapter 4** concerns the ATLAS SCT, where the sub-detector is SCT, silicon barrels and disks using Si-strip sensors for tracking (a SVD). This is an experiment with an enormous increase in complexity due to the increase in speed, size and radiation levels. This requires new technologies for solving all problems. Several hybrid designs are presented, most of them based on BeO substrates, but also alternative thin film designs using aluminum/polyimide. Some results achieved with these hybrids (also assembled modules) are referred to. It is shown that the material budget can more or less be met with both technologies. The reason for doing RD on the aluminum/polyimide solution is the potential of even lower material, better thermal properties, and better electrical properties.

Chapter 2

A General read-out and test system based on VA/TA

A general low-cost PC-based system for test and read-out VA/TA front-end amplifiers was fully developed by the author during 1998. The complete hardware and an extensive collection of software routines, contained within the VA-DAQ program, were made within this short time span. The short turn-around time and its flexibility in use are mostly attributed to the choice of implementing the code in the graphical programming language LabView, a trade mark of National Instruments. Labview is today one of the most used tools for data acquisition and instrumentation for scientific and commercial applications.

The system has been highly successful and is today used for probe testing, verification and data sheet generation of all VA/TA chips of IDE. The flexibility of the system also allows it to be connected to any high ohmic capacitive (the signal being a charge) solid state detector that can be read out by VA/TA chips.

The success of the system is also demonstrated by being sold to over 20 research institutions, universities and major companies in the field of particle detection throughout the world.

2.1 Introduction to the VA/TA and the VA-DAQ

The VA-family of chips manufactured by Integrated Detector & Electronics AS (IDE) in Norway, contains more than 20 very low noise read out chips normally used as the front-end amplifiers for particle and photon sensors, such as silicon pad- and strip sensors and multi-wire proportional chambers. These sensors find their use both in high energy physics and medical imaging. Even though the VA series of chips are tailored for a variety of applications, as seen from their wide range of possible input charges, input capacitance and peaking times, they have all the same functional schematic. The chips typically have 128 or less parallel input charge sensitive amplifiers. The front-end is based on a pre-amplifier integrator followed by a shaper, both constructed from OTAs as described in chapter 1. Each channel facilitates a separate hold circuitry and the chip has a common

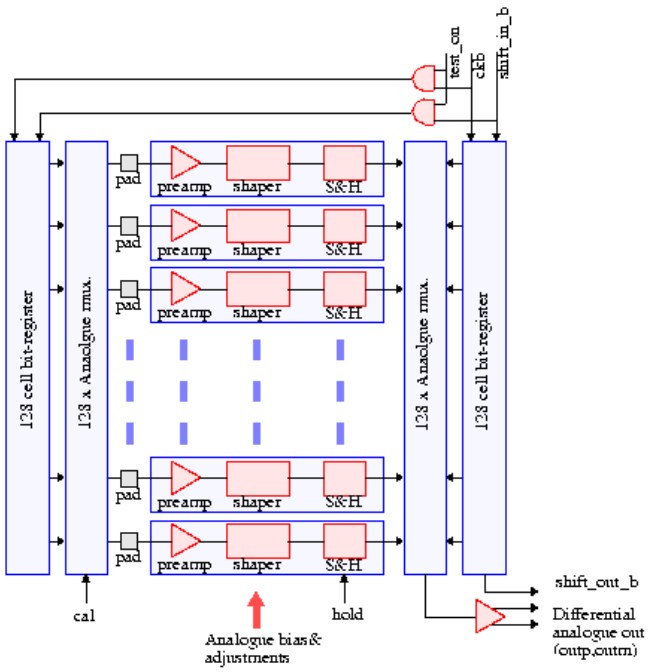


Figure 2.1: The working principle of a VA chip.

multiplexed analogue output. The principle of the chips is shown in figure 2.1, and the accompanying timing diagram in figure 2.2.

The read-out sequence starts with issuing a hold signal, which will open the sampling switches such that each channel holds the signal at the time the hold was issued. At the end of the previous read-out cycle a shift-in bit has been inserted in the chip. This means that the value of the first channel is already at the chip output and ready to be sampled. The chip is clocked and an ADC sampling performed, and this is repeated until all channels have been sampled.

All chips have the possibility to be fully checked on a channel to channel basis without having to connect to the actual input channels (or to a sensor), by using the calibration input mux to inject a charge into any specific channel.

The chip size, typically in the order of 5 mm by 5 mm, allows the sensor to have as low as 50 μm channel pitch. Table 2.1 summarizes parameters for two VA-chips, VA1 and VA-RICH, the chips used in the experiments discussed in chapter 3. Figure 2.3 shows the actual layouts of these two chips. The VA-RICH is a 64 channel chip for bonding to a board, whereas the VA1 is a 128 channel chip for direct bonding to a 50 μm strip detector.

The VA-DAQ system described in this chapter is intended to be used as a general test and read-out system for the whole family of VA-chips. Typical use is in probe testing for verification of chips before they are taken from the silicon wafer, or in testing of read-out hybrids, which typically feature from 2 to 10 chips on small printed circuit boards or thick film hybrids. Since the VA-family, as opposed to the XA-family of IDE, does not facilitate

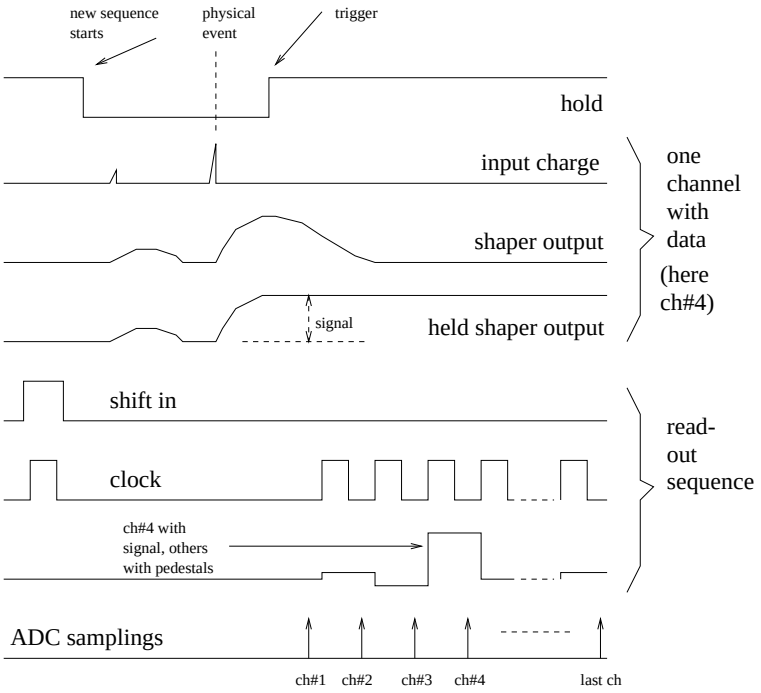


Figure 2.2: Channel response and readout sequencing of a VA chip.

Parameter	**VA-RICH**	VA1
Process	1.2 μm CMOS	1.2 μm CMOS
Size	5.2 mm by 4.5 mm	4.5 mm by 6.2 mm
Direct detector pitch	not applicable	50μm
Capacitive load	< 10 pF	< 100 pF
Noise	$100e^- + 15e^-/pF$	$165e^- + 6.1e^-/pF$
Typical gain	$\sim 8.3\,\mu A/fC$	$\sim 17.9 \pm 0.8\,\mu A/fC$
Gain range of chip	10% of mean chip gain	5.4% of mean chip gain
Pedestal range of chip	4.5% of full range	2.4% of range
Avg. chip ped. spread	$\sigma < 2.5\%$ of range	$\sigma < 0.8\%$ of range

Table 2.1: Summary of VA-RICH and VA1 parameters.

self-triggering, an external trigger is needed to use VA-DAQ as a read-out system. The VA-DAQ system can accept several types of external triggers. For instance a NIM trigger on a LEMO from a scintillator/photo-multiplier or from a TA-chip, the trigger chip of IDE. The TA-chip can not be used with any VA-chip, since it requires to be bonded to the output of the preamplifier of each VA channel.

The TA contains a very fast shaper (compared to the VA shaper), which is followed by a comparator. A common voltage threshold can be set for all channels. The output of all comparators are ORed together, to give a single trigger for the chip. The TA principle is shown in figure 2.4, and the timing diagram in figure 2.5. The fast TA trigger is, after a delay to match the typical VA peaking time, a suitable candidate for making a hold signal

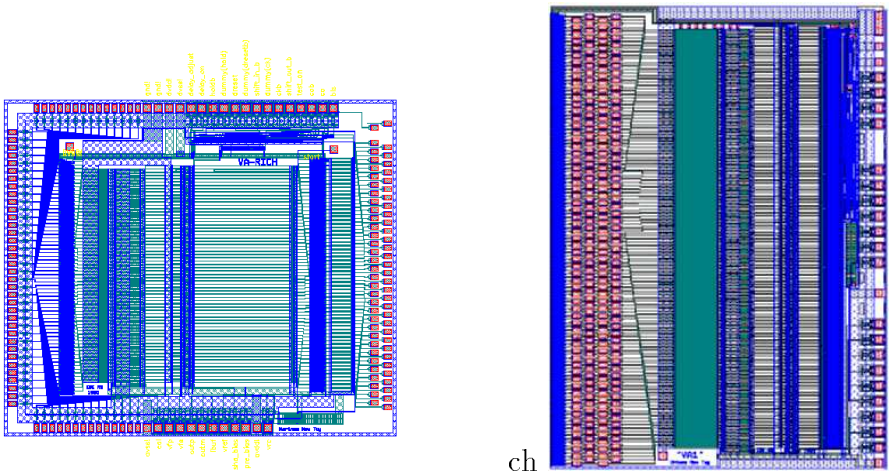


Figure 2.3: Layout of VA1 (right) and VA-RICH (left), their size being 6.2 mm by 4.5 mm and 5.2 mm by 4.5 mm, respectively. The chips shown in scale 10:1.

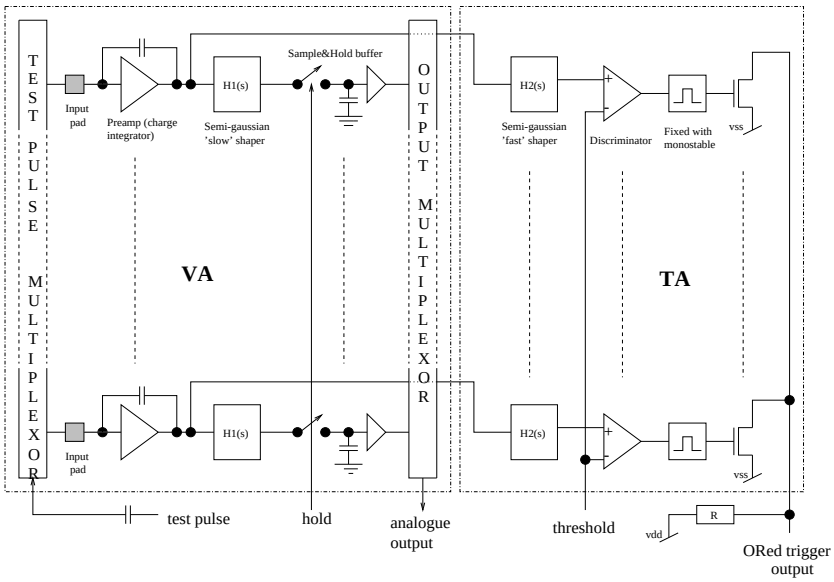


Figure 2.4: The working principle of a VA-TA combination.

for the VA. Only a very small time jitter is associated with the trigger for different input charges above the threshold, since the fast shaper has a very fast rise time.

The VA-DAQ was designed to minimize cost and equipment for the user. It is fully controlled with a PC through the parallel port, and the user interface is LabView, the present standard in data acquisition and instrumentation, which features easy graphical programming. The software, consisting of many high level VIs (short for Virtual Instrument), allows the user to measure all fundamental parameters of the chips, such as gain, pedestal and noise profiles. In addition exists a detailed description of the lower level routines, which makes it easy for the user to build his own high level VIs for measuring other

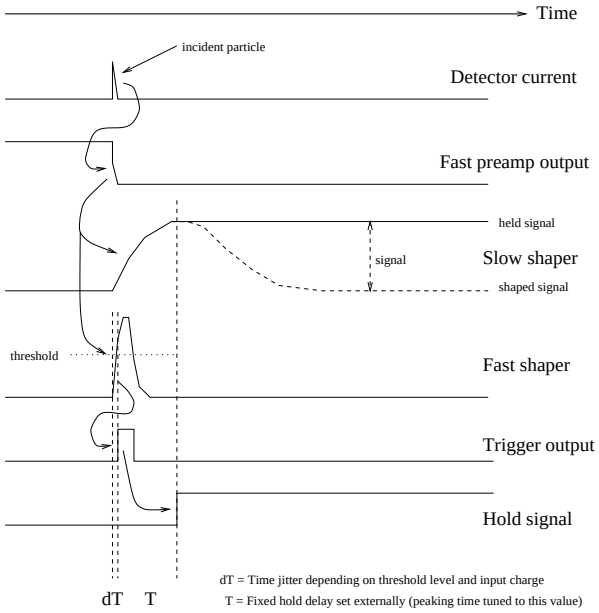


Figure 2.5: Timing diagram for a VA-TA front end.

interesting parameters or correlations.

The VA-DAQ system is fitted in a box of approximately 25 cm square and 10 cm height. The general VA-DAQ board is within this box plugged into a board that routes all necessary signals to a connector in the front of the box (The ADAPTER board). Two such ADAPTER boards currently exist, one that emulates the old VA repeater card output, and one recommended for new designs. Both definitions use a 50 pin ERNI connector for 50 mil flat cables. The new definition contains all signals needed for a VA-TA hybrid board. The user can have his own ADAPTER board designed, to interface to any preferred connector in the front plate of the VA-DAQ box. Figure 2.6 shows a picture of a VA-DAQ setup, consisting of the VA-DAQ, a PC and a lab-bench power supply. Figure 2.7 shows a picture of the inside of a VA-DAQ system, with the VA-DAQ board and an ADAPTER board visible.

This chapter will try to focus on the more general side of the VA-DAQ software and hardware. Most of the details are described in the appendix.

2.2 A short software description

The main program for controlling the VA-DAQ system, is the LabView VI (Virtual Instrument) called VADAQ.VI. This is a menu driven program from where a large selection of measurements on a VA/TA chip or hybrid can be launched. The most important VIs are:

- **Bias settings.** The VA-chip supplies and biasing can be set. Definition files can be read or written for the chip or hybrid under test, such that the system rapidly can be brought to a specific operating condition.

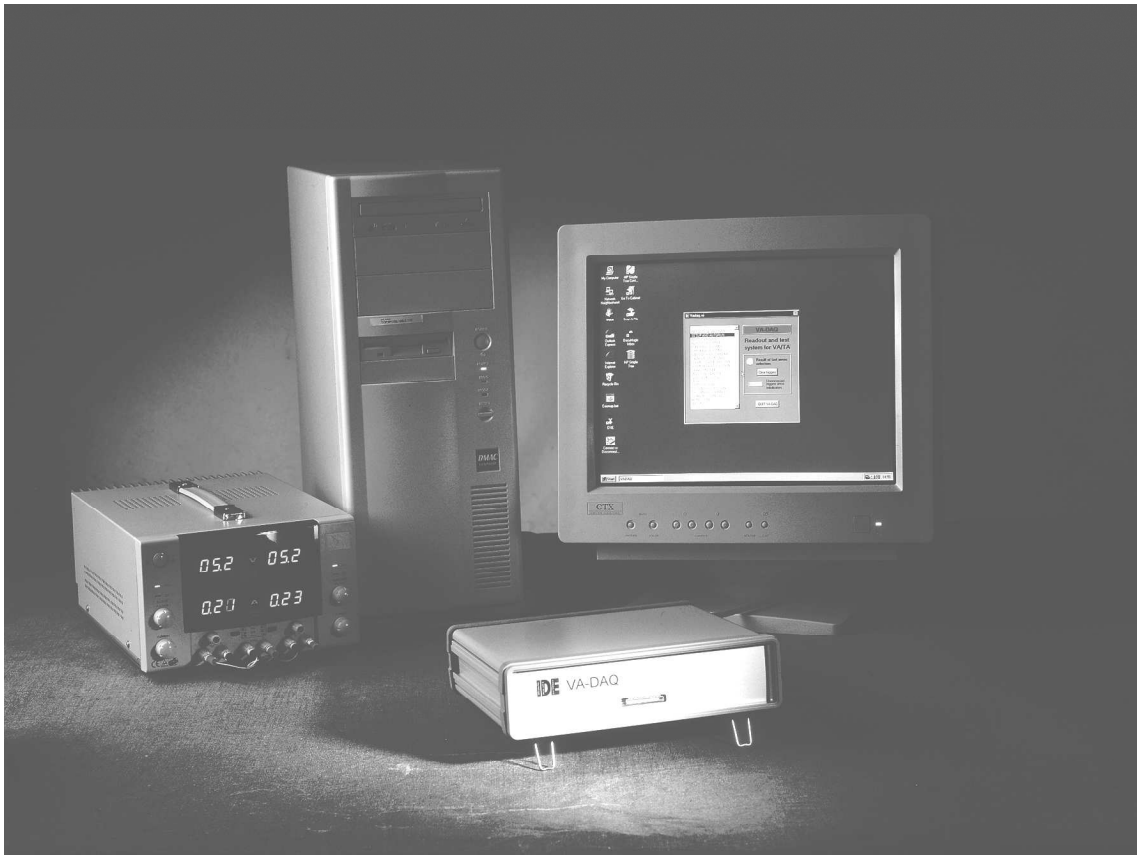


Figure 2.6: Picture of a VA-DAQ system, showing the VA-DAQ box, a PC and a lab-bench supply.

- **Oscilloscope.** The output wave-form from a VA chip subjected to a calibration pulse is shown continuously. The size of the calibration pulse, and biasing voltages and currents can be changed on the fly. This will help the user to find an appropriate pulse-shape response of the chip.

- **Pedestals and noise.** Measures the pedestal and the noise of all channels in a chip. This is done by using a standard read- out sequence, where a hold is issued to the chip and consecutive clocks and samplings of the VA chip output return the pedestal of all channels. The noise is calculated from the spread in the pedestal value of a channel over several read-out sequences. The noise is given after common mode subtraction on a chip basis, and also the common mode for each chip is shown.

- **Gain measurement.** Measures gain and pedestal of every channel in a chip. This is done by fitting the signal response curve (output voltage vs. input charge) for a channel to a n'th order polynomial. The gain is taken as the slope of the profile (and the pedestal as the value of the profile) at zero input charge.

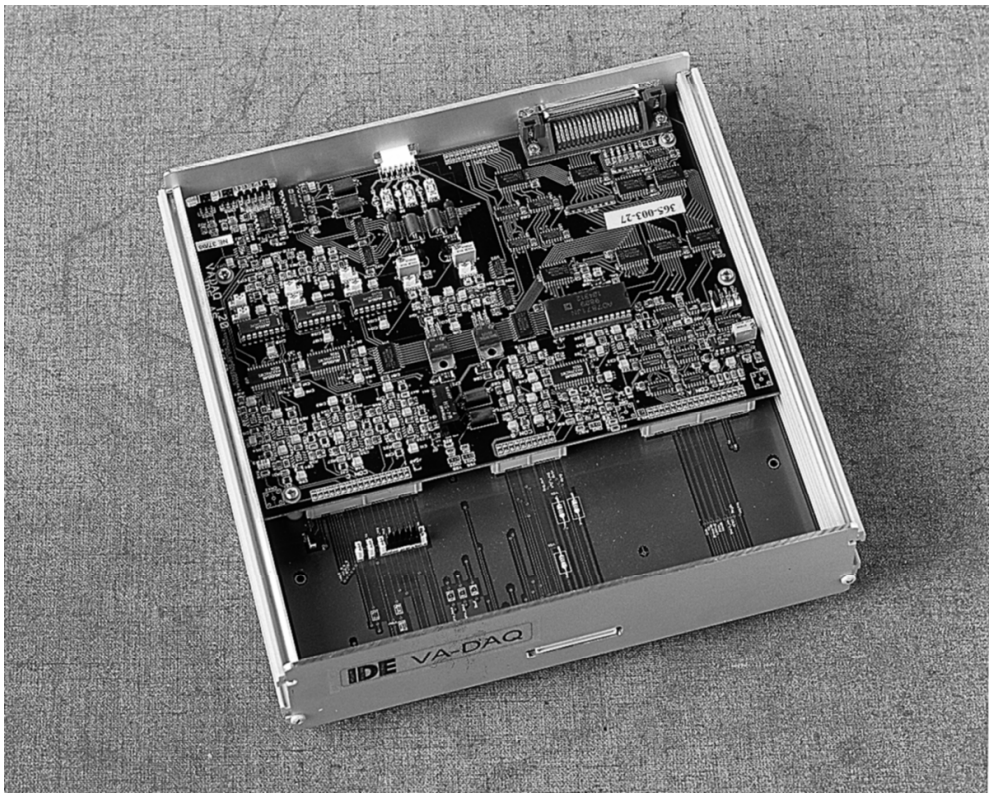


Figure 2.7: Picture of the inside of a VA-DAQ system. It shows the VA-DAQ PCB and an adapter board.

- **Peaking time measurement.** Measures the peaking time for each channel for a fixed input charge. The exact peaking time is found from fitting a polynomial to an averaged oscilloscope picture.

- **Signal profile.** Sweeps through the full range of calibrating pulses to make a signal profile for a channel. Should give an arc-tangent shape with plateaus for both extreme polarities of the calibration step. If these plateaus are not seen, the attenuation of the calibration step should be changed so that the calibration signal covers the full dynamic range of the VA chip under test. A routine similar to this is the core of the gain measurement.

- **Automatic data sheet generation.** Sweeps through a set of tests, defined by the user, resulting in a data sheet in ASCII format describing the results. Acceptance criteria can be set for all important parameters to mark channels as dead or alive. After a data sheet is defined the settings can be committed to a file for later use.

2.3 The use of VA amplifiers

The VA serial readout structure is a very simple scheme, but it has its limitations, compared to the more advanced chips of chapter 4. It can not be used in a dead-time free system, because when a trigger is issued the chip will hold the data from each channel until all channels are multiplexed out. This puts limitations on the readout rate. A system with 1024 channels using a readout clock of about 1 MHz will be busy and not accepting triggers (events/particles) for about 1 ms after the previous trigger.

A certain pre-amplifier/shaper stage can not be optimal for all ranges of input charges (dynamic range), input capacitive load and peaking times. The first decisions for a specific application will be to select a chip which more or less match the dynamic range and capacitive load presented by the detector.

The most important parameter for the system is the S/N-ratio, since this ultimately defines the resolution of the system. In an energy measurement (of photons) this decides the energy resolution, and in a silicon strip detector it will decide the optimal position resolution. To tune the front end will correspond to maximize S/N by scanning all adjustable front-end parameters. These parameters usually includes the current consumption and the feedback resistance in the pre-amp and shaper. The parameters will change the gain, peaking time, amount of undershoot and other features of the pre-amp/shaper output waveform. Unfortunately is this tuning often constrained. The two most typical constraints are the power consumption and the peaking time.

The power consumption is usually limited due to total power budgets, for instance in space applications, or due to limited cooling possibilities. The chip power consumption is almost totally determined by the current in the gain stages (transistors) of the pre-amp and shaper, thus constraining the tuning possibilities.

In a collider experiment the first important setting is peaking time, which is fixed. When a collision occur there will typically take in the order of $1 - 10\,\mu$s (a fixed time for each experiment) until we know if this was an interesting collision/event. When the trigger decision comes, typically based on calorimeters or muon spectrometers, the front end chip is told to hold the data. Since we want to sample at the peak of the pulse shape the chip should be optimized to have a peaking time equal to the trigger decision time. Trying to sample off the peak means including extra noise since any time jitter in the system will be mapped into a voltage jitter (noise).

When optimal settings are found for the S/N (measured as the ENC of each channel) other parameters can be measured for the chip. Typically the signal response of a chip is characterized by only two number, being the pedestal and the gain. The pedestal of a channel is defined as its value (DC value) at zero input charge. The gain is given as the slope of the signal response at zero input charge. Due to transistor variation the pedestal and gain are slightly different from channel to channel. In a typical application the user is interested in constraining the channel to channel variation. This is easily motivated by the fact that the serial readout necessarily means quantization of the data by a single ADC with a certain input range. A channel with pedestal or gain far off the typical values is more or less useless since its output does not map the ADC input range. If parameters

are close enough it will often be sufficient to represent the gains and pedestals of a chip with two single numbers (the average pedestal and the average gain), greatly reducing the calculations needed in the later data analysis. It can even facilitate more of the analysis on a DSP close to the front end, reducing the data files dumped to disk for later analysis. For some applications also linearity plays a role. The channel output should be linear for a certain input charge range.

This was a general description on characterizing CSA chips, which motivates the existing measurements available within the VA-DAQ software.

2.4 Overview of chip measurements

The VA-DAQ system front panel is shown in figure 2.8. It is a menu driven program where the required operation can be selected from the menu list on the left hand side. The operations can be divided into four classes. The first menu items are for setting up the system, the next group of items for measuring VA parameters, the third group for measuring TA parameters and the last group for doing detector readout. The detector readout options are for single channel readout or full system readout. The chip supplies and their current draw are shown on the front panel. The supplies are automatically turned off if a defined current limit is passed.

2.5 Setting up the VA-DAQ system

Three menu items exist for setting up the system, **Initialize & Calibrate**, **VA-DAQ setup**, and **Swap VA Chip/Board**.

2.5.1 Startup of system

When the VA-DAQ system is first started one need to initialize it with the menu item **Initialize & Calibrate**. The system will go through a self test and also calibrate some parameters. Each self test will either give a red or green LED depending on the success. All LEDS should be green for the system to perform properly.

It is not necessary to run this item more than once unless the lab-bench supply for the VA-DAQ or the PC is turned on or off. The system can query for an initialization file during this phase, and the VADAQ.INI file needs to be specified. The file contains the parameters specific for the VA-DAQ system used. If this file is found in the correct directory it will not be queried.

2.5.2 Setting up for VA-TA testing

After the initialization of VA-DAQ one should set up the system for testing a specific VA-TA-board, by the **VA-DAQ Setup** menu item. Figure 2.9 shows the setup window,

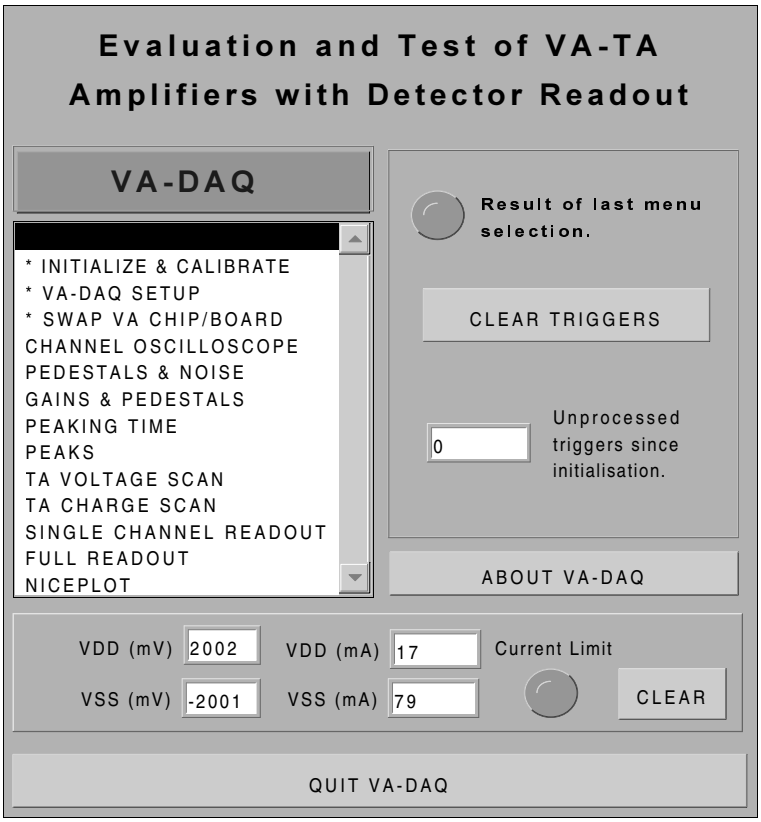


Figure 2.8: Front panel of the VA-DAQ software.

which presents the user with several options. The menu items on the left could more or less be run in the listed order from top to bottom to setup the system.

The first menu item, **Calibrate VA Current**, is used to calibrate the current used by the VA chip/board under test. This calibration is needed since also the VA-DAQ board itself has units powered by the same supply as the VA-chips. The currents used by these units should be subtracted in order to get the correct current draw by the chips.

All parameters for putting the VA-DAQ in a specific state for testing a certain VA-board can be put in a file, called a definition file. This file can be retrieved by choosing the menu item, **Read definition file**. When the file has been read the right side of the setup window will show the general parameters given by the file, such as the chip type under test, how many chips on the tested boards and so on. However, the most important parameters are the values of all voltage and current biases and the values of the chip supplies. These can be popped up by selecting the **Setup biasing** item in the setup frame. Here the values of all biases as read from the definition file are listed, and they can be changed. The menu item **Use current bias settings** is very useful. It will take the values currently in the system and fill them in as default values in the tables. For each bias and supply an offset value can be set. If a bias is further from the default value than the offset indicates it is regarded as an error.

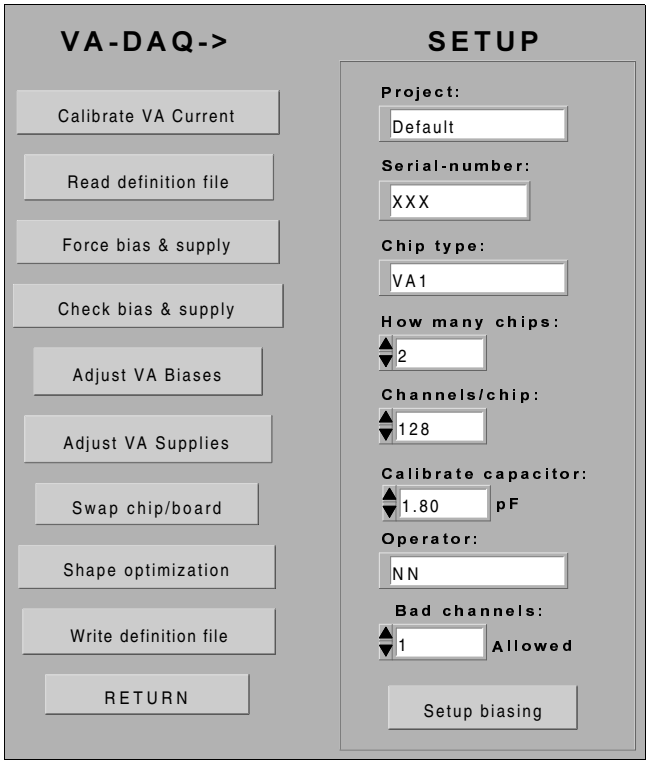


Figure 2.9: The Setup menu of the VA-DAQ system.

After the definition file has been read the system will not apply the values from the file before it is ordered by the user. This is done with the **Force bias & supply** menu item. The result of the forcing will be listed and error messages given if it was not possible to set a bias to a value closer than the offset value indicates. Errors can be caused by chip problems or by the board under test. At later stages it can be interesting to check whether biases and supplies are within the default values set, this can be done by the **Check bias & supply** menu item.

Several of the VI's in the main menu can change the setup, for instance can the **Oscilloscope** change specific bias values. As long as the new value has not been set to default value by selecting **Use current bias settings**, they will be reset to default by using for instance the **Force bias & Supply**. After playing around with a new board and one is satisfied with all settings, one should push **Use current bias settings** and write a new definition file, using the **Write definition file** menu item.

If one for some reason would like to change a bias or a supply to a new value it can be done by the buttons **Adjust VA biases** and **Adjust VA supplies**. The first one list all bias values of the system in a window, as seen in figure 2.10 for a five chip VA2 hybrid. The user can change a specific bias or force all biases to the values given by the definition, similar to the force program. The user can set the VA chip supplies in the range $1.7 - 2.4\,\mathrm{V}$ for the positive supply and the equivalent negative range for the negative supply. The values for the currents listed will only be the actual VA chip currents as long

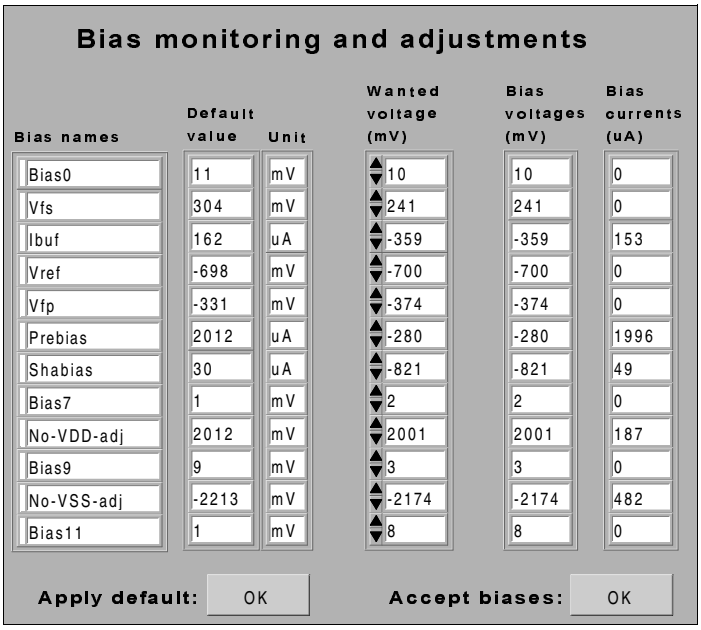


Figure 2.10: VA-DAQ panel for setting VA bias values.

as the **Calibrate VA current** has been performed.

Hot swapping of a chip/board under test is vital to speed up testing. This is done by the **Swap chip/board** button. It will put all supplies, biases and digital lines for the VA chips to ground level. When finished, a re-calibration of the test charge is performed. This is easily motivated, since the injected test charge depends on the actual terminating resistor on the board under test. The attenuation of the of the test charge also includes some jumpers in the back plate of the VA-DAQ system. If these jumpers have been moved, **Swap chip/board** must be run to re-calibrate. In this case the board does not have to be disconnected.

The last button in the setup menu is called **Shape optimization**. There exist two possible options, one to scan any bias to find an optimal peaking time and a second to scan any bias to find the ENC and the gain (usually to locate the lowest possible noise). These are described below.

Peaking time as a function of biasing

It is sometimes interesting to work with bias values not at nominal settings, for instance to re-tune for another peaking time that better match the application. For instance in a collider experiment the hold time (peaking time) of the chip needs to be set to the first level trigger delay.

In order to find such a setting it is interesting to scan for instance one of the biases, with the others still at nominal value, to see the effect on the peaking time and signal height. This is exactly what this menu item can perform.

For the shape of the VA pulse, the most interesting parameters to scan are the shabias and the vfs. The first controls the amount of current floating in the shaper OTA. Lowering the current will lower the band-with of the OTA, thus increasing the peaking time. The vfs voltage controls the feedback resistance in the shaper, and thus the RC time-constant and the pulse shape.

ENC as a function of biasing

This VI allows the user to scan one of the biases and see the effect it has on the ENC and gain. Both ENC and gain are defined as the average over all channels. It is important to note that the test is performed at a fixed hold delay. This is a very important optimization, since the ENC is the single most important parameter of a system.

In order to achieve good noise performance it is important that vfp is as low as possible. This voltage controls the feedback resistance of the front-end OTA. Since this OTA should operate as an integrator, the resistance should be as high as possible. If it becomes to high, nothing will stabilize the DC point of the integrator and the signal response will die. By scanning vfp one can find the voltage knee where the channel dies. To have good noise performance one should select a vfp value $50 - 100\,\mathrm{mV}$ above this point.

An alternative way to find a good vfp value will be to alter vfp in the **Oscilloscope** and look for the vfp point where the signal response dies out, and in a similar way select a vfp value $50 - 100\,\mathrm{mV}$ above.

2.6 VA measurements

The menu items corresponding to VA measurements are the **Channel oscilloscope**, **Pedestals & noise**, **Gains & pedestals**, **Peaking time** and **Peaks**. The oscilloscope looks only at a single channel, while the other measure some parameter for all channels.

2.6.1 VA signal waveform

The VI allows the user to look at a running oscilloscope picture of an user selected channel, by selecting the **Oscilloscope** from the main menu. The front panel is shown in figure 2.11.

It is possible to select the time window (typically $-1\,\mu\mathrm{s}$ to $30\,\mu\mathrm{s}$) with respect to the time of charge injection to the chip, and it is also possible to select the input charge in fC. The waveform is not the response to a single charge injection, but rather each point on the waveform is found from a separate charge injection. The full waveform is therefore found by scanning the sampling time over the selected time window, sampling at each time-step with a charge injected. The scan interval (time resolution of waveform) is in the order of 250 ns if the **COARSE** button is set, which is good enough for typical VA waveforms with $2\,\mu\mathrm{s}$ peaking and tails reaching to about $10\,\mu\mathrm{s}$. If the time resolution is set to **FINE**, it is in the order of 25 ns and a maximum time window of about $2.5\,\mu\mathrm{s}$. It can be used to look

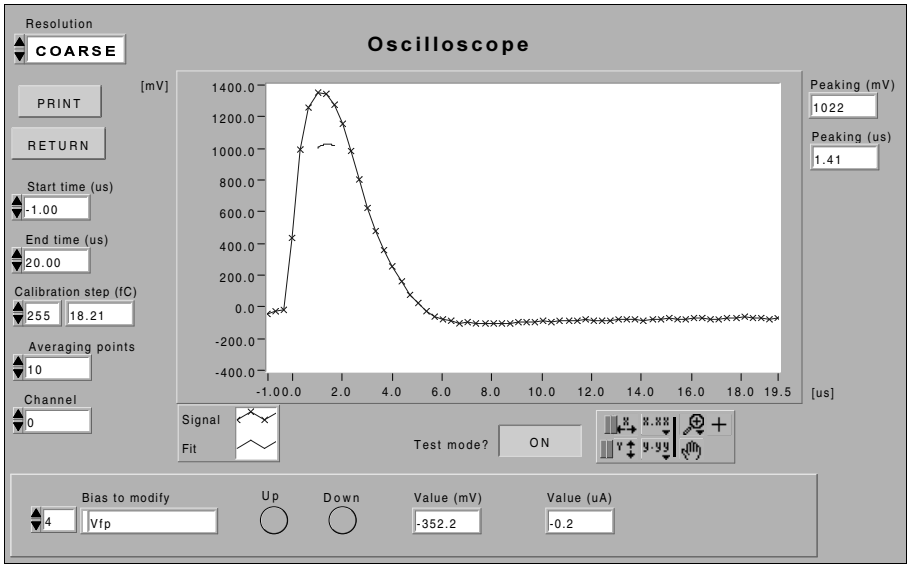


Figure 2.11: VA-DAQ oscilloscope showing a typical VA channel response.

at details of the rising edge of VA pulses and to look at waveforms for fast VA chips with peaking times from $75 - 500$ ns.

If the user zooms in on the peak by selecting a suitable start and end time, the values on the right side of the screen will indicate the correct peaking time and peak value.

In the lower end of the panel it is possible to adjust any of the chip biases so that an optimum shape can be found.

2.6.2 Measuring offsets and their deviation

The VI **Pedestals & noise** performs a full read-out sequence a certain number of times (runs) indicated by the user. The pedestal (offset) of a channel is taken as its average value over the runs. The raw noise of a channel is defined as the standard deviation of the samples for this channel. For each readout sequence and for each chip a quantity called common mode can be defined, being the average of all pedestals for that chip for that specific readout cycle. The common mode can be subtracted from the raw pedestal data, giving the common mode subtracted pedestals. The channel noise is calculated from the common mode subtracted data, as opposed to the raw channel noise. The standard deviation on the set of common mode values for a chip over all runs is defined as the common mode noise of the chip, also listed on the front panel.

In the case of a Gaussian distributed channel noise and a Gaussian distributed common mode noise, it is easily shown that the total channel noise is the root square sum of the common mode subtracted channel noise and the common mode noise. This result is proved on a general basis in the appendix, as equation B.15.

Figure 2.12 shows the front panel of this VI, with data for a 5-chip VA2 hybrid. Both the noise and the pedestals are listed as voltage levels into the ADC.

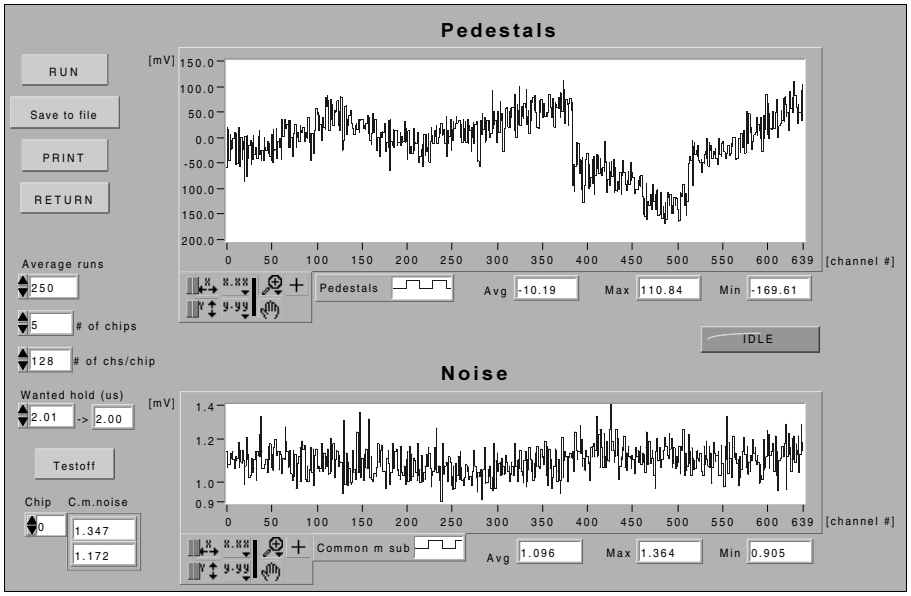


Figure 2.12: VA-DAQ front panel for measuring pedestals and noise.

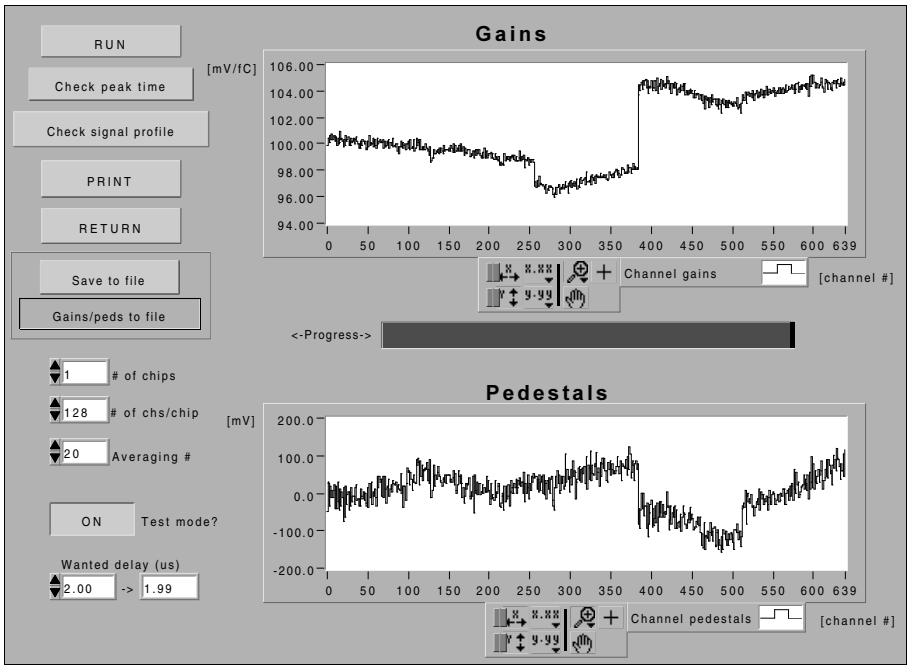


Figure 2.13: VA-DAQ front panel for measuring gains and pedestals.

2.6.3 Gain measurements

The menu item **Gains & pedestals** will measure the gain and pedestal of all channels, its window being shown in figure 2.13. The shown plot is for a 5-chip VA2 hybrid, and it is clearly visible that the 5 chips have slightly different gain.

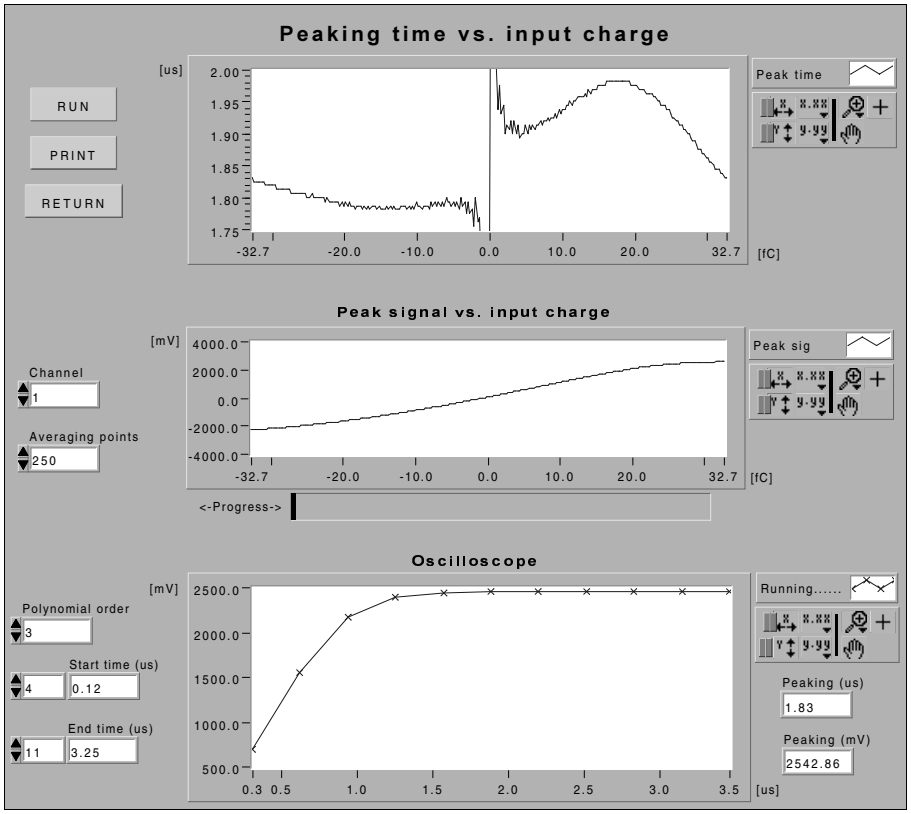


Figure 2.14: Variation of peaking time as a function of input charge for a VA channel.

In order to achieve a correct result, two single channel tests should be run. These have their own buttons on the front panel called **Check peak time** and **Check signal profile**.

It is important that the user has found a suitable hold time, such that the signal response is sampled at the peak. This can be found by the **Check peak time**. The injected charge will be scanned in the currently set charge range. For each charge point the peaking time and signal height (not subtracting the pedestal) are measured. Two plots are presented, one is the peaking time as function of input charge, the other the signal height as function of input charge. This is shown in figure 2.14.

When a VA chip is used in a real read-out the hold time (peaking time) is fixed and it is therefore important that the peaking time does not change much with the input charge. In the ideal case where the signal response is proportional to $Qt\exp(-t/\tau)$, with Q the input charge and τ the peaking time, the peaking time should be independent of the input charge. An acceptable spread is about ± 200 ns. This will still give sampling more or less on the flat part of the peak. If the shape is assumed as above a calculation give that the signal height is still 99.5% at time $t = 1.8\,\mu$s and $t = 2.2\,\mu$s, for a peaking time of $2.0\,\mu$s. Figure 2.14 shows that for positive input charge is the peaking time in the range $1.8-2.0\,\mu$s for the scanned charge range, and for negative charge a bit flatter, more like $1.75-1.85\,\mu$s. A peaking time matching the typical input charge of the experiment should be used. This

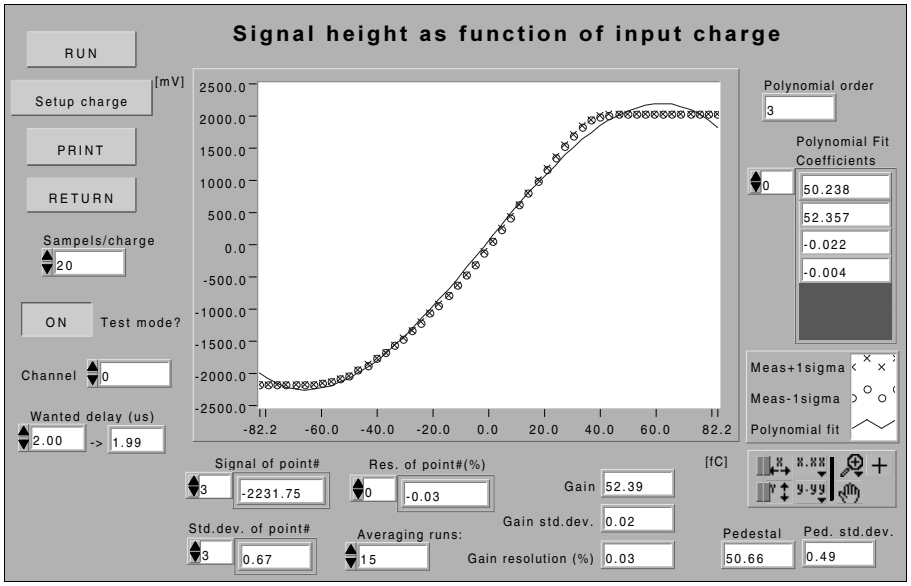


Figure 2.15: Signal profile for a channel in a TA1 chip.

spread over input charge can be compared to the cannel-to-channel spread found by the main menu item **Peaking time** described later.

Check Signal profile will scan a desired range of input charges (fC) and measure the chip output signal (mV) at a desired hold time. The values are plotted with the input charge along the x-axis and the chip response along the y-axis. The plot is fitted to a polynomial, and the gain of the chip (mV/fC) is defined to be the slope (first order coefficient) of the fit at zero input charge, whereas the pedestal (offset, the channels DC value) is defined as the output signal value at zero input charge (zero order coefficient of the fit). The signal profile is obtained several times for the same channel to get statistics on the accuracy of the gain measurement (%). If the accuracy is not good enough, either the averaging or the number of charge points along the x-axis can be increased. Figure 2.15 shows a typical front panel. The typical signal response is an arcus tangent shape, which is easily fitted to a polynomial as long as the flat plateaus are not included in the fit. The shown plot has defined a too big charge range and the third order polynomial has problems with the plateaus at large input charges. In this case the input range should be limited to a smaller range to get a good fit.

If the two VIs **Pedestals & noise** and **Gains & Pedestals** have been run, the last main menu item, **Niceplot**, can be run. It will present the gain, pedestals and noise for all channels in three plots, with accompanying histograms. This is the VI best suited for printing the important chip parameters. Figure 2.16 shows the plot produced for a five chip VA2 hybrid after it has been optimized for minimum noise, with the constraint that the peaking time should be $2\,\mu$s. Average channel noise is $64\,e^-$, when the system noise is subtracted, to be compared to $60\,e^-$, the lowest possible noise for a single chip according to the VA2 data sheet.

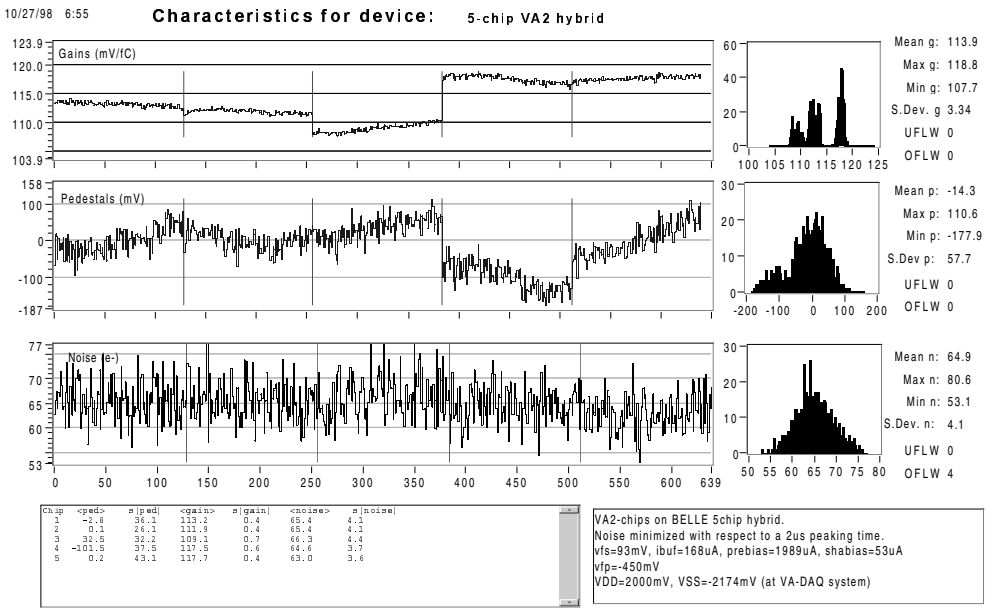


Figure 2.16: Showing channel pedestal, gain and noise for a 5 chip VA2 hybrid. All 640 channels are fully functional.

2.6.4 Peaking time measurements

The menu item **Peaking time** will check the peaking time of all channels. Each channel is pulsed with the same input charge, selectable by the user, and the signal waveform for a certain time range around the peak is obtained. A polynomial fit is done to obtain the peaking time of each channel, which is plotted. Figure 2.17 shows the front panel.

2.6.5 Peak measurements

The **Peaks** menu item can be used to check the full dynamic range of all channels in a VA chip. Two input test charges can be defined for injection to the chip under test. Typically one selects a big negative charge and a big positive charge. The signal height for each of these two for all channels is shown in two plots. This can be used to check the full dynamic range of the channel, since the gain measurement itself usually only selects a more or less linear part of the arcus tangent shaped total channel response. If the two input charges are selected to be on the two plateaus of the arcus tangent shape, the difference between the two plots is the full output range of the channels.

2.7 TA measurements

The interesting feature to measure for a TA chip is the channel-to-channel variation of the charge needed to have the channel trigger, once a specific threshold voltage is applied to

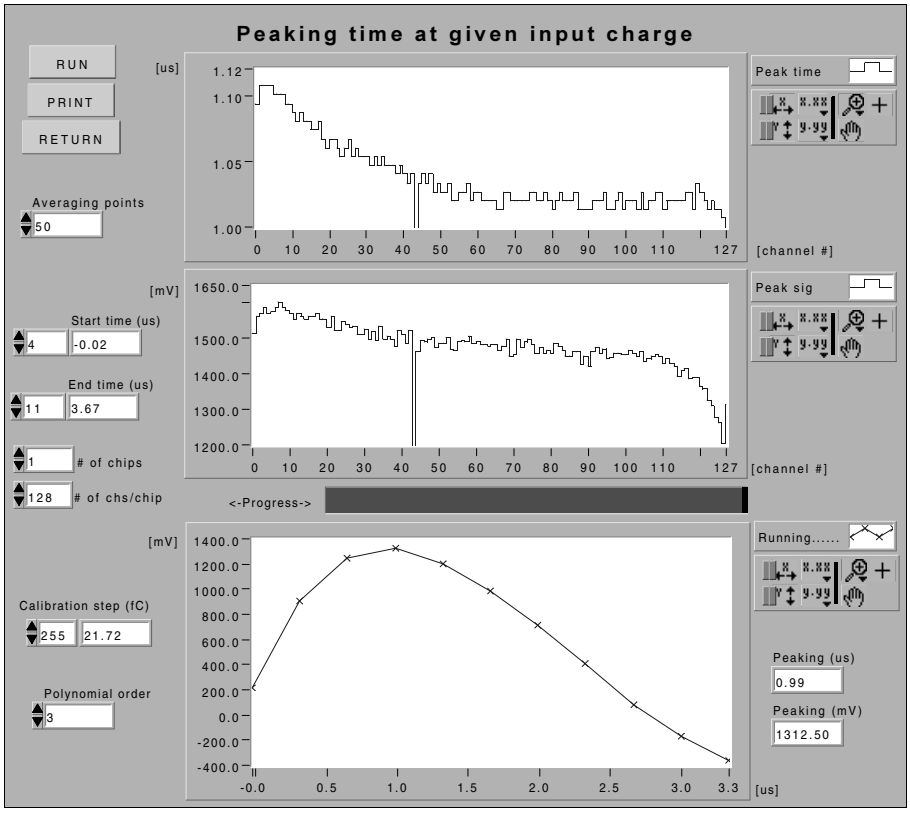


Figure 2.17: Peaking time of all 128 channels of a TA1 chip. The peaking time is in the range 1.0 to 1.1 μs. Channel 43 is a dead channel.

(the comparator inputs of) the TA. The spread should be small to ensure that particles (for instance photons) have the same absolute energy threshold regardless of what channel the particle should hit. The VI **TA charge scan** will measure the trigger charge for each channel for a specific threshold voltage.

In addition it is interesting to look at the linearity of each channel. This is done with the **TA voltage scan** which is a single channel measurement. Both menu items are described below.

2.7.1 Threshold charge vs. voltage

Figure 2.18 belonging to the menu item **TA voltage scan** shows a scan for a single channel of a TA1 chip. We see that the trigger charge in the threshold voltage range of $15 - 50$ mV is linear. For the specific channel a TA threshold of about 40 mV is needed to set the trigger level to 3.6 fC, which is a signal of a MIP in 300 μm of silicon. This VI is typically used to check the linearity of the charge trigger level versus the set voltage threshold, and to have a feeling for what threshold voltage to set to obtain a certain trigger charge level.

When this VI is run only the specific channel under test is enabled to trigger. This is

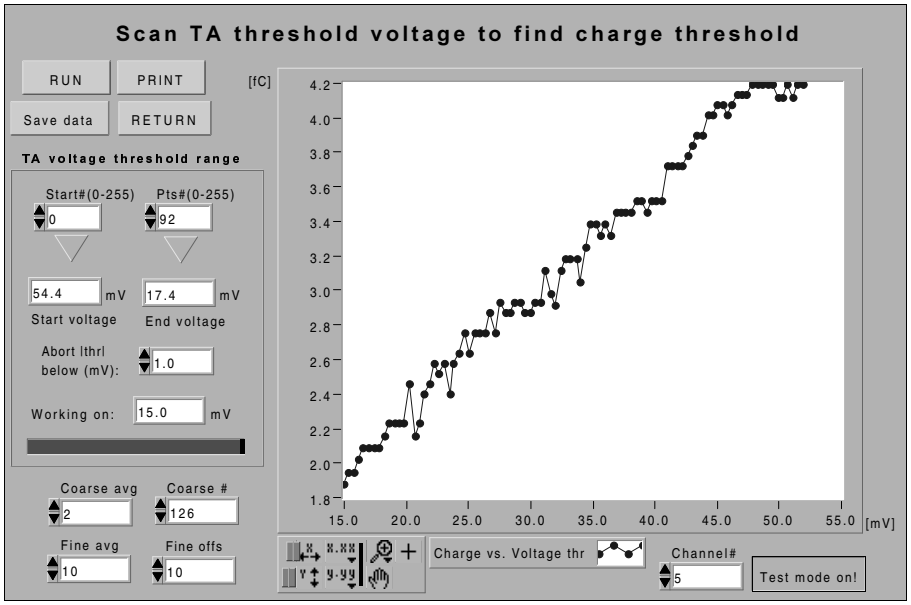


Figure 2.18: Trigger charge level as a function of TA threshold for one channel of a TA chip.

done by down-loading a mask to the TA where only one channel is set to trigger.

2.7.2 Trigger charge level

The **TA charge scan** will for all channels find the necessary injected charge to trigger the chip. This is done at a fixed TA threshold voltage. Figure 2.19 shows this plot for a TA1 chip. It shows that for a set threshold of 53 mV the trigger charge needed is in the range $2.9 - 3.8$ fC for all channels except for channel 43, which is dead. The charge range to scan, from 1 to 7 fC in plot 2.19, should be selected to be a wide charge range around the expected average trigger charge, which here is 3.4 fC.

Two other interesting buttons exist. One is the **Set threshold** button, which allows one to set the TA threshold voltage. The other is the **Single channel** button, used to perform a more detailed test of a single channel. It is this single channel test that helps the user to select a good charge range to scan, and the use of this test is described below.

Single channel trigger level

This VI operates on a rather low level, offering several possibilities of experimenting with the TA trigger for a specific channel. The window associated with this test is shown in figure 2.20. Three buttons on the left will allow the user to define a certain input charge range to scan, **Set charge**, a TA threshold voltage **Threshold** and to define the TA mask, **Manual mask**.

The **Manual mask** allows one to enable certain channels for triggering. Typically you

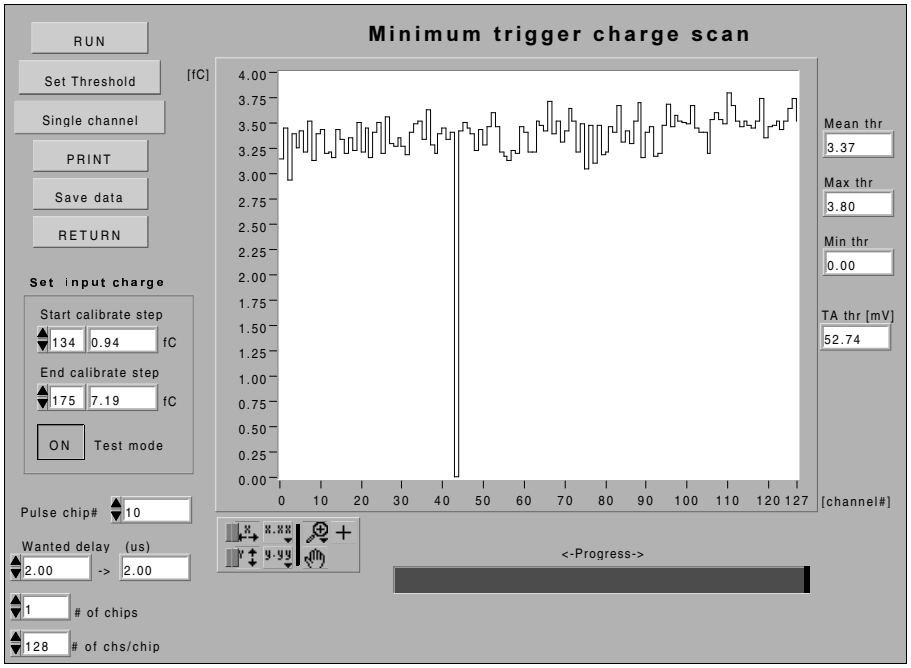


Figure 2.19: Trigger charge level at a given threshold for all channels of a TA1 chip.

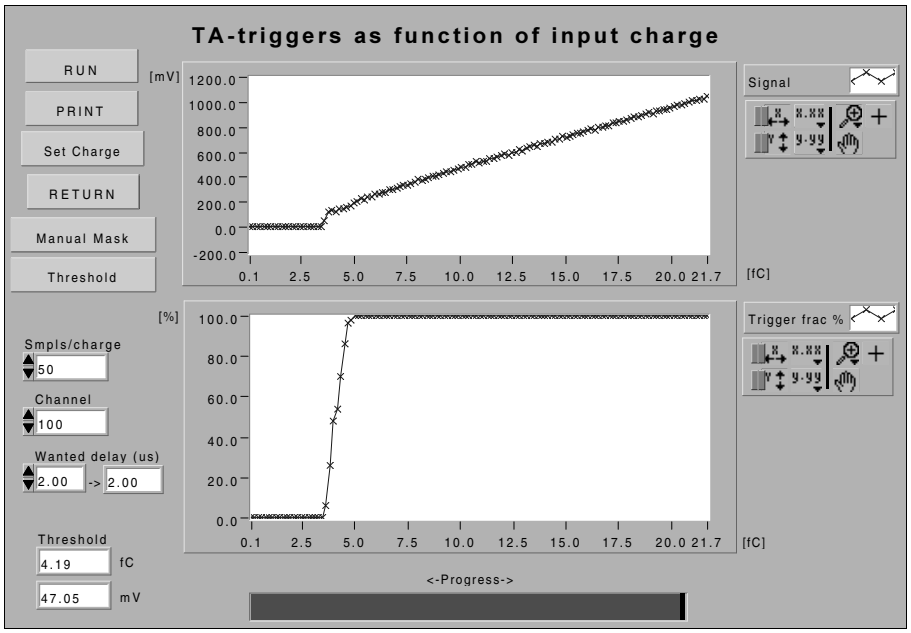


Figure 2.20: Trigger probability of a given channel as a function of the input charge.

should only enable the channel you want to test. It is also possible to select what polarity you want the chip to trigger on. This polarity is by default set to positive if the present TA threshold voltage is positive, and to negative if the voltage is negative.

When the VI is run it will for each charge in the selected range pulse the VA-TA board a certain number of times, given by the parameter 'Smpls/charge'. The VA-DAQ system will count how many of these pulses that actually gave a TA trigger in response, to build the lower plot that shows the trigger fraction in percent for the scanned charge range. The trigger charge associated with the set TA voltage is given by the x-axis charge at the point where the trigger probability crosses 50%. Figure 2.20 (lower left) shows the trigger charge to be 4.2 fC at a TA voltage threshold of 47 mV. The observed plot should be that of an error function, width the sharpness of crossing from 0 to 100% trigger efficiency giving the noise of the trigger channel.

A feature of the TA chip should here be mentioned. If the charge range is selected including both polarities one can often see that triggers are returned for the 'wrong' polarity as long as the charge is big enough. This only implies that the fast shaped TA pulse into the comparator has a small undershoot and then an overshoot, which, when the total charge injected is large, can create a comparator trigger.

2.8 VA-DAQ as a readout system

The last group of menu items is for using the VA-DAQ system as a read-out system. Two menu items, **Single channel readout** and **Full readout** exist. The first one is typically used to get a high rate system, in the order of 10k events per second. A single channel readout can not give results as good as reading out the full system. This is due to the fact that the common mode noise cannot be removed without reading out several channels. The full channel readout will give a maximum readout rate of about 32 kHz/channel on a typical equipped 1998 PC running Windows-95. This amount to about 250 events/s for a 128-channel readout system.

Both readout possibilities are otherwise very similar, and only full readout will be described here. The front panel for **Full readout** is shown in figure 2.21. It should be stressed that the data presented on the screen always will be raw data before any pedestal and common mode analysis have been performed.

The collection of data is divided into data collection cycles. The first part of setting up this VI will be to select the acquisition time for each cycle, and also the maximum numbers of events allowed in each cycle, in the shown plot these are 1000 ms and 1000 events, respectively. The last requirement is necessary to minimize the amount of RAM used by the arrays. If the arrays become too big, the PC will have to do swapping of data between RAM and disk, which will slow down the data collection. Acquisition times should maximum be half an hour. Another reason to divide the acquisition into cycles is to reduce time used to update the screen. The screen is only updated at the end of each cycle.

The second part of the setup will be to define the number of data collection cycles to be started when the **RUN** button is pushed, in the shown plot this is 100 cycles. A run can be stopped before all cycles are completed by pressing the **STOP** button. The **RETURN** button will return to the main VA-DAQ panel. The actual plot also shows

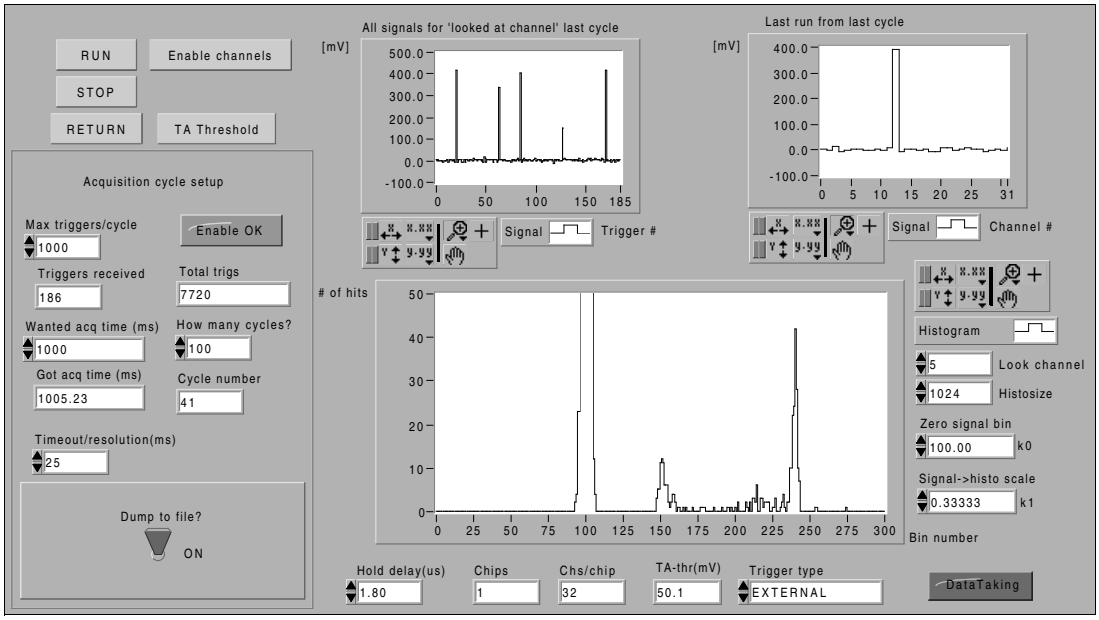


Figure 2.21: Full readout of a system including a detector. Allows raw data dumping to file for later analysis.

that dumping of raw data to file is enabled, meaning that a file with raw data collected is written at the end of each cycle. The actual file dumping can be disabled, typically done under the evaluation phase of a new setup, and in this case the number of cycles is set to a large number, such that one does not need to constantly start acquisition with the **RUN** button. The acquisition time should be set short so that the screen is often updated. For data taking to file, longer acquisition time for each cycle is better, reducing the time used to update the screen and other unnecessary tasks.

The data files contains raw 16-bit signed ADC values for each channel from each event. There are no markers in between each event, so the file contains $N_{events} \cdot N_{channels}$ signed 16 bit integers. An index file will be written to the same directory as the raw data files, showing the time the cycle was started and the amount of events in each data file.

Three graphs on the panel allows the user to have a visualized picture of the continuous data collection. The upper left one shows all values in a specific channel (here channel number 5) for all events of the last acquisition cycle. This shows a rather flat plot with 6 spikes. These spikes are the times when the trigger was associated with this specific channel and are thus real signals. Most of the time it is however some of the other channels that trigger and we see just the pedestal value in this channel. The pedestal is seen to be just above 0 mV, while the largest signals are around 400 mV.

The upper right graph shows the last event of the 186 events of the last cycle. We see that clearly channel 12 has a big signal and must have been the channel that gave a trigger for this event. The signal is around 400 mV. For the other channels that did not trigger we only see the pedestal value.

The last graph is a histogram for one of the channel, here number 5. This histogram accumulates data from all cycles since the run started. On the left it is seen that this histogram contains data from 41 cycles (the run will continue to 100) and so far there are 7720 entries in this histogram. The data sample from each event is scaled by the constant 'Signal $\rightarrow$ histoscale' and offsetted such that zero value ends up in bin number 'Zero signal bin'. The by far biggest peak is seen around bin 100, being all the events for channel 5 when it was not the triggering channel. The peak is therefore indicating the pedestal value of this channel. The peak around bin 238 is however associated with the Am-source used. One clearly see that the threshold voltage is set such that signals corresponding to lower than bin 145 will not trigger the TA. The width of the pedestal peak in the histogram can be used to define the raw channel noise before any common-mode subtraction routines have been used. It should be stressed that the histogram is not written to file, only the raw ADC data is written.

The user can write their own program to analyze the raw data files. Additional programs, not integrated into the VA-DAQ software, exist to analyze such raw data files. It will read in the data files, do pedestal and common mode subtraction on the data, and build histograms for each channel. Various cuts on the quality of each event can be set, and also the histogram size can be altered. Scaling and offset coefficients map the raw ADC values into a specific histogram bin. Measurements can be performed on the energy histograms, for instance to measure the energy resolution (%) of peaks in the spectrum. The figure 2.22 shows the result of a very simple analysis program used on data collected by a 32 channel VA-TA system connected to a silicon pad detector. The sensor was radiated with an ^{241}Am source, which radiate 59.5 keV photons. The VA-TA system was confined in an aluminum box and the sensor radiated through a window from the top. The figure shows the energy spectrum for one of the channels, and the Am-peak is easily located around bin 515. Bin 100 in the histogram refers to 0 keV, and again shows a peak due to the pedestals. The width of the pedestal peak gives the noise in a channel after common mode subtraction since the analysis do common mode subtraction. The plot in the lower right corner of the figure reveals the energy resolution of the Am-peak and it is seen to be in the order of 2.8% FWHM for most channels.

In figure 2.23 the spectrum for one of the channels is shown. The pedestal peak has been removed and the x-axis scaled to show the energy in keV. The energy resolution of the Am-241 peak is about 2.8%. The threshold for this channel of the TA chip is around 20 keV. Closely below the sensor the bottom of the aluminum box will give rise to some back-scattered photons. Figure 1.6 shows the most probable recoil electron energy of about 11.4 keV, which is also the maximum allowable energy, giving back scattered photons with a peak at about 48 keV. This is seen in the spectrum.

2.9 A description of the hardware

The VA-DAQ system contains 5 functional hardware units. These are referred to as PARIO, SUPPLY, ADC, PULSE and BIAS, each described below. The VA-DAQ is a bus based

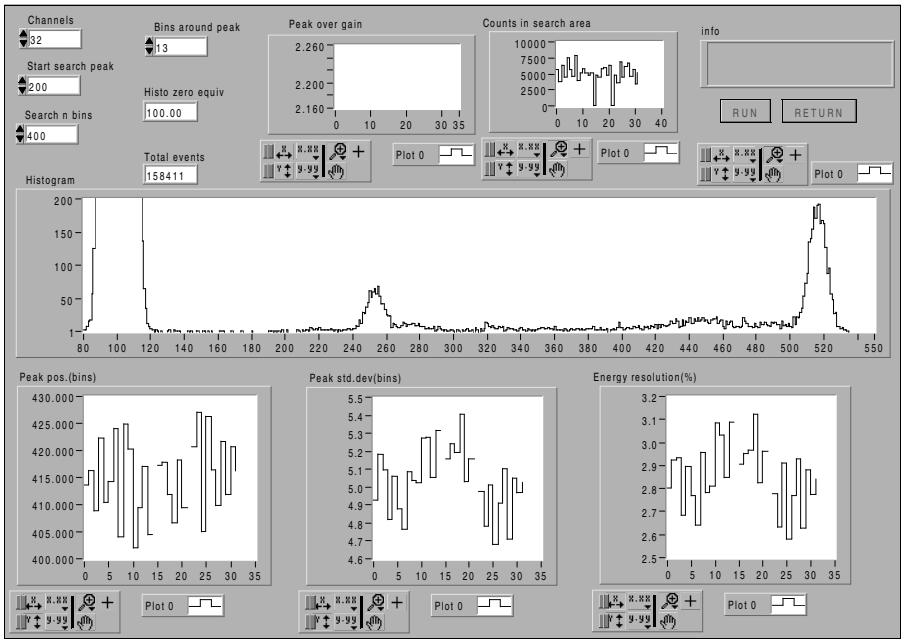


Figure 2.22: Pre-analyze of Am-241 data taken with VA-DAQ system.

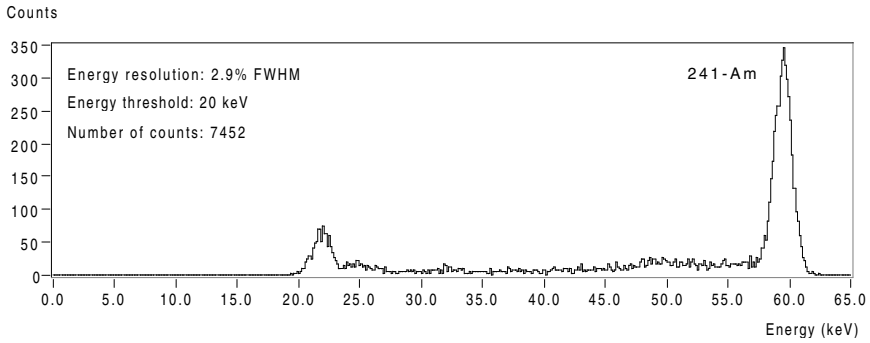
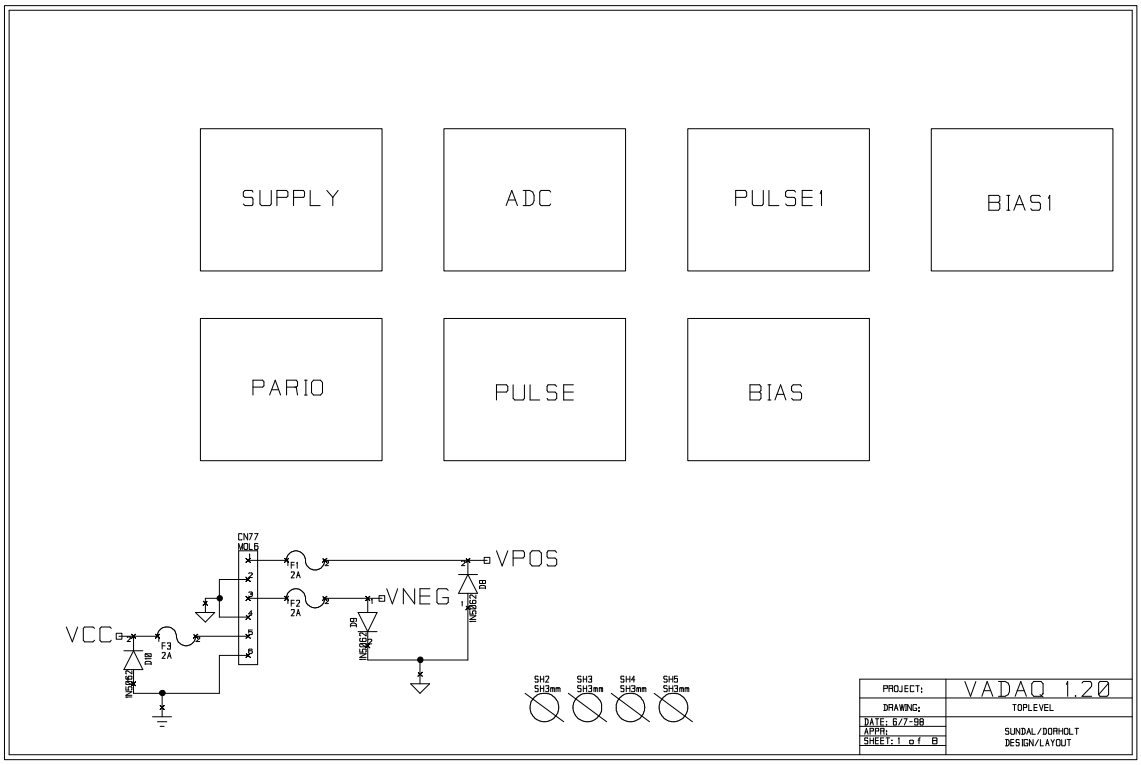


Figure 2.23: Am-241 spectrum from one pad of a 32 pad silicon detector.

system, and the card contains an 8-bit bi-directional bus, called the VA-DAQ bus. The PARIO unit sits between the PC and the VA-DAQ bus, allowing the PC to read and write to registers belonging to the other units over the VA-DAQ bus. The other units, all containing different analogue functions, are controlled by the state of these read and write registers. The VA-DAQ address space contains 8 readable and 8 writeable registers, making the VA-DAQ a memory mapped IO system. All operations that can be performed with a VA-DAQ system can be boiled down to a series of read and write operations to this IO-space (registers).

The design is implemented on a double Europe card (160 mm x 233 mm). The top schematic and the PARIO interface are found in figure 2.24. A silk print showing com-



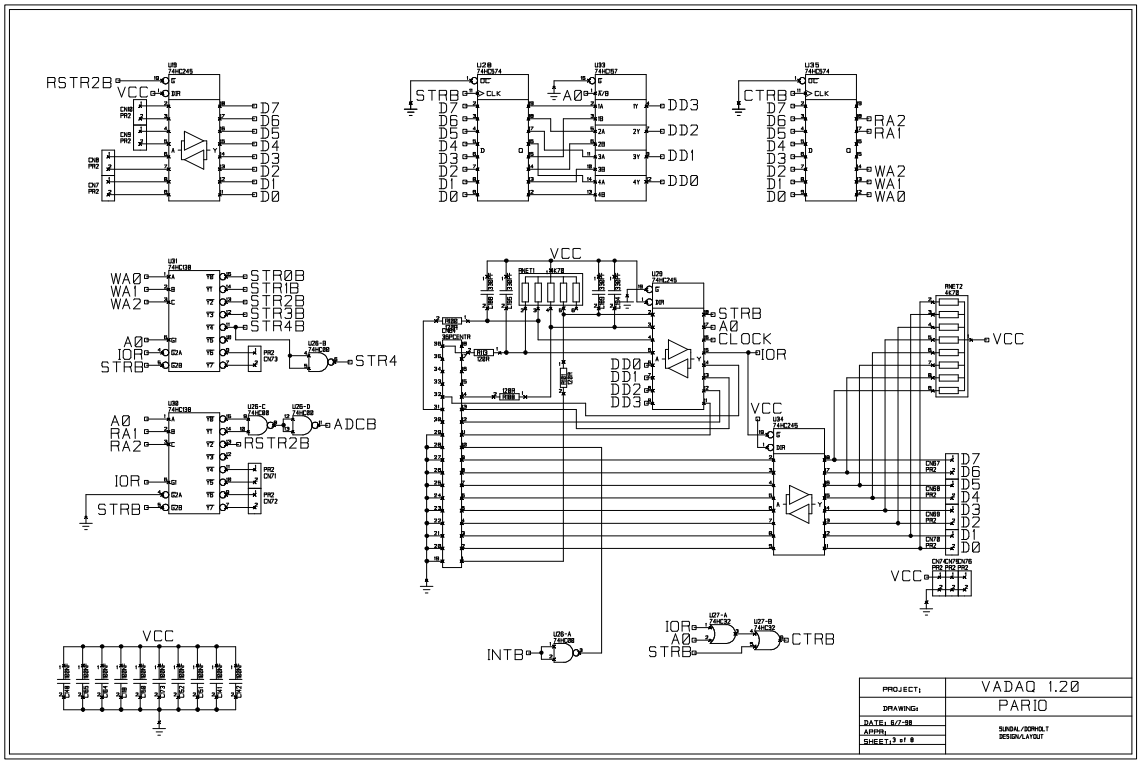


Figure 2.24: The top schematic and the PARIO schematic for VA-DAQ 1.20.

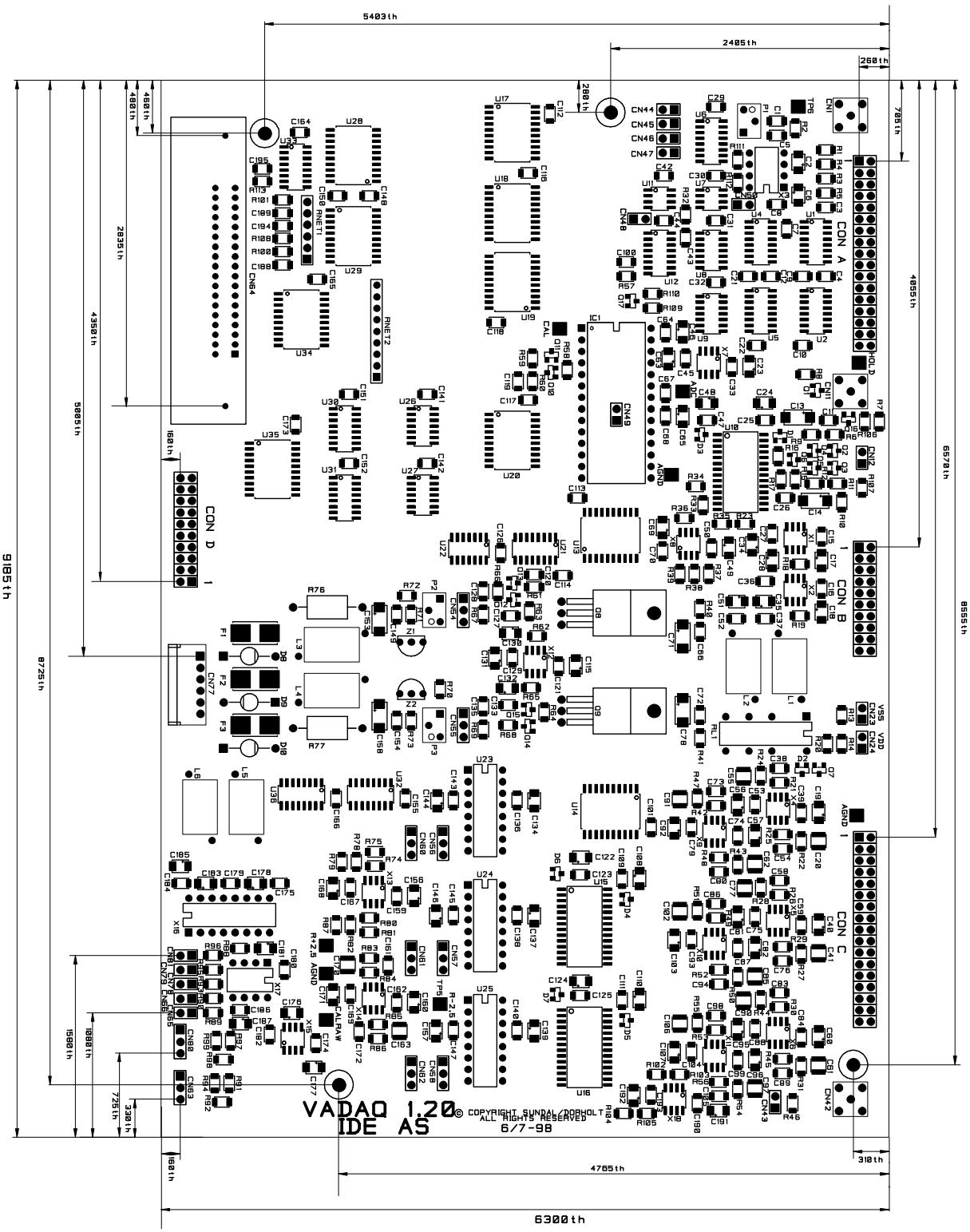


Figure 2.25: Silk print showing component placement and dimensions of VA-DAQ 1.20.

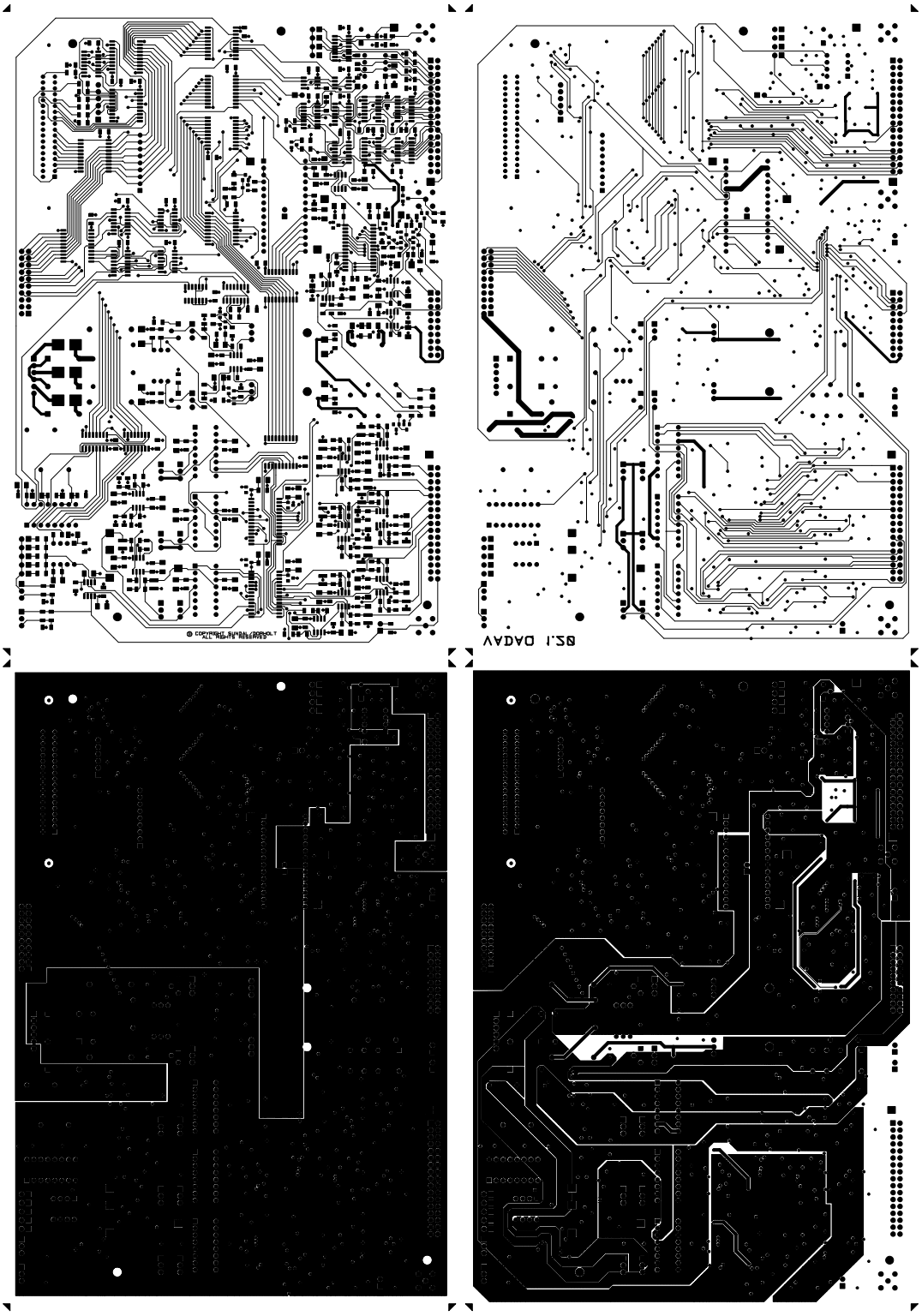


Figure 2.26: All 4 electrical layers of the VA-DAQ 1.20, showing from upper left to lower right: the top layer for component mounting, the bottom layer, the ground plane and the power plane.

ponent placement is given in figure 2.25. The VA-DAQ board contains just above 500 components, all mounted on the top side, and almost all being surface mounted. The design is a 4 layered structure. Two signal routing layers and two inner planes used for split ground and split power. Figure 2.26 is a collage showing all 4 electric layers.

A variety of connections to this local bus can be foreseen. The present VA-DAQ system use the parallel port of a PC as the outside world connection. The PARIO unit contains buffering and logic to map the parallel port Compatibility/Nibble-mode protocol for two-way data transport into the VA-DAQ local bus protocol. The low-level software driver on the PC contains all that is specific for the parallel port, such that the user of this driver sees only read and write operations to the VA-DAQ local bus as the possible/allowed operations.

In this way the only changes needed when changing the interface to say USB (Universal Serial Bus) would be to redesign the PARIO unit of VA-DAQ to a USBIO unit and change the driver to translate between USB and VA-DAQ local bus instead of between the parallel port and VA-DAQ local bus.

2.9.1 Parallel Port Interface; PARIO

The PARIO unit is the parallel port interface and uses Compatibility mode (Centronics or standard mode) for byte transport to VA-DAQ, and Nibble mode for the reverse data transport. Both these modes are supported by IEEE1284-1994, which is the industry defined parallel port standard. The schematic is shown in figure 2.24.

The VA-DAQ system has 16 1-byte registers, 8 for reads and 8 for writes. The interface has been designed such that a change to the much faster EPP (Extended Parallel Port) mode easily can be done. In this mode byte reads and writes are both performed in a single ISA bus I/O cycle. In this way at least 500 Kbytes of transfer rate could be achieved, even in the reverse direction, if the ADC is changed to a faster type (like LTC1419) that converts in 1.25 μs. A channel could be read out in approximately 5 μs (or less), compared to the current system where the read-out time is around 30 μs.

In the back end of the VA-DAQ card, access to the internal data bus is available on a 20 pin IDC (standard flat-cable) connector. The 8 data lines, 4 read strobes and 2 write strobes and also 5V digital and ground, are available. This makes it easy to build an extension card. By using a so called long ADAPTER card, the users can have access to the VA-DAQ bus and implement functions specific for their use.

2.9.2 Supply voltage generation; SUPPLY

The schematic for this unit is shown in figure 2.27. The low noise ± 2 V supplies are generated, based on a schematic originally from the CERN VIKING repeater used for VIKING chips.

Both supplies are monitored, and it is possible to measure the current to about 1 mA and the voltage to about 200 μV. It is possible to select between pot-meter or PC control (via a DAC) of each of the supplies by a jumper. The output of each supply is accessible

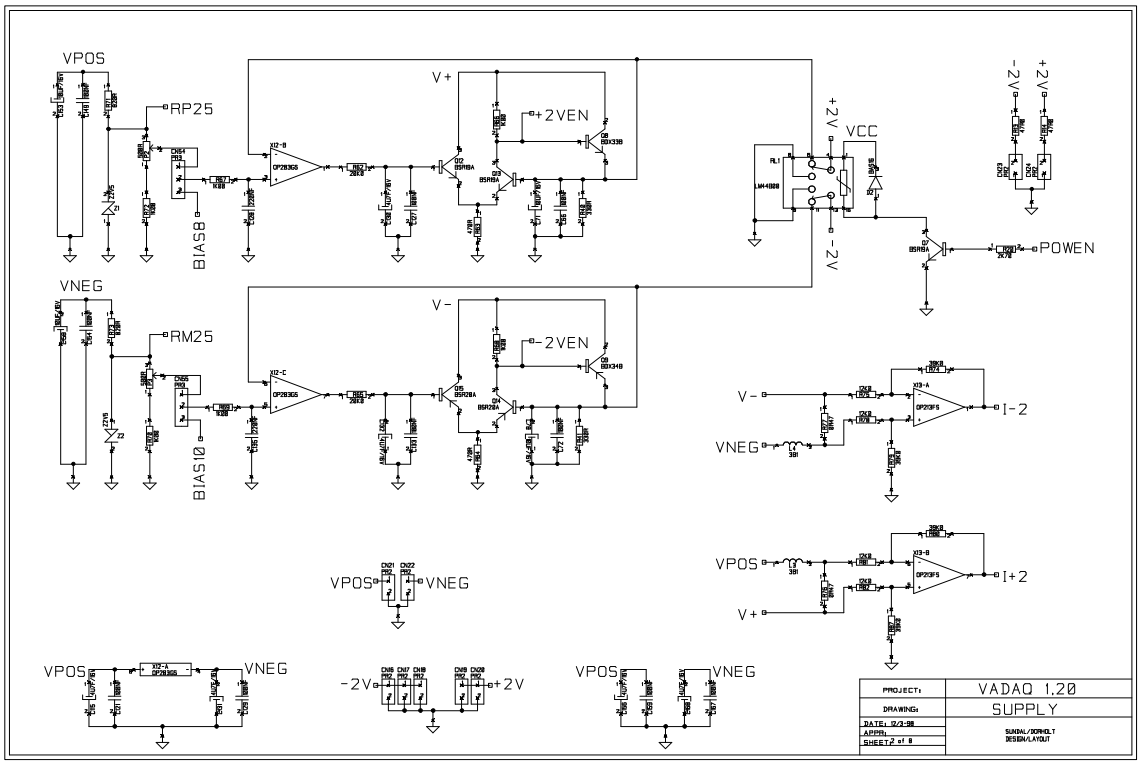


Figure 2.27: The SUPPLY schematic of VA-DAQ 1.20.

to the rest of the system via a software controllable relay. This can be used to avoid latch up during probe testing or to ground lines when swapping VA-boards under test.

In front two optional green light diodes indicates if the $\pm 2\,\mathrm{V}$ supplies are on. The intensity of the light indicates the voltage of the supply. About 1.8 V gives weak light while 2.4 V gives strong light.

2.9.3 Input signal selection and sampling; ADC

The ADC schematic is shown in figure 2.28, and it contains a 14-bit ADC called AD7871 from Analog Devices, with an input range of $\pm 3\,\mathrm{V}$. The input is buffered by an op-amp follower, which input is from a 16 channel input multiplexor. The 16 channels are the cards reference voltages ($\pm 2.5\,\mathrm{V}$), the VA chip supplies ($\pm 2\,\mathrm{V}$), the current draw of the chip supplies, the $\pm 5\,\mathrm{V}$ analogue supplies, the VA chip output after being processed by the trans-impedance input stage, the analogue ground, Monitor-A and B and finally 4 general signal inputs. The monitoring information comes from two 16 channel multiplexors, called Monitor-A and Monitor-B, which means that 32 channels of monitoring information, mostly from the biasing (BIAS) part, is available.

When the ADC has finished a conversion it asserts the parallel port $-$ACK line. Today this is polled by the readout program. A read-out routine being invoked by an interrupt

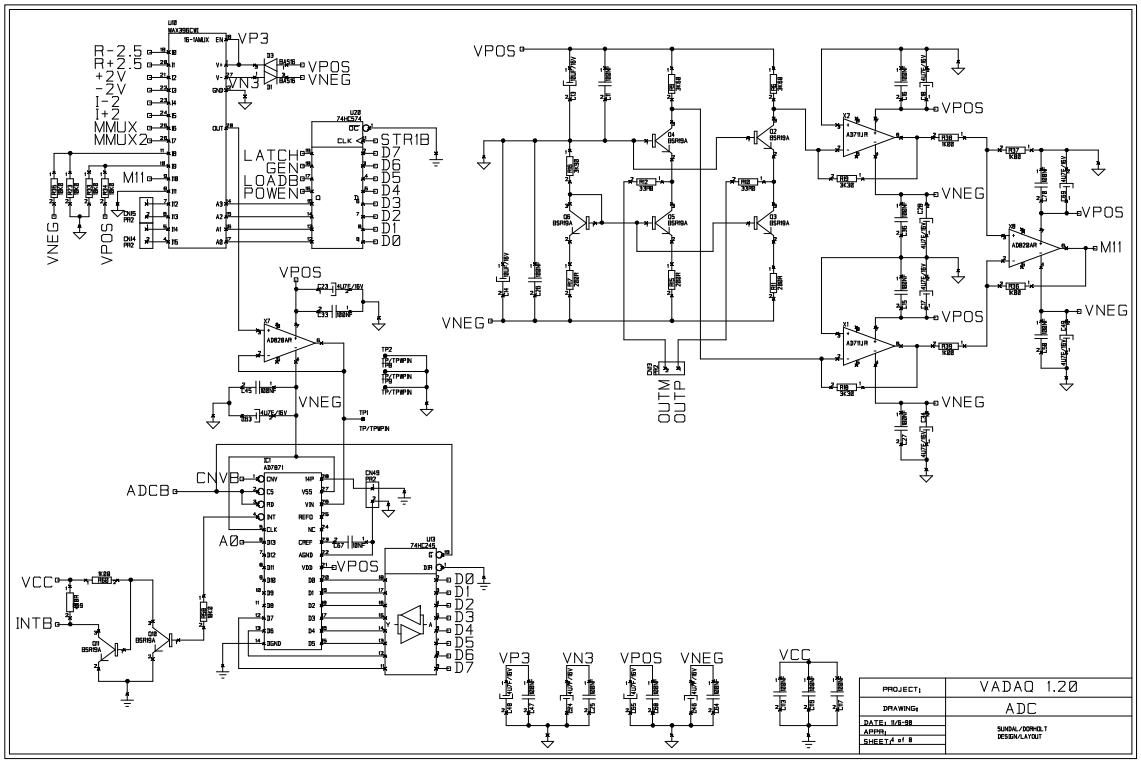


Figure 2.28: The ADC schematic of VA-DAQ 1.20.

can be used to process data every time the ADC has finished a conversion.

2.9.4 Digital signal generator and analogue test pulse; PULSE

This unit contains several sub-units, as can be seen in the schematic in figure 2.29. One sub-unit generates 8 differential digital signals at VA logic levels. Six of these are general. The two last one are primarily intended to be used for the clock and hold signals of the VA chip. If the VA ± 2 V are turned off, these lines are at ground levels.

The second sub-unit of PULSE generates the calibration pulse, which can have both polarities and is generated by a fast 8 bit DAC. The calibration pulse needs to be terminated by $50\,\Omega$ to avoid distortion. If this is the case, the rise/fall time of the pulse should be 20 ns or less. The attenuation of the step is performed by jumpers in the back plate of the VA-DAQ box, to allow for the great variety of input charges existing for the VA family. The attenuation jumpers are described in appendix A.

The third sub-unit processes the trigger (the trigger gives the time of the physical event) and generates the necessary hold delay. This delay is in the order of 500 ns to 30 μs for an external trigger. When the chip is pulsed with a calibration signal (which simulates an event by injecting a charge into a selected VA-channel), one can have delays in the range of about $-1\,\mu$s to 30 μs. Here a negative delay indicates that the chip hold is set before the

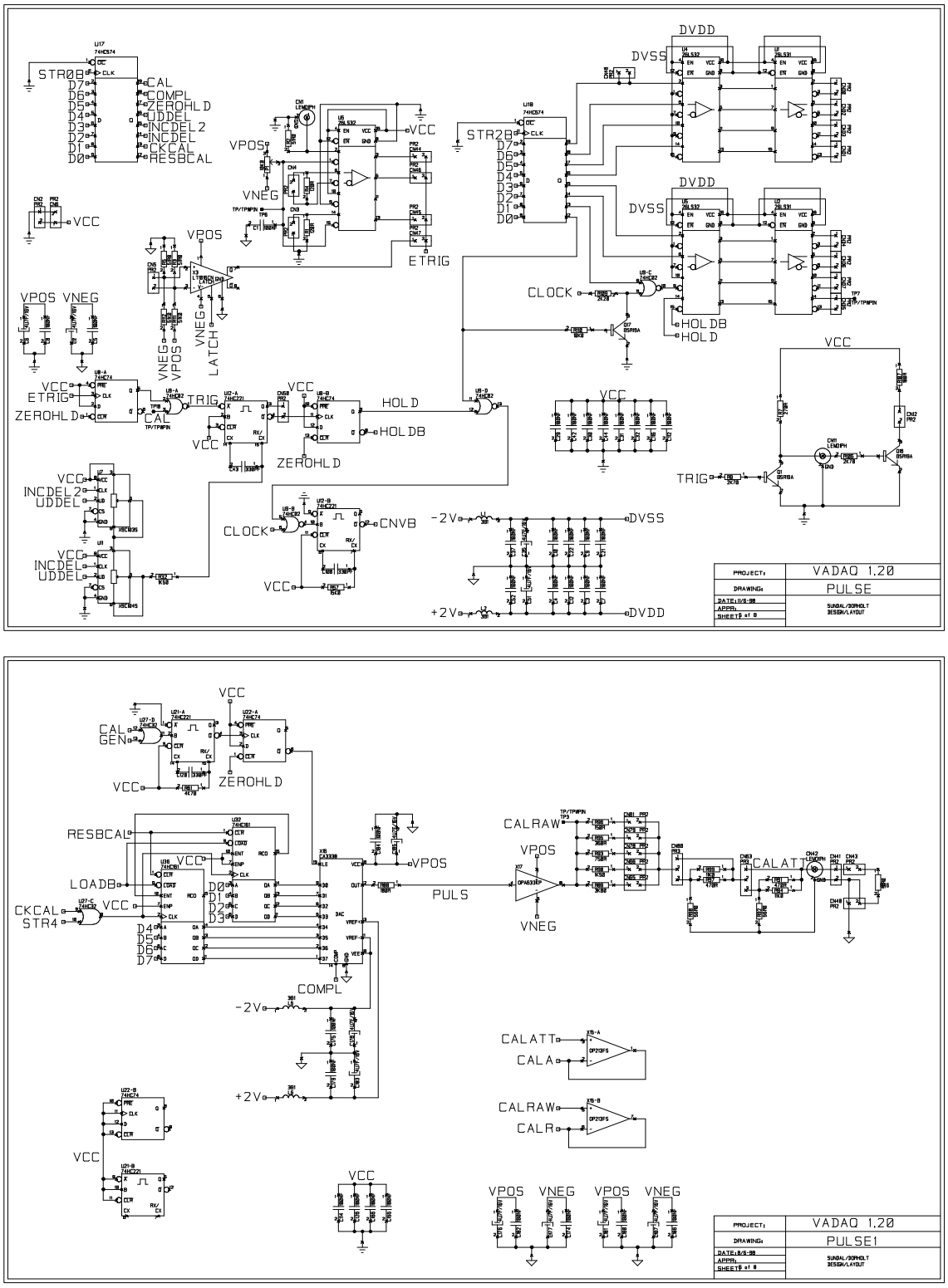


Figure 2.29: The PULSE schematic for VA-DAQ 1.20.

calibration line is pulsed. In this way the full waveform in the time domain (oscilloscope) of a VA chip can be investigated. The delay is set by a mono-stable, and the various delays are obtained by using a programmable CMOS resistor in the time constant for the mono-stable. Both resistors contain 100 steps, but one of them have a total resistance being 10 times the other. This allows for both the fine and coarse oscilloscope options found in the software.

It is possible to select between several types of external triggers. A NIM trigger can be given via a LEMO input. This input is terminated in 50 Ω. It is also possible to give a single ended TTL trigger, which is terminated in 50 Ω. A differential TTL (or RS422) terminated in 120 Ω is also available. The last trigger is a differential current trigger to be delivered by a TA chip, which is processed by a very fast comparator.

It is also possible to read back a byte of signals as TTL-levels. In addition spare analogue monitoring inputs can be used to read back logic signals at VA logic levels. This is typically used to check the shift out signal of a VA-chip. The advantage of analogue monitoring of digital signals is that the voltage levels of the logic signals are checked.

2.9.5 Bias generation and monitoring; BIAS

There are two sub-units in BIAS, one is the generation of biases for the VA chips, and the other is the monitoring of these biases. This is seen in the schematic in figure 2.30. The system can generate 12 biases, all monitored for both voltage and current. For every pair of bias (like BIAS0/BIAS1) a jumper needs to be set on the board to select between positive or negative voltages generated by this pair. This minor inconvenience gives a factor of two better resolution in the setting of a bias voltage. The 8 first biases can be referenced to either the ±2 V supplies or to the reference voltages (±2.5 V). The first alternative is the preferred choice since it grounds all biases when the ±2 V supplies are turned off. Only these 8 first should be used for the standard VA biasing currents and voltages vref, vfp, vfs, shabias, prebias and ibuf.

There are 6 available monitoring channels brought to the ADAPTER board by nonnector CON-C. These can be used differently from application to application. They can typically be used to remotely sense the value of ground and supply and vfp on the readout card. On the standard adapter boards only one of these are used to sense the threshold voltage for the TA chip, since it is taken not directly from a bias, but first scaled down by a resistor network.

2.10 Overview of read and write registers

All bits in the read and write registers are summarized in table 2.2 and table 2.3. The detailed function of each of the bits/signals are explained in appendix A.

The possible analogue values that can be sampled by the ADC is controlled by multiplexors. These are organized in a two-layer structure. The ADC input multiplexor is a 16-to-1 multiplexor, and the signals selected depends on the multiplexors 4-bit address.

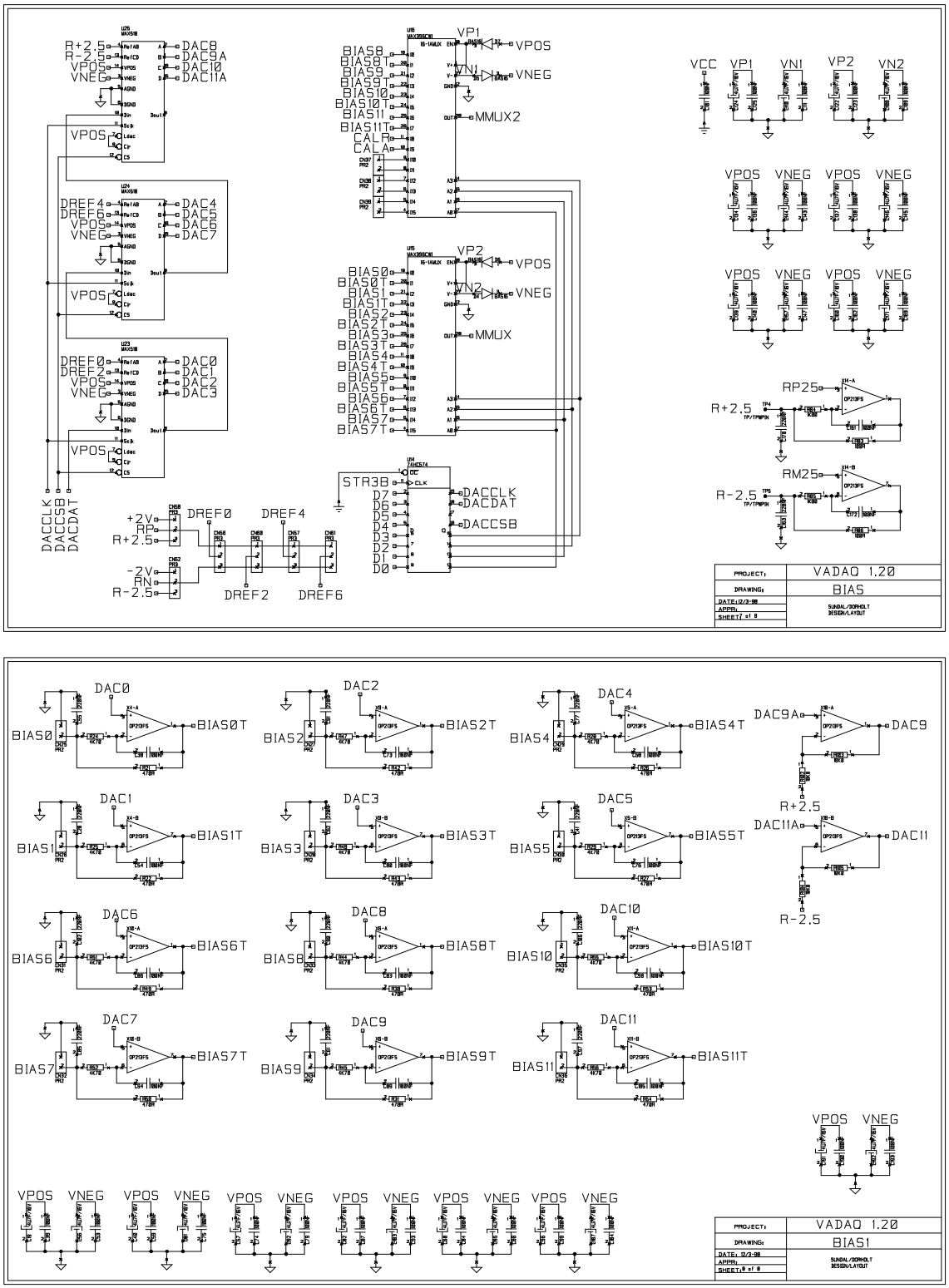


Figure 2.30: The BIAS unit performing bias generation and monitoring in VA-DAQ 1.20.

Address	Bit	Name	Description
W0	0	RESBCAL	Zero cal-pulse register value.
	1	CKCAL	Increase cal-pulse register value.
	2	INCDEL	Increase/decrease coarse hold delay.
	3	INCDEL2	Increase/decrease fine hold delay.
	4	UDDEL	Select increase/decrease for hold delay.
	5	ZEROHLD	Acknowledges/clears an ADC trigger.
	6	COMPL	Complement the value of the pulse DAC.
	7	CAL	Generate an internal trigger.
W1	0-3	SADR0-3	Select address of main signal multiplexor.
	4	POWEN	Turn on/off VA chip supplies.
	5	LOADB	Enables writing of pulse DAC.
	6	CALGEN	Pulses the calibration DAC.
	7	LATCH	Enables/disables TA triggers.
W2	0	CONVERT	Start ADC conversion.
	1	VADIG1, CK	The VA clock signal.
	2	VADIG2, DRESET	The VA reset signal.
	3	VADIG3, SHIFTIN	Controls the VA shift register loading.
	4	VADIG4, TESTON	Sets VA chip test mode.
	5	VADIG5, CLKIN	The TA shift register clock.
	6	VADIG6, REGIN	Data for TA shift register.
	7	VADIG7	Available digital signal at VA levels.
W3	0-3	MADR0-3	Selects address for the monitoring MUXes.
	4	DACCSB	Enabling of bias DACs down-loading.
	5	Unused	Reserved for future extensions.
	6	DACDAT	Data for serial bias DAC down-loading.
	7	DACCLK	Clock for bias DAC down-loading.
W4	0-7	DACBYTE	Calibration pulse register.
W5	0-7	Unused	Register reserved for future extensions.
W6	0-7	WREG6	Optional write register on adapter board.
W7	0-7	WREG7	Optional write register on adapter board.

Table 2.2: Summary of write registers in a VA-DAQ system.

The signals are described in table 2.4, and the address is controlled by the four lower bits of write register 1. Two of the multiplexor inputs are even connected to the output of two other 16-to-1 multiplexors, used for monitoring mostly the biasing part of the VA-DAQ system. The address for these two multiplexors are common and controlled by the four lower bits of write register 3. The signals on these two multiplexors are described in table 2.5.

The naming convention used in table 2.5 is as follows; BIASx are the actual voltages on the bias output lines and BIASxT is measured on the other side of a 470 Ω resistor, which allows measuring the current in each bias. CALR is the raw voltage of the calibration step signal before it is attenuated. The CALA is the voltage after the attenuation.

Address	Bit	Name	Description
R0	0-7	ADC0-7	Least significant byte of ADC result.
R1	0-7	ADC8-15	Most significant byte of ADC result.
R2	0-7	TTLREG	Readable TTL data on adapter board.
R3	0-7	Unused	Register reserved for future extensions.
R4	0-7	RREG4	Optional read register on adapter board.
R5	0-7	RREG5	Optional read register on adapter board.
R6	0-7	RREG6	Optional read register on adapter board.
R7	0-7	RREG7	Optional read register on adapter board.

Table 2.3: Summary of read registers in a VA-DAQ system.

Address	Signal name	Description
0	R+2.5	+2.5V reference voltage
1	R-2.5	-2.5V reference voltage
2	VDD	The VA chip +2V supply
3	VSS	The VA-chip -2V supply
4	I-2	The current in the -2V
5	I+2	The current in the +2V
6	MON-A	Data from monitoring MUX A
7	MON-B	Data from monitoring MUX B
8	-5V/2	Half the analogue -5V supply
9	+5V/2	Half the analogue +5V supply
10	VASIG	Signal from the VA chip
11	AGND	Analogue ground
12	SIG12	General signal for user
13	SIG13	General signal for user
14	SIG14	General signal for user
15	SIG15	General signal for user

Table 2.4: Signals on the ADC input signal multiplexor.

2.11 VA-DAQ connector description

The VA-DAQ PCB is equipped with three IDC connectors to facilitate plug-in boards (ADAPTER boards) that map all relevant signals to a connector in the front plate of the VA-DAQ box for the specific VA-hybrid used. These three connectors are named CON-A, CON-B and CON-C, as can be seen in the mechanical drawing showing dimensions, connectors and jumpers. The signals on these three connectors are found in the tables 2.6, 2.7 and 2.8.

The differential output current OUTP/OUTM from a VA-chip has a typical output range (OUTP-OUTM) of ± 5 times the ibuf value. The standard ibuf value is $140\,\mu$A giving an output range of $\pm 700\,\mu$A. The input trans-impedance amplifier of the VA-DAQ system uses $3.3\,\mathrm{k}\Omega$ resistors giving voltage swings of about $\pm 2.3\,$V to the $\pm 3\,$V input range ADC. This input stage was designed by the Cleo-III group to be used for the read-out of

Address	Monitor A	Monitor B
0	BIAS0 (TA vfs)	BIAS8
1	BIAS0T	BIAS8T
2	BIAS1 (vfs)	BIAS9
3	BIAS1T	BIAS9T
4	BIAS2 (ibuf)	BIAS10
5	BIAS2T	BIAS10T
6	BIAS3 (vref)	BIAS11
7	BIAS3T	BIAS11T
8	BIAS4 (vfp)	CALR
9	BIAS4T	CALA
10	BIAS5 (prebias)	MON10
11	BIAS5T	MON11
12	BIAS6 (shabias)	MON12
13	BIAS6T	MON13
14	BIAS7 (TA vth-neg)	MON14
15	BIAS7T	MON15

Table 2.5: Signals on the two monitoring multiplexors.

the VA-RICH boards. The general input signals are all well protected, and can sustain rather large over-voltages. The VSS is given one more line than VDD, reflecting that most current into the VA chips are in the VSS-AGND loop.

Several other connectors can be fitted to the VA-DAQ system, the details are explained in appendix A, only two will be described here. These are the PC connection and the power supply connection.

CN64: Centronics connector for parallel port communication

A standard Centronics cable to the PC is used. For correct load a 3 meter cable is required.

CN77: VA-DAQ supply connector

This is a 6-pin connector on a 100 mil grid. The leftmost pin, when the VA-DAQ is viewed from the back, is number 1. The pin-out of the connector is given in table 2.9. All three supplies should be floating, low-noise and linear. The analogue supplies should be 2 A and the digital 1 A. The supplies are listed in table 2.9. The same supply for analogue and digital +5 V could be used if not extreme noise performance is required.

User made extensions to the VA-DAQ bus

A mechanical description of the ADAPTER boards is found in figure 2.31. In the case of a long ADAPTER board, the VA-DAQ bus extension connector (CON-D) can be used. The pin configuration for CON-D is given in table 2.10. There are two write strobes and four read strobes found on the connector, to be utilized on the ADAPTER board. As write registers 6 or 7, a 74LS574 8-bit flip/flop can be used. This is easily implemented by connecting the data-bus to the data inputs of the LS574, and tying the wanted write strobe to the clock input of the LS574. Reads are just as easily implemented by using a 74LS245. Here the data bus is connected to the B-side of a LS245 (pins 11 through 18),

Pin	Signal	Description
1	VDIG	+5V digital supply
2	DGND	Digital ground
3	TTLSNG	Single-end TTL trigger (120Ω)
4	DGND	Digital ground (TTLSNG reference)
5	TTLDIFP	differential TTL trig. (120Ω)
6	TTLDIFN	Neg. phase of differential TTL trigger
7	TANEG	Negative phase of TA trigger
8	TAPOS	Positive phase of TA trigger
9	DGND	Digital ground
10	VDIG	Digital +5V supply
11	VADIG7B	General VA logic signal, neg. phase
12	VADIG7	Positive phase
13	VADIG4B(TESTONB)	VA logic
14	VADIG4 (TESTON)	pos. phase
15	VADIG6B(REGINB)	VA logic
16	VADIG6(REGIN)	pos. phase
17	VADIG5B(CLKINB)	VA logic
18	VADIG5(CLKIN)	pos. phase
19	VADIG3B(SHIFTINB)	VA logic
20	VADIG3(SHIFTIN)	pos. phase
21	HOLDB	VA hold signal
22	HOLD	pos. phase
23	VADIG2B(DRESETB)	VA logic
24	VADIG2(DRESET)	pos. phase
25	VADIG1B(CKB)	VA clock signal
26	VADIG1(CK)	pos. phase
27	RD2B0	Bit0 of read reg. 2
28	RD2B1	Bit1, TTL input
29	RD2B2	Bit2
30	RD2B3	Bit3
31	RD2B4	Bit4
32	RD2B5	Bit5
33	RD2B6	Bit6
34	RD2B7	Bit7

Table 2.6: CON-A. 34-pin IDC connector for digital signals and triggers.

the read strobe to the chip enable (pin 19 of LS245) and direction bit (pin 1 of LS245) is connected to +5V digital. To the A-side of the LS245 the 8 TTL-signals that one wants to read are connected.

2.12 VA-DAQ low and mid level software description

All communication between the PC and the VA-DAQ system goes through the hardware driver. The driver is a LabView VI implemented as a Code-Interface-Node (CIN), which means that the actual code performing the IO operations to the VA-DAQ address space,

Pin	Signal	Description
1	OUTM	Negative phase of the VA diff.current signal
2	OUTP	Positive phase of the VA output signal
3	SIG15	General input signal
4	SIG14	General input signal
5	SIG13	General input signal.(REGOUT)
6	SIG12	General input signal.(SHIFTOUTB)
7	AGND	Analogue ground
8	VSS	The VA chip -2 V supply
9	AGND	Analogue ground
10	VSS	The VA chip -2 V supply
11	AGND	Analogue ground
12	VSS	The VA chip -2 V supply
13	AGND	Analogue ground
14	VDD	The VA chip $+2$ V supply
15	AGND	Analogue ground
16	VDD	The VA chip $+2$ V supply
17	AGND	Analogue ground
18	VPOS	The analogue $+5$ V supply
19	AGND	Analogue ground
20	VNEG	The analogue -5 V supply

Table 2.7: CON-B. 20-pin IDC connector for analogue VA signal, and the chip supplies.

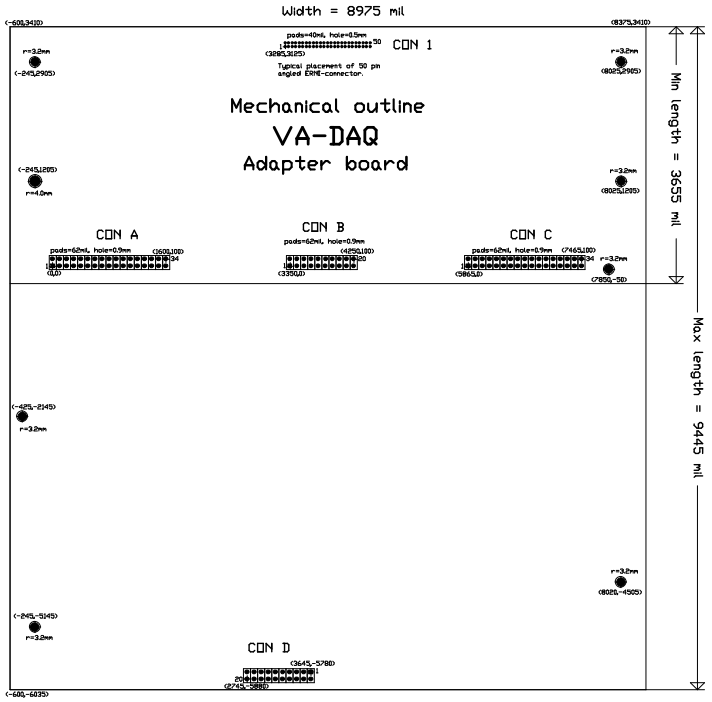


Figure 2.31: Mechanical outline of VA-DAQ Adapter boards.

Pin	Signal	Description
1	BIAS0	Is default used for TA vfs
2	AGND	Analogue ground
3	BIAS1	Is default used for VA vfs
4	AGND	Analogue ground
5	BIAS2	Is default used for VA ibuf
6	AGND	Analogue ground
7	BIAS3	Is default used for VA vref
8	AGND	Analogue ground
9	BIAS4	Is default used for VA vfp
10	AGND	Analogue ground
11	BIAS5	Is default used for VA prebias
12	AGND	Analogue ground
13	BIAS6	Is default used for VA shabias
14	AGND	Analogue ground
15	BIAS7	Is default used for vthr-neg
16	AGND	Analogue ground
17	BIAS8	Default used to set value of +2 V supply
18	AGND	Analogue ground
19	BIAS9	Default used for TA vrc
20	AGND	Analogue ground
21	BIAS10	Default used to set value of −2 V supply
22	AGND	Analogue ground
23	BIAS11	Default used for twbi
24	AGND	Analogue ground
25	MON11	Monitoring, channel 11 in Monitor-B, Default TA threshold
26	MON10	General monitoring input.(twbi monitoring)
27	MON13	General monitoring input.(GND sense)
28	MON12	General monitoring input.(vfp sense)
29	MON15	General monitoring input.(VDD sense)
30	MON14	General monitoring input.(VSS sense)
31	AGND	Analogue ground
32	AGND	Analogue ground
33	AGND	Ground for the calibration signal
34	CAL	Calibration pulse, (terminate in 50Ω)

Table 2.8: CON-C. 34-pin IDC connector for biasing and monitoring.

Pin	Signal	Description
1	VPOS	The +5 V analogue supply
2	AGND	Analogue ground
3	VNEG	The −5 V analogue supply
4	AGND	Analogue ground
5	VDIG	The +5 V digital supply
6	DGND	Digital ground

Table 2.9: CN77. 6-pin supply connector. Pin1 is on the left when the system is viewed from the back.

Pin	Signal	Description
1	DGND	Digital ground
2	VDIG	Digital +5 V supply
3	DGND	Digital ground
4	VDIG	Digital +5 V supply
5	DGND	Digital ground
6	VDIG	Digital +5 V supply
7	WSTRB7	Access strobe for write register 7
8	WSTRB6	Access strobe for write register 6
9	RSTRB7	Access strobe for read register 7
10	RSTRB6	Access strobe for read register 6
11	RSTRB5	Access strobe for read register 5
12	RSTRB4	Access strobe for read register 4
13	D0	Bit 0 (least significant bit) of data bus
14	D1	Bit 1 of data bus
15	D2	Bit 2
16	D3	Bit 3
17	D4	Bit 4
18	D5	Bit 5
19	D6	Bit 6
20	D7	Bit 7 (most significant bit) of data bus

Table 2.10: CON-D. 20-pin IDC connector for VA-DAQ bus extension to the ADAPTER board.

through the parallel port, is implemented as a C-code program linked to the VI.

The low level library, **Lowlevel.llb**, contains all functions to manipulate the hardware settings of the VA-DAQ system. An example list is setting hold delays, setting calibration signal size, choosing the analogue value to sample, turn on or off the chip supplies, setting bias values etc. These functions all work in hardware units, like ADC and DAC counts.

The mid level library, **Midlevel.llb**, more or less performs the same operations as the low level library, but tries to abstract from hardware units to real values like current, voltage and charge. Some of these involve calculations and the use of calibrated constants for the conversion from hardware units to physical units. The library **Globconv.llb** contains all global variables used in such conversions and also routines to translate between hardware units and physical units. The library **Calculate.llb** tries to assemble all calculations that are typically needed to achieve this higher abstraction level. Appendix A will list the most important VI's from these libraries.

2.12.1 The VA-DAQ hardware driver

The LabView version used to make the VA-DAQ VIs is version 4.1. The current hardware driver is written for Windows 3.11 and Win95. Common to all VIs that are involved in time sequential requests to the VA-DAQ hardware, are the error input and error output parameters. Each time the driver is called and it cannot perform the specified data fetch,

Mnemonic	Code	Description
Readword	0	Read a word. LSB at even adr, MSB at odd.
Readword14ext	1	Read a word, assuming 14bit ADC-value.
Readwordauto	2	Read and clocks VA and starts new ADC cycle.
Readword14extauto	3	As above, but assumes 14bit ADC data.
Writebytecore	1002	Writes, assumes writing enabled.
Writebyte	1003	Writes, changes to write mode if not.
Writebytetoadr	1004	Writes a byte to a specific register.
Writereadback	1005	Writes, and checks actual bus value.
Dtardy	100	Returns the ADC conversion status flag.
Waitrdy	101	Waits, but times out with error if not.
Waitrdyb	102	Waits for ADC, but times out if not.
Setport	500	Set parallel port hardware address.

Table 2.11: The most important VA-DAQ driver function code calls.

it will return an error out value that is equal to the error input plus one. The error output of a high level VI will always be the accumulated count of missed samplings that occurred during the run of the VI.

Another motivation for using error in and out nodes on all VIs is that it ensures sequential running without the use of the LabView (or G) construct 'sequence' that usually ruins the possibility to understand the data flow from one glance at the graphical code.

There are four other special inputs in addition to the error input, called Function, Address, Data and Mask. Function is a simple number to select the function one want the driver to perform. Table 2.11 describes the functions that are implemented and inherent to the hardware driver. Only four functions are vital; **Readword**, **Writebytetoadr**, **Waitdta** and **Setport**. **Readword** will read a word (16 bit) from the address specified in the Address parameter (even address required). The word is built by reading the least significant byte from read register 'Address' and the most significant byte from 'Address+1' of the VA-DAQ system. **Writebytetoadr** will write a byte to a register specified with the 'Address' parameter. The actual byte written is given by the 'Data' parameter, but only those bits marked by an 1 in the 'Mask' will be altered in the hardware register. The other bits will remain unchanged. **Waitdta** will poll a certain time (100 μs range) for a data ready (ADC finished sampling). If no data ready is received, it will time out with an error. **Setport** is only for initialization, and is used to set the hardware address of the parallel port. In Win3.11 and Win95, the address is 0x378 for parallel port 1.

Some higher level functions are put in the driver to speed up acquisition, since a lot of overhead is removed when the driver is not called for each read/write operation. These functions are not described in the function table for the driver, since they have their own VI's, though these VI's most often contains only a call to the driver.

2.13 Summary

The development of the VA-DAQ system has resulted in a low-cost PC based chip testing and read-out system for the VA-TA chip sets. The VA-DAQ system has shown the ability to measure chip parameters to a high accuracy, and is able to measure noise figures down to the lowest possible values given by the theoretical noise performance on the input transistor. Equally interesting and important is the possibility to measure chip parameters with similar good results based on probe testing.

A development starting with the first multi-channel multiplexed charge amplifiers like BALDER, AMPLEX and VIKING in the mid 80's has resulted in the VA/TA chips of today. A multitude of technical problems were solved in these years, resulting in chips that are commercially available for a wide range of applications (input ranges and capacitive loads). The chips are highly reliable, and are today off the shelf products, which due to the VA-DAQ system, can be delivered with guaranteed performance based on wafer testing or testing of finished boards. Exact measurements on a large number of chips have been used to find typical values for all important chip parameters.

The flexibility of the VA-DAQ system also allows it to be a read-out system. More than 20 systems have been sold worldwide to universities, research institutes and major companies for test and verification of new semiconductor detectors in materials such as silicon, CdTe and CdZnTe, making it a successfull product in the portfolio of IDE AS.

Chapter 3

Readout electronics for B-physics experiments

The most promising experiments for revealing completely new physics, like the Higgs sector and physics beyond the Standard Model, will take place at the Large Hadron Collider at CERN. At this pp-machine operating at a center of mass energy of 14 TeV the long awaited Higgs particle, predicted by the Standard Model, will hopefully be directly produced, giving us the understanding of the mechanism which provides particles with mass. The LHC we could call the energy and luminosity frontier of particle physics, due to the fact that one hopes for direct verification of new and heavy particles. In particle physics there has traditionally also been a sensitivity frontier. This branch has in later years been pursued by LEP, by very accurate Standard Model measurements, and also by dedicated B-physics and neutrino experiments. The B-experiments are also generally sensitive to very small rates, and accurate enough to detect small discrepancies from the Standard Model, which indirectly can predict new particles or physics. This was for instance seen in the discovery of the Z. The Z (91 GeV) was indirectly seen as 'neutral currents' in the CERN bubble chamber Gargamelle [26] and in the Hamburg PETRA e^+e^- collider. In the latter experiment with a total energy of 45 GeV it was seen as a forward/backward asymmetry in the $\mu^+\mu^-$ production caused by interference of the two channels, $e^+e^- \rightarrow \gamma \rightarrow \mu^+\mu^-$ and $e^+e^- \rightarrow Z^* \rightarrow \mu^+\mu^-$. The Z-mass was thus estimated before the first real Z was produced at the CERN SPS $p\bar{p}$-collider and detected in the UA1 experiment [29].

When the LHC experiments start, the sensitivity/energy frontier is not as easily differentiated anymore. Even though LHC is at the energy frontier, the extreme luminosity boost in the gigantic LHC experiments will make them very sensitive to rare decays and discrepancies from the Standard Model. The more dedicated B-physics experiments will however be built and give valuable results within the time span of the LHC construction. LHC will first start data taking around 2005, and in the years ahead of this, the most interesting experiments in the B-physics sensitivity frontier will be based on hadronic colliders like HERA-B and the Tevatron and the three large 'clean' leptonic (e^+e^-) collider experiments; BaBar at PEP-II (Stanford, US), Belle at KEK-B (KEK, Japan) and Cleo-III at CESR (Cornell, US). The most important goal of these experiments is the investigation

of the CP-violation found in B-decays, that can point to physics beyond the Standard model. The PEP-II and KEK-B colliders will operate with asymmetric beam energies, while CESR will be a symmetric beam experiment.

My involvement has been in the Belle and Cleo-III experiments. For Belle in the design, construction and testing of the front-end read-out boards for the Silicon Vertex Detector (SVD) and for Cleo-III in the design, construction and testing of the read-out boards for the Ring Imaging Cherenkov Detector (RICH). These are vastly different sub-detectors in experiments with more or less the same physics goal, and serves as a good comparison of the use of front-end electronics in different sub-detectors. The physics of the different sub-detectors motivates the different technology choices made for the two readout boards.

The Cleo-III board went through three iterations in production starting around the summer of 1996, and all boards were delivered in batches of typically 200 ending around end of 1998. The responsible contact person in Cleo-III has been M.Artuso at Syracuse University in the US. The Belle board was made in two versions during the last part of 1997, and the deliveries starting in the first part of 1998. The first board, a prototype, is described in most detail, based on a PCB and AlN substrate glued together. The second board used for the deliveries was a multi-layer AlN hybrid in the Kyocera thick film process. At the Belle collaboration I have had the pleasure of working with D.Marlow at Princeton University and M.Hazumi at Osaka University.

A large amount of chip and board statistic has been collected. The Cleo-RICH project involves around 2200 readout boards and the Belle-SVD about one tenth of this. For both projects the basis for the analysis has been around half the boards. The statistics does not only give important insight into typical spread in chip parameters, but also proves the validity of probe testing results in the assembly of the readout boards. In addition has the testing proved the usefulness of the VA-DAQ test and readout system described in chapter 2.

3.1 The Belle and Cleo-III experiments

Compared to one of the big experiments at LHC, ATLAS or CMS, the Belle and Cleo-III detectors are rather small, seen already in the amount of people involved. The ATLAS and CMS experiments involve of the order of 150 institutes and close to 2000 persons, whereas the Belle and Cleo-III experiments both involve about 250 persons. Also the size of ATLAS, over 20 m tall and 25 m long and a mass of over 7000 tons will dwarf a detector like Cleo-III with an overall dimension of about 6 m and a mass of 1000 tons.

Both KEK-B and CESR are e^+e^- collider that are typically operating at a center of mass energy of 10.57 GeV, which is on the $\Upsilon(4S)$-resonance, giving the highest possible production rate of B-mesons. In the case of CESR the beam is symmetric, whereas KEK-B operate with an e^- beam about three times as energetic as the e^+ beam. Since typical branching ratios are in the order of 10^{-6} one needs about 100 million B-meson pairs produced per year (integrated luminosities of about 100 fb^{-1}) to get good statistics.

CP-violation is described in the Standard Model by the Cabibbo-Kobayashi-Maskawa

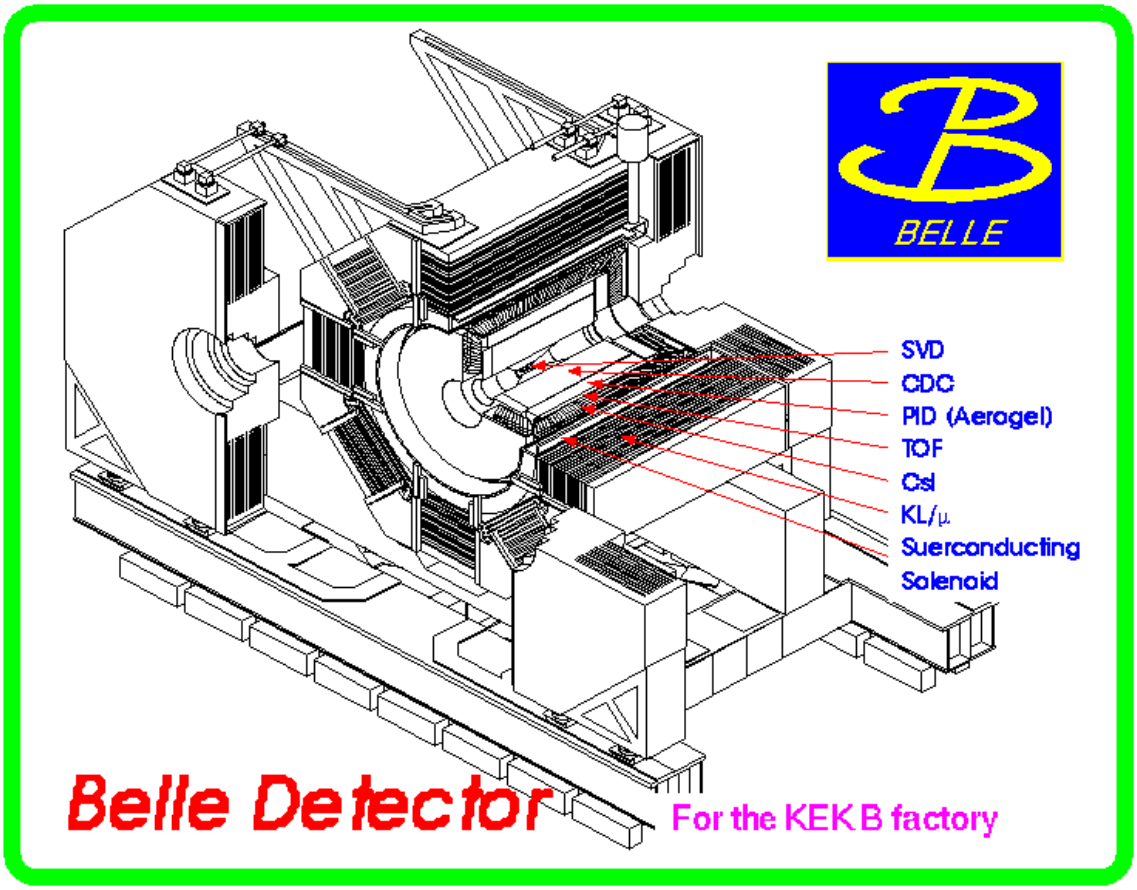


Figure 3.1: The Belle detector at the KEK-B collider.

(CKM) matrix. According to the SM the 3 by 3 coupling matrix (CKM-matrix) of the three quark generations must be unitarian. The matrix can be represented as three phasors in the complex plane, and the matrix is unitarian if the three phasors form a closed triangle. The verification can be reduced to the problem of measuring the length of the phasors and the internal angles of the triangle [28, chapter 1].

In the case of the Belle experiment, it has been optimized to look for decay channels of B-mesons that will give the best possible measurements of the three angles. And the first glimpse of physics beyond the Standard Model can be seen if the sum of these angles are not 180^o. In the Cleo-III the symmetric beam assures that the B's are produced almost at rest, giving no particles with momenta above 2.6 GeV, ensuring better energy resolution and fewer particles lost along the beam direction. Since there is no boost along the beam direction, the time evolution of the decays will not be as simple to measure as in the Belle experiment [29].

All e^+e^- collider experiments will have more or less the same construction, illustrated in figure 3.1 showing the Belle detector. Closest to the beam a tracking detector is found, especially important in the case of B-physics to properly reconstruct primary and secondary

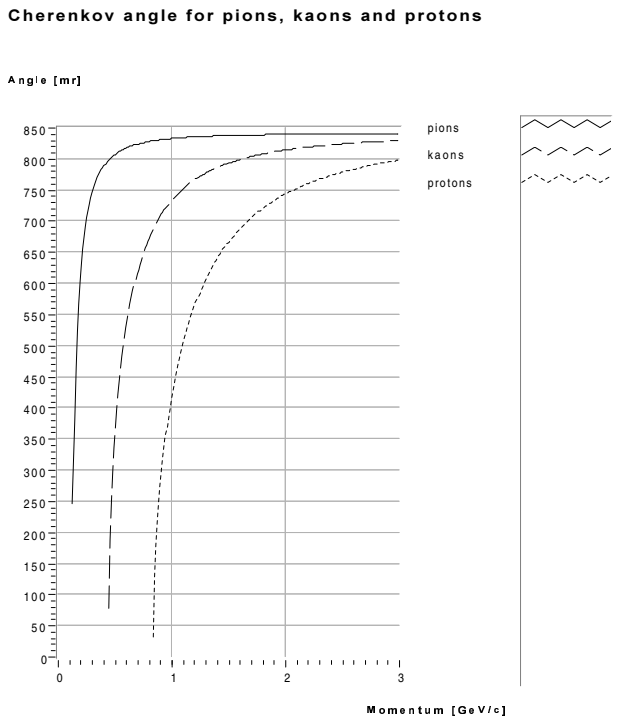


Figure 3.2: The Cherenkov angle for pions, kaons and protons in the LiF radiator of the Cleo-III RICH.

vertices of the B-decay. Belle and Cleo-III will be using a 3/4-barrel Silicon Vertex Detector based on double sided silicon strip detectors. The next tracking element in both detectors is a wire drift chamber. The wire drift chamber will also give a measurement of traverse momentum in the $0.5 - 1.0\,\%$ range and dE/dx resolution around $6\,\%$. The next detector element is the particle identification. In Cleo-III this will be a Ring Imaging Cherenkov detector (RICH), to replace Time-Of-Flight detectors (TOF) in Cleo-II. Belle will use both TOF and Cherenkov detectors, but the latter detector will be using photo-multiplier-readout compared to the MWPC readout in Cleo-III. The dE/dx measurement from the wire drift chamber is also used to supplement the particle identification. The importance of the particle identification comes from the requirement of separating K and π. The following electro-magnetic calorimeters will in both experiments be based on CsI. Belle will use a crude hadron calorimeter (K_L-catcher) outside the magnet to detect decays/interactions of K_L. This will indirectly reveal the muons. Cleo-III will rely on interleaved proportional tubes in the return yoke of the magnet as an alternative way of doing muon identification.

3.2 The Cleo-III RICH

The aim of the RICH is to provide particle identification. In a B-physics experiment the crucial separation is between π and K up to the highest possible meson-energy of 2.8 GeV. The required separation is 3 sigma or better, compared to about 2 sigmas obtained from

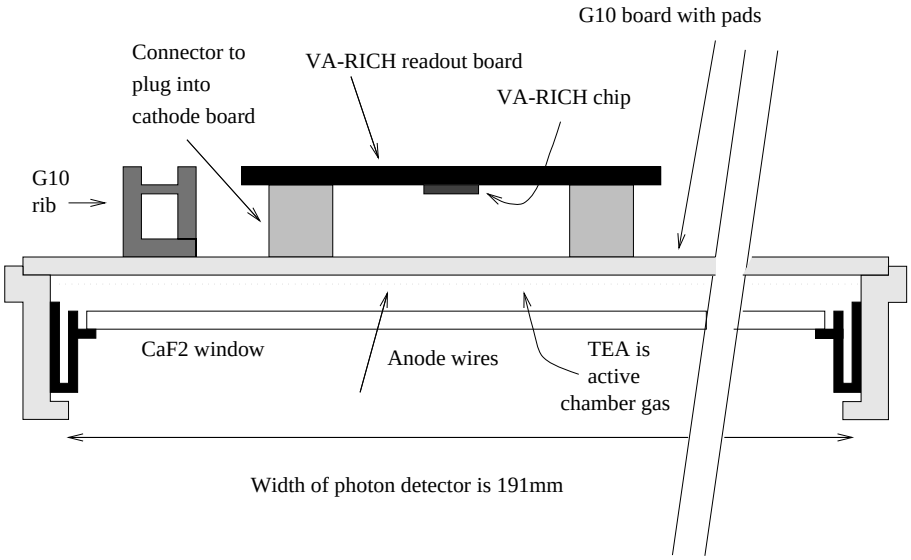


Figure 3.3: The photon detector of the Cleo-III RICH.

the dE/dx measurement of the wire drift chambers. Figure 3.2 shows the Cherenkov angle as a function of particle energy for π, K and protons up to 3 GeV [30, page 10]. The separation between π and K is 12.8 mrad at the highest energy. A better than 3 sigma separation gives a design goal for the resolution of about 4 mrad.

The cone projected onto the cathode plane consists of hits due to several detected photoelectrons and the accuracy of each of these do not need to be 4 mrad. The detector is designed to give an average of $N = 12$ photo-electrons for each track, and thus each photo-electron need only be reconstructed to an accuracy of $\sqrt{N} \cdot 4\,\mathrm{mrad}$ or about 14 mrad, to reconstruct the track to $\sigma = 4\,\mathrm{mrad}$.

3.2.1 Mechanical description of the Cleo-III RICH

The RICH detector is cylinder-shaped, with an outer radius of 1.01 m and an inner radius of 0.82 m and a total length of 2.4 m. The detector is segmented into 30 sectors in azimuth, giving elements of about 0.2 m width, 2.3 m length and 0.2 m thickness. The inner wall of this sector consists of a LiF window where a crossing particle will produce a cone of Cherenkov light. These windows are about 0.17 m long, so 14 are stacked to form the full length of the sector.

The Cherenkov cone of light will expand in the inner volume of the sector for 0.16 m [30], this volume being filled with N_2-gas, until it hits the photon detector. The photon detector, shown in figure 3.3, is itself a wire chamber of a few centimeter thickness. The inner wall in the wire chamber is a CaF_2-window transparent to photons in this energy range. The outer wall is put together of G10 printed circuit boards. On the inside the G10 boards contain pads of 7.5 mm by 8.0 mm forming cathode pads for the wire chamber.

The 70 anode wires, made of 20 μm Au plated W, are stretched in the full length of

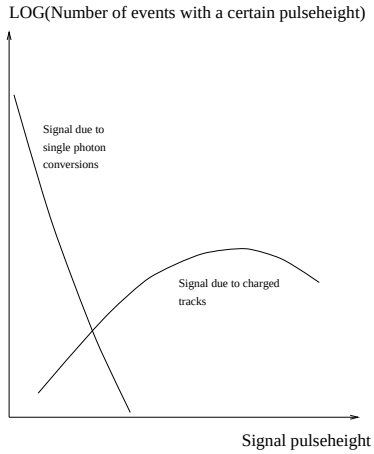


Figure 3.4: Signal released in a MWPC channel for single photons and for charged tracks.

the sector and soldered and glued in the two ends. Every 30 cm these are held in place by ceramic spacers to maintain the wanted 1 mm spacing to the cathode board. To form the correct drift field a second cathode is needed. This cathode is made as 100 μm wide conducting traces vacuum-deposited onto the CaF_2 window.

The MWPC gas is TEA (trethylamine) as the photo-converter, added some CH_4 (methane). The maximum in the photo-conversion cross-section is at 150 nm with a mean free path of 0.5 mm. The photoelectrons will drift towards the anode wires. Close to the wires the strong field will make an electron avalanche, producing a large number of electrons and ions. The electrons are very fast collected by the anode, while the more slowly collected ions will drift towards the cathode pads. The drifting ions induce a signal in the cathode pads, to be detected by the front-end amplifiers. The expected signal due to one photo-converted electrons is rather small. The probability for larger signals drops exponentially with the signal size. This is schematically indicated in figure 3.4 [30, page 13].

One would think that the front-end amplifiers would not require a very high dynamic range. This is wrong, since charged particles will give much larger signals. A charged particle crossing the gas will give an ionized track producing a large signal in some cathode pads in the center of the ring formed by the photoelectrons. Figure 3.4 shows that the large signals are from charged tracks. In fact the tracking of the charged particles is improved by use of the RICH information.

The cathode pads on the G10 boards are routed through the board to connectors soldered on the outer side. The VA-RICH readout boards are plugged into the connectors, as seen in figure 3.3. Each board is plugged into two connectors and processes the signals from 128 cathode pads by means of two 64-channel VA-RICH chips.

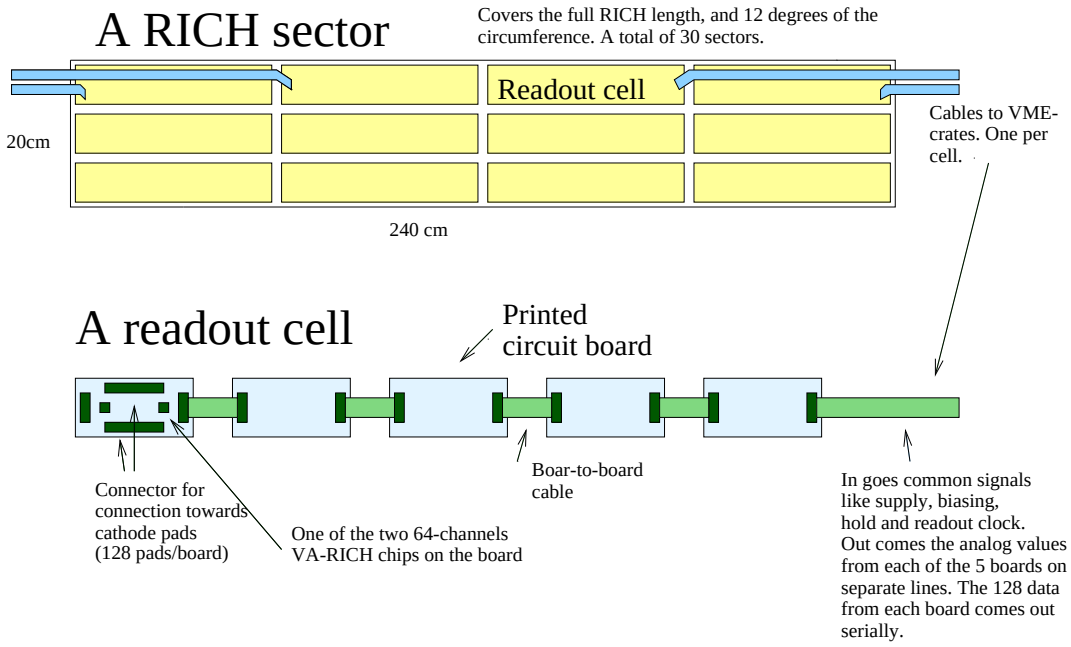


Figure 3.5: Description of a Cleo-III RICH readout sector and a readout cell.

3.2.2 Read-out structure of the Cleo-III RICH

The read-out boards are plugged into the outer side of a sector as explained in the previous section. Each sector has been divided into 12 read-out cells, 3 in width and 4 in length. Each cell consists of 5 readout-boards daisy-chained together, and with a common cable out of the detector and to a read-out module in a VME-crate. The functionality of a sector and a cell are shown in figure 3.5. Each cell of 5 boards will contain $128 \cdot 5 = 640$ readout-channels and a sector of $640 \cdot 12 = 7680$ channels. Since the full detector consists of 30 sectors, the RICH detector will contain $30 \cdot 7680 = 230400$ channels placed on 1800 readout-boards. Figure 3.5 also shows that each board in a cell has its own analogue output to facilitate digitization of a full cell in parallel.

3.2.3 The VA-RICH readout boards

The VA-RICH readout board is a 4-layered printed circuit board. The mechanical dimensions are 107 mm by 42 mm. The board is not symmetrical in width and length about the four (2.45 mm) guiding holes for the board-to-board connector, but 1 mm shorter on the left edge. The board went through two upgrades, and the described board is the last version.

3.2.4 VA-RICH board schematic and description

The VA-RICH chip is a 64-channel VA readout chip as described in chapter 2. Since sparking is a risk in a MWPC is each channel protected with a resistor and clamping

diodes in front of the pre-amplifier, not found in other VA-chips since it adds some noise. The design goal for the RICH is to use a 5 MHz readout clock, which will require around 30 μs to sample, hold and readout the 128 channels of a readout board (or cell, since they are read out in parallel). The parameters of the VA-RICH chip was summarized in table 2.1 and the layout shown in figure 2.3 of chapter 2.

The output of a VA-chip is a differential current, which gives a very low noise readout due to its low susceptibility to pick-up, and the ability to directly drive cables in the 10 m range. In the VA-RICH case are the cables around 6 m long.

The schematic of the board is shown in figure 3.6. Each board contains only two active components, the 64-channel VA-RICH readout chips, with their 128 signal inputs routed to two 70-pin JAE connectors which serve as the interface towards the cathode plane G10 boards.

Since a readout cell daisy-chains five readout boards, all signals that are to be supplied in parallel to all boards are routed straight from the input connector to the output connector (next board in the chain), as indicated in figure 3.7. Biasing, supply and digital control signals are all in this category. The branch off of signals to the chips is done to minimize the length of the branches. In the case of the chip biases, the branch off contains an RC, to decouple the bias close to each chip. This low-pass filtering is around a few kHz, so that the most dangerous noise for the chip (100 kHz range, since the signal peaking time is in the order of 2 μs) is filtered out. For the supply, each branch (either VSS, the -2 V supply, or VDD, the $+2$ V supply) is split into two sub-branches. One branch is for the analog and one for the digital supply of the VA-RICH chip. Each branch can be fitted with a decoupling capacitor. In the digital branches there are not much current floating, so 100 nF is enough. In the analog branches there are about 7 times the current in the VSS branch compared to the VDD branch. To accomodate this there is made room for two decoupling capacitors in each VSS branch. In both branches 1 μF ceramics are used, while the second VSS position is fitted with a 100 nF.

All digital signals are provided differential. There is made room for terminating resistors on the boards, and these are mounted only on the last board in a cell. The termination scheme is such that both lines of a differential pair are terminated in a resistor. A pair in a long flat-cable typically has $100 - 120\,\Omega$ of characteristic impedance, and the resistor is chosen to be $100\,\Omega$.

There is room for one thermistor. It can be fitted on one of the boards. If several are put one, the effect will be to measure an average temperature of the boards fitted with thermistors. One could argue that to really measure temperature to good precision one would need to bring out both ends of the thermistor, and not grounding one end on the hybrid. This is true if an absolute temperature measurement is needed, because it is not easy to know the potential drop in the ground between the hybrid and the point where the monitoring is performed. In most cases, however, the absolute value is not very important, what really matters is to monitor sudden changes, which indicates an error condition.

The analogue outputs are in parallel from the five boards in a readout-cell. Since the cell is daisy chained, and the readout-boards are identical in production, the board must route all five outputs between input and output connectors (CON1 and CON2). On the

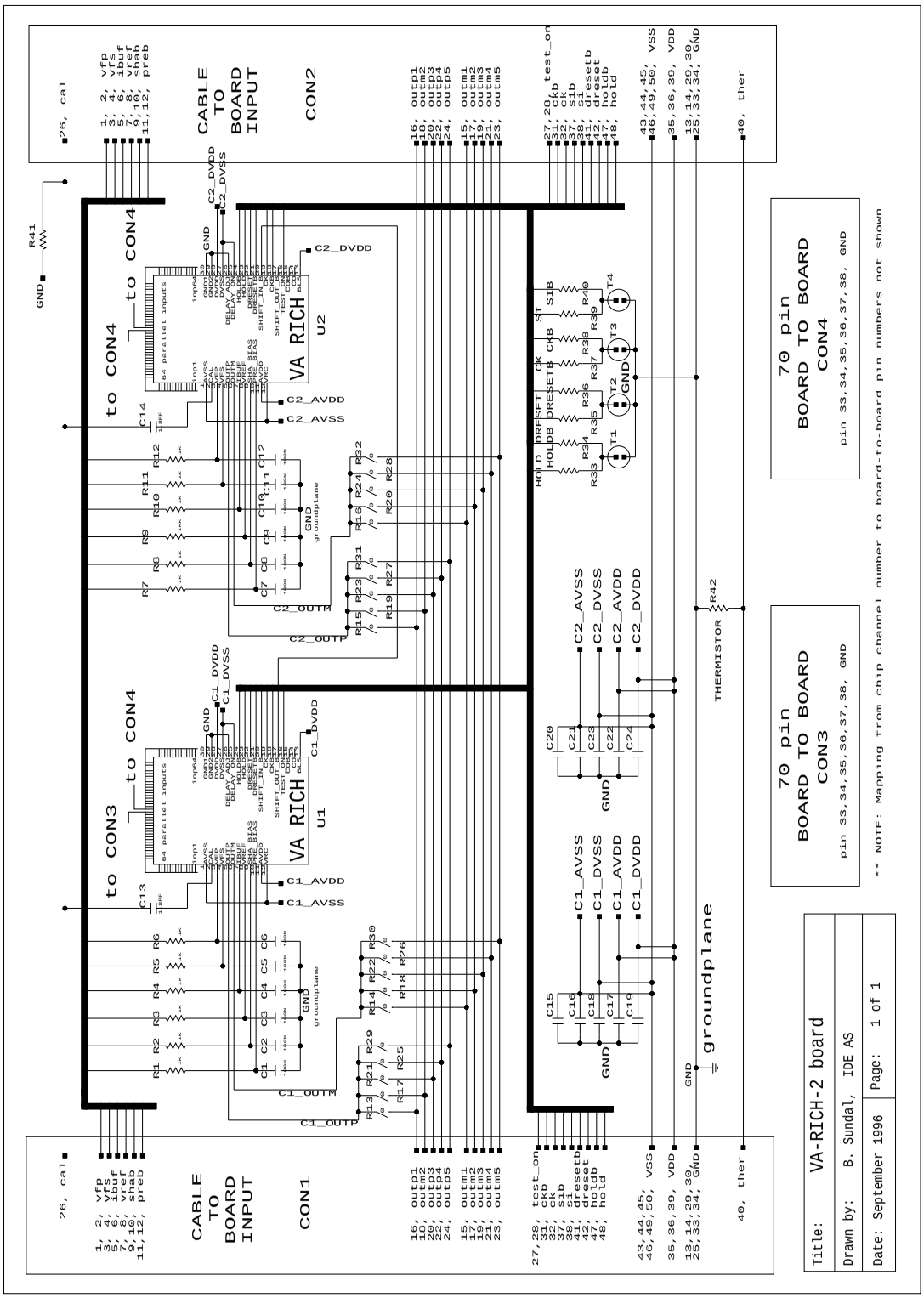


Figure 3.6: Schematic of the VA-RICH readout boards.

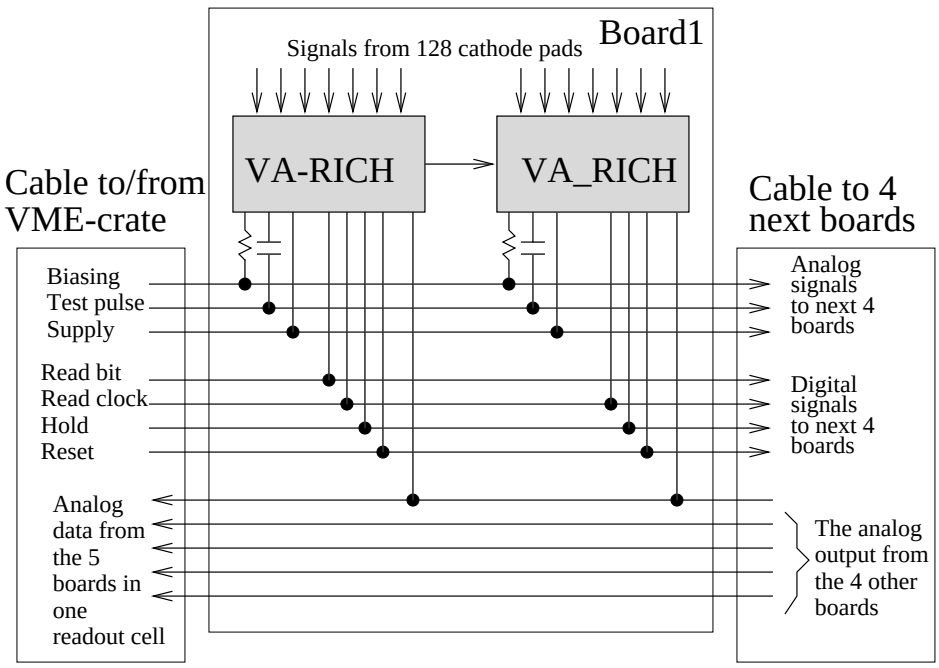


Figure 3.7: Functionality of a VA-RICH board in a read-out daisy chain.

board one can by means of $0\,\Omega$ resistors decide to which of these five outputs the chip output of the board should go. This is seen in the schematic, but the chip output is a differential current output, so that the total number of lines passing between the two connectors are 10. Inside a board the two chips are daisy chained, by taking the shift-out of the first chip to the shift-in of the second. Both chips on a board should by means of the $0\,\Omega$ resistors be connected to the same output line. With this connection the two chips on one board behave exactly as a single 128 channel chip.

The components list is shown in table 3.1, and a description of the pin numbering for the board-to-board connectors is found in table 3.2.

3.2.5 VA-RICH board material and layout considerations

Board material and PCB process

The PCB is of FR4 material with a total thickness of 1 mm, thick enough to give a satisfactory mechanical stability in this application where the boards play no role in support or alignment of any critical detector component. FR4 is also the most used PCB material, and hence the cheapest in production. The FR4, which is an epoxy material, is also thin with respect to radiation length. A 4-layer board is necessary, both due to the large amount of signals in a small area, and for the desire to have a low resistivity and low inductive ground plane.

Components	Value	Board no.	Description
U1, U2		All	VA RICH chips.
CON1	50 pin	1	Angled ERNI connector on bottom.
	50 pin	2-5	Samtec connector on top side.
CON2	50 pin	1-4	Samtec connector on top side.
CON3, CON4	70 pin	All	JAE Board to board connectors.
R1 thru R12	1kΩ	All	Bias current/voltage limiting.
C1 thru C12	100nF	All	Decoupling of bias.
C13, C14	1.8pF	All	Calibrate capacitors.
C15 thru C24	100nF	All	Decoupling of supply.
R13 thru R16	0Ω	1	Select analog line.
R17 thru R20	0Ω	2	Select analog line.
R21 thru R24	0Ω	3	Select analog line.
R25 thru R28	0Ω	4	Select analog line.
R29 thru R32	0Ω	5	Select analog line.
R33 thru R40	100Ω	5	Terminating digital lines.
R41	50Ω	5	Terminating the cal-step.
R42	-	3?	Thermistor for temperature reading.

Table 3.1: Component list for the VA-RICH boards.

The PCB conductors are in the outer layers made by a 17 μm Cu process. To facilitate 25 μm Al-bond wiring of the chip on the top layer, the Cu has an approximately 5 μm Ni cover and about 1 μm Au on top. The most important design rules are 4 mil (100 μm) tracks and spacing, and minimum via pads of 20 mil (500 μm), with the drilled via of half this diameter. The inner layers have conductors of double thickness (35 μm), which has the effect that tracks and spacings must be increased to 5 mil. The vendor used for the design was KAM Circuits in England, chosen for their ability to provide a low pitch and gold covering of the traces. Both factors are vital for assuring mounting and bonding of a low pitch chip directly to a PCB. The VA-RICH chip covers an area of about a fourth of a square centimeter and requires 90 bonds to the PCB spread over three of its edges.

Components

The only two active components are the two 64 channel VA RICH chips. The active components together with the rest of the components are mounted on the top layer. Only the connectors CON1 and CON2 are hole mounted, the rest of the components are surface mounted. All SMD resistors and capacitors are in the series 1206.

Chip cooling

Each chip is placed by conducting glue on a copper plane that is connected to the negative analogue supply. This serves as the substrate connection for the chip, but also as the the chip cooling. Cooling is improved by having the plane extend to a bigger area than the

Pin number	Signal name	Description
1,2	vfp	Pre-amp feedback resistor control voltage.
3,4	vfs	Shaper feedback resistor control voltage.
5,6	ibuf	Pre-amp/shaper buffer current.
7,8	vref	Output level adjustment.
9,10	sha_bias	Shaper bias current.
11,12	pre_bias	Pre-amp bias current.
13,14	GND	Ground.
15	outm1	Negative differential analog signal board 1.
16	outp1	Positive differential analog signal board 1.
17	outm1	Negative differential analog signal board 2.
18	outp1	Positive differential analog signal board 2.
19	outm1	Negative differential analog signal board 3.
20	outp1	Positive differential analog signal board 3.
21	outm1	Negative differential analog signal board 4.
22	outp1	Positive differential analog signal board 4.
23	outm1	Negative differential analog signal board 5.
24	outp1	Positive differential analog signal board 5.
25	GND	Ground.
26	cal	Calibrate pulse to use in test mode.
27,28	test_on	Put the chip in test mode.
29,30	GND	Ground.
31	ckb	The readout clock signal.
32	ck	The inverted readout clock. (dummy).
33,34	GND	Ground.
35,36	VDD	Positive supply. (+2 V).
37	sib	Inverted read bit. (dummy).
38	si	Read bit to mux shift register.
39	VDD	Positive supply.
40	ther	Temperature measurement.
41	dresetb	Inverted digital reset. (dummy).
42	dreset	Digital reset.
43,44	VSS	Negative supply. (-2 V).
45,46	VSS	Negative supply.
47	holdb	Inverted hold of mux.
48	hold	Hold mux value. (dummy).
49,50	VSS	Negative supply.

Table 3.2: Signals on the board-to-board connector.

chip itself, and having such a plane in all three routing layers except for the ground plane. The three cooling planes are connected together with an array of 9 vias, to give an effective heat transport. The plane is biggest on the bottom side where most of the cooling will take place. In the bottom layer one must make sure that the plane is not covered by the solder stop to have optimal radiation and convection to the surrounding environmental gas.

Supply and grounding

The ground is provided as a full plane in the third layer from the top. This is a very low resistivity plane, helped by the fact that the inner layers of the PCB are made of thicker copper than the outer layers. On the input/output connectors 7 lines are allocated to ground, 6 to VSS and 3 to VDD. This reflects that most of the current is floating in the VSS supply. On the board itself the VSS routing between the input and output connectors are very fat, in order to minimize the voltage drop between the 5 boards of a cell. This is the only interesting voltage drop since the drop over the incoming cable can be compensated by adjusting up the VSS and VDD supplies in the readout-crate until ± 2 V is found on the the third board. This will ensure the two first boards having somewhat more than nominal supply and the two last ones slightly less. Several lines on the cable are allocated for the supplies, the purpose being shielding of digital and analogue signals from each other in addition to minimizing voltage drops and providing redundancy. Paralleling supply lines on the cable helps to reduce contact resistance in the cable to board connectors, which there are 9 of in a cell, further reducing voltage drops within the cell.

Signal lines

The most critical lines are the ones bringing the signals from the cathode pad input connectors to the chips. The noise is proportional to the capacitance seen by the inputs and several actions are taken to reduce this capacitance and to minimize pickup.

- The input lines should be well separated to avoid inter-channel capacitive couplings. Close to the chip this is not possible. Here the lowest distance allowed by the PCB technology is required, since the chip itself has an even smaller signal pitch, and a too wide angle fan-out is not possible with wedge bonding. Further from the chip the signal lines should be spread from each other.

- To minimize capacitive coupling to ground, the ground plane is placed as layer 3 of the board. It cannot go further down since the screening of inputs from digital lines constrains them to go in the bottom layer.

- The lines (especially from the cathode pads) should be kept as thin as possible to minimize pickup.

- The lines should be well shielded from the digital control signals, especially the hold and clock signals, which are active at the sampling time and during readout. The shielding is achieved by placing the board ground plane in between the input lines and the digital bus. The digital signals are also provided differential to reduce pick-up and common mode effects.

- The two 64-channel readout chips are organized to minimize the signal routing length from chip to the input cathode pad connectors. The position of the connectors is fixed by the layout of the cathode backplane G10 boards.

The prototyping revealed problems with over-etching of input lines, making automatic bonding very difficult since 4 mil lines ended up closer to 3 mil. The PCB vendor allowed 5 mil tracks and 3 mil spacing in the layout the last few millimeters of the input tracks. After production this gave bond pads of at least 4 mil width.

Figure 3.8 shows the evolution of the bond pattern around a chip from the first to the third version of the VA-RICH board. The first version had 3 mil bond pads and 3 mil spacing, whereas the third version had 5 mil tracks and 3 mil spacing. In the third run all bond pads are in addition widened wherever possible. These measures increase the bonding yield considerably. In fact the first version is not possible to bond automatic, whereas the third version is.

The layout of the VA-RICH board is found in figure 3.9 and figure 3.10, where the first figure shows the component placement, the solder stop layers and the drill (hole) information. The second figure shows the four electrical layers with the third plot from the top being the ground plane shown inverted.

3.3 The Belle SVD

The primary function of the SVD is vertex finding, even though it aids the tracking from the wire drift chamber. In the Belle experiment the vertex detector should be able to measure the distance between decay vertices along the beam axis of the produced b and $\overline{\mathrm{b}}$, when the pair decays into a CP-eigenstate. The reason is that this reveals the asymmetry in the proper time distribution in the decay, since $\Delta t \approx \Delta z / c\beta\gamma$, where $\beta\gamma$ is the Lorentz boost due to the asymmetric beam.

The inaccuracy in the time measurement smears the distribution, and it can be shown that a time resolution of $\Delta t/\tau = 1/2$ will require a 30% luminosity increase compared to perfect vertex reconstruction. The required luminosity will increase fast for even worse vertex reconstruction. With a time resolution of 1/2, the required vertex resolution along the beam axis is $95 - 100\,\mu$m.

3.3.1 Mechanical description of the Belle SVD

The SVD, see figure 3.11, is a three-layer cylindrical structure, built from double sided detectors (DSSD), from Hamamatsu Photonics (HPK). The readout electronics is sitting only at the ends of the cylinders, to minimize material within the Belle detector acceptance.

Each cylinder is built from a structure called a ladder, consisting of two, three or four DSSD's glued together in length and with a readout hybrid at each end. This results in ladders of three different lengths. All layers are built from ladders of the same width, consisting of 7, 10 and 13 ladders in the cylinders 1 (inner), 2 and 3, favoring the use of the same readout hybrid all over. The radii of the layers are approximately 30 mm, 43 mm and 57 mm, constrained on the inside by the beryllium beam pipe and on the outside by the CDC (wire drift chamber). The actual read-out unit will be of two types, short and long half-ladders. This since the middle and outer layers will have units consisting of two DSSDs

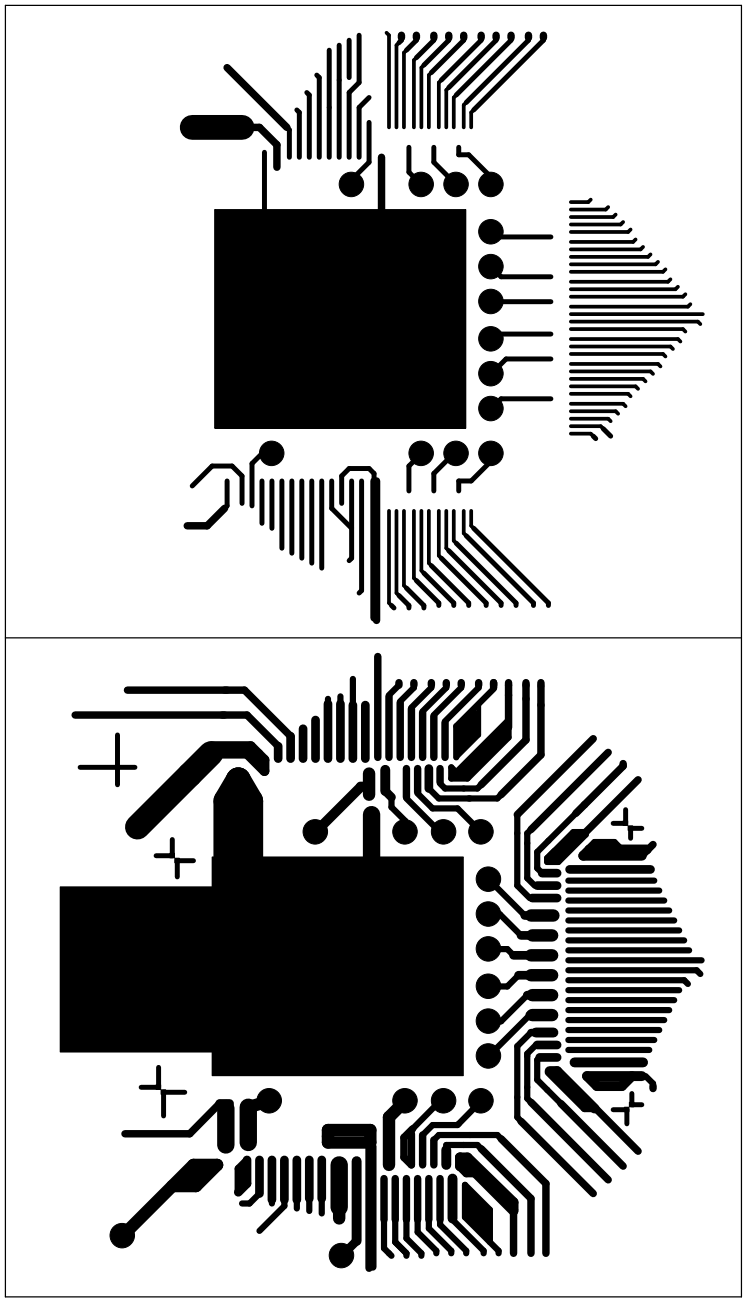


Figure 3.8: Evolution of bond pattern from VA-RICH board version 1 to version 3. The last version is possible to bond automatic, whereas the first is not. In the latter version also note the alignment crosses required by the bond machine.

glued and electrically connected together. This is shown in figure 3.12. The chosen scheme is to connect p-side to n-side and vice versa for the two DSSDs in the long half-ladders. This is similar to the DELPHI vertex detector. It has the advantage of removing some

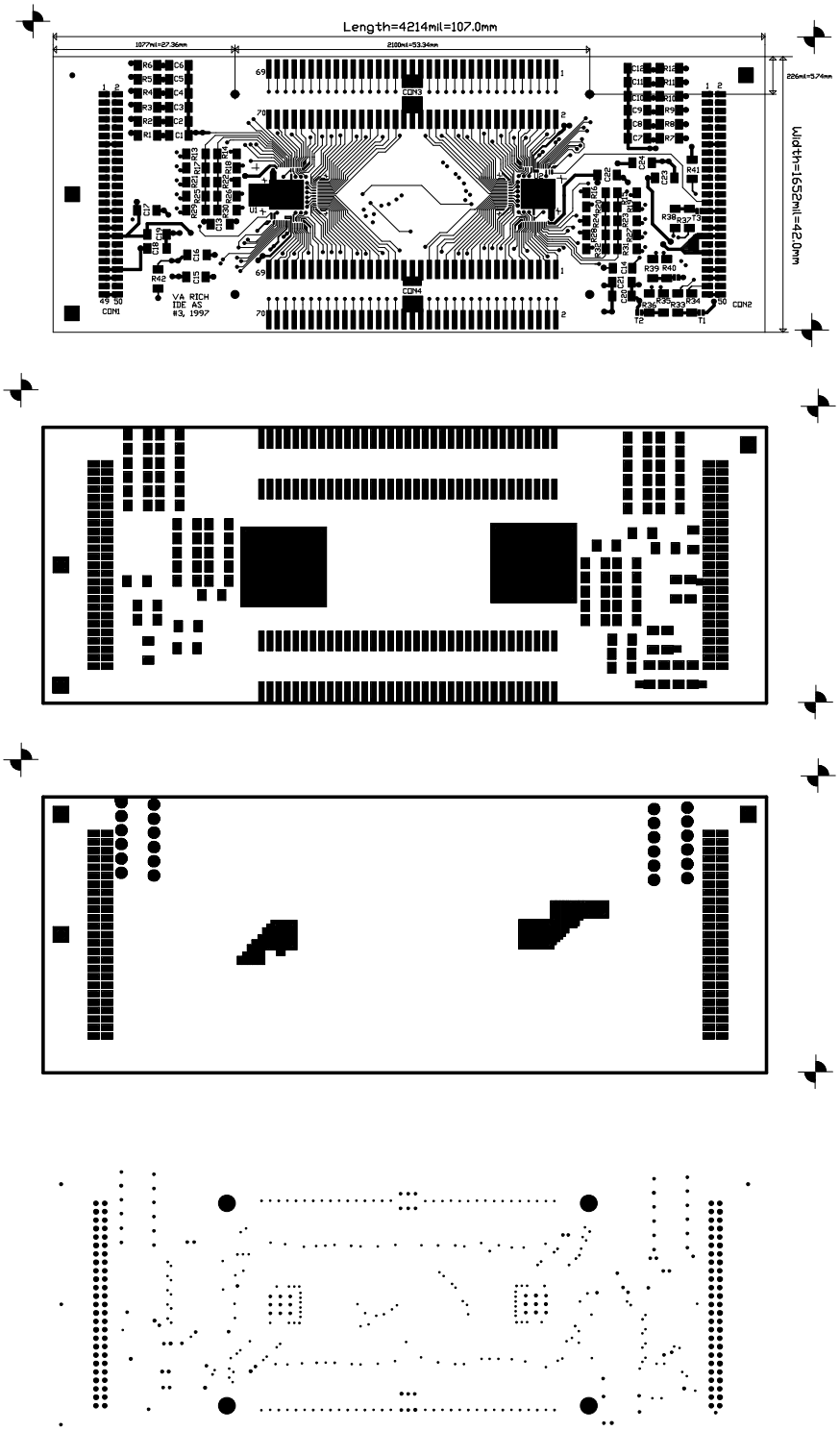


Figure 3.9: The component placement, the solder stop layers (top and bottom) and the drill file for the VA-RICH board.

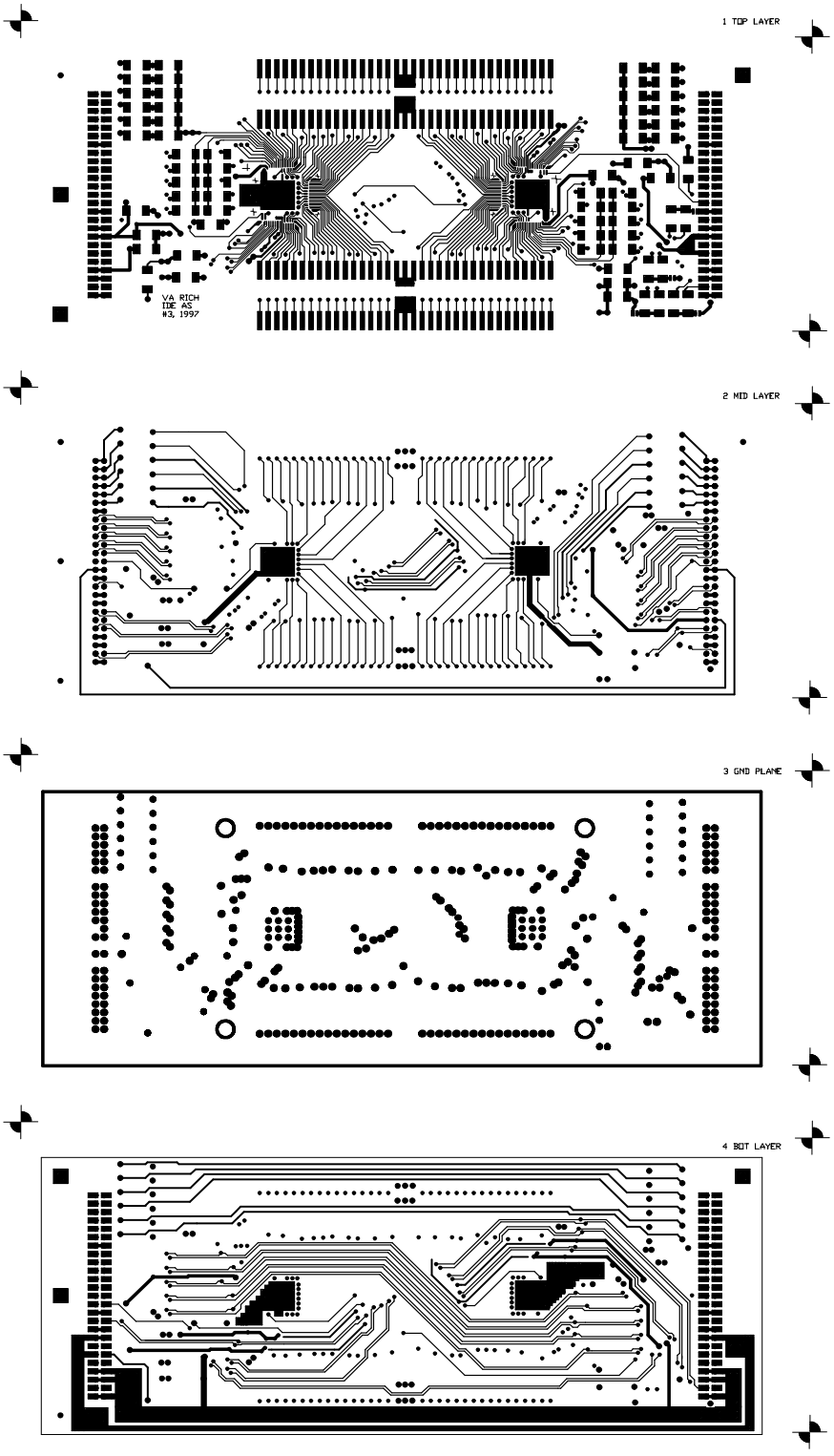


Figure 3.10: The layout of the four electrical layers of the VA-RICH board. From top to bottom.

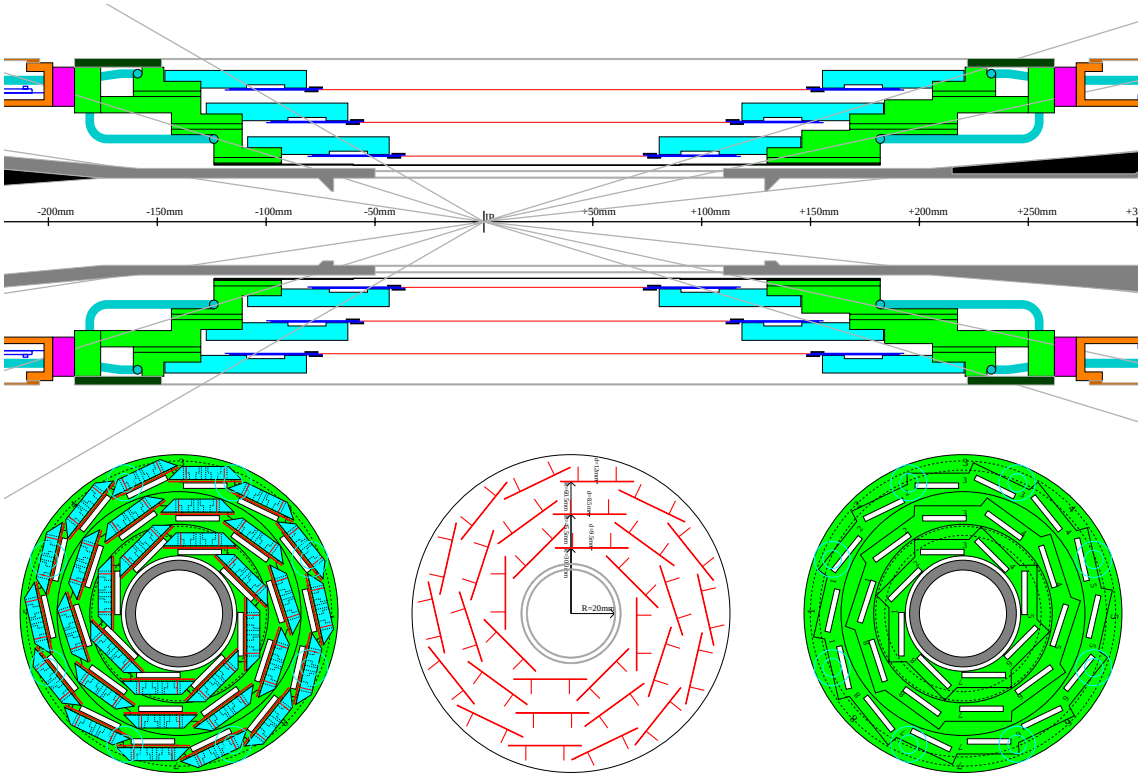


Figure 3.11: Axial and radial cut through the Belle SVD. Drawing by Y.Yamada, Belle.

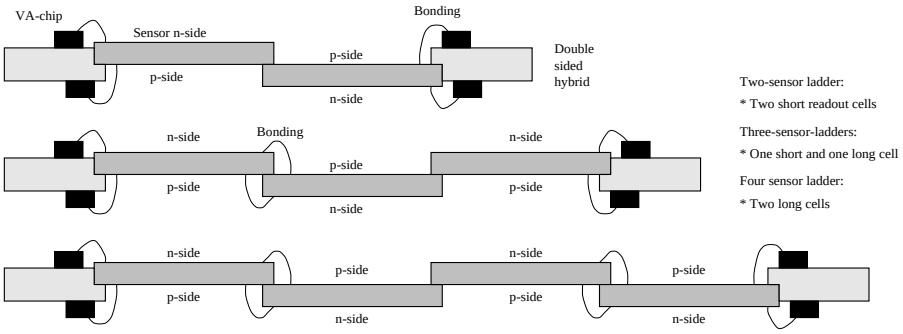


Figure 3.12: Configuration of short and long half ladders into full ladders for the SVD.

ambiguity, since the signals in one specific read-out channel will have different polarity for the first and second DSSD of the long half-ladder.

The Hamamatsu DSSDs to be used are of the double metal layer type described in chapter 1. It implies that the p-strips on the top side are to be connected directly to the readout electronics by bonding in the end of the short side. The n-strips on the bottom side are orthogonal to the p-strips, and a second metal-layer is used to route these strips so that they arrive on the short end where the readout sits. To shield the n-strips from each other a common p-stop is used in this detector. The detectors for the short half ladder

is approximately 33.5 mm by 57.5 mm. Since the readout pitch towards the VA-chips is 50 μm, this decides the readout p-strip pitch of the sensor. The average n-strip pitch is of course wider, since the detector is almost twice as long as wide. The n-strips will be routed out by the second metal layer to the short end where the chips force a 50 μm pitch. Typical capacitances for the detectors are 7 pF on the p-side and 22 pF on the n-side. The higher number is due two the extra line lengths and capacitive coupling between strips due to the double-metal routing. In the long half-ladders, which have two DSSD's with p on one DSSD connected to n on the other and vice versa, the capacitance of a strip is the sum, or 29 pF.

The Belle collaboration has measured the radiation effects of the VA1 chip [32]. Irradiation by γ-rays by ^{60}Co up to 200 krads show a more or less linear increase in the constant noise part and in the noise slope. The initial ENC in their measurement was given by $194e^- + 7.19e^-/\text{pF}$ growing to $429e^- + 22.1e^-/\text{pF}$ at 100 krad. The gain drop was found to be 0.3%/krad. To properly use cluster finding algorithms in the reconstruction, a signal-to-noise of 10 is needed [33, page 7]. Armed with the capacitance values for the DSSD's shown above, the long half ladders should be functioning up to about 150 krad with a S/N=12. In the case of the VA-RICH the radiation tolerance is not an issue. These are experiments with similar luminosities, but the SVD occupies the space a few centimeter from the interaction point whereas the RICH is situated a meter away.

The front-end boards have to drive the analogue signals about 2 m to the SVD control and repeater system (SVD-CORE) located behind the CDC end-cap wall. The SVD-CORE is connected to the readout crates by 30 m long cables.

3.3.2 The Belle VA1 readout boards

The VA1 chip is a 128-channel VA-chip, as opposed to the 64-channel VA-RICH. A few important differences in parameters and layout are found. The VA1 is made for read-out of large Si-strip detectors, with capacitive loads up to 100 pF. The design of the front-end is therefore concentrated on reducing the noise slope, which is 6.1 e^-/pF, sacrificing a little in the constant term, which is 165 e^-. In the VA-RICH chip which is optimized for a smaller capacitive load, the slope is higher, about 15 e^-/pF, but the constant term is only 100 e^-, which could have been even lower without the spark protection.

The input channels are organized in two rows on one side, to facilitate direct bonding to a 50 μm strip-detector. In VA-RICH they are spread around the available space, as to give the highest possible pitch, since wire-bonding towards a hybrid or PCB is needed, and typically 200 μm pitch is the minimum available in hybrid/PCB technology. The parameters of the VA1 chip was summarized in table 2.1 and its layout plot found in figure 2.3 of chapter 2.

The readout-boards, from now on called hybrids, incorporate five 128-channel VA1 chips on an area of approximately 43.0 mm by 33.5 mm. Two versions of these boards were made. The first consists of a two layered FR4 PCB glued on top of an AlN ceramic board, which contains only one electrical layer. It will later be referred to as the mixed hybrid. This is a very good structure, at least in the prototyping phase since it has a rather low

turnaround time of a few weeks, and the NRE cost is typically a factor of five below that of a thick film hybrid. The second hybrid was a thick film hybrid made in the Kyocera thick film process, later referred to as the pure hybrid. The technology is based on wolfram conductors on thin AlN ceramic laminates. These laminates are fused together at high temperature to give a multi layer hybrid. Each technology has different advantages, and this is reflected in the differences in the actual layouts.

The motivation for the more costly Kyocera solution was better thermal properties. Later simulations and measurements of the composite hybrid have shown these worries to be more or less unfounded. Reference [34] shows the results to be within acceptable limits for the composite hybrid.

3.3.3 Board schematic and components

The schematic of the hybrid is shown in figure 3.13. It can be seen that the active parts consist of 5 daisy-chained VA1-chips, to build a serially readout chain of 640 channels.

Due to the limited space available for each ladder, no component is allowed to be taller than 1.2 mm, greatly reducing possible connection schemes in the back end of the hybrid. Around 30 lines are required for all signals to the hybrid, and since only 18 mm width is available in the back end, less than 0.7 mm connector pitch is needed. The chosen connector is a 30-pin Omnetics nano-strip connector at 0.625 mm pitch.

The incoming connector brings only $\pm$2V and ground for the supply. On the hybrid close to the connector each of them are split into two branches. One branch is used to supply the analog part of all chips, the other branch has a little series resistor and is used to supply the digital part of the chips. Each branch is decoupled by an 1 μF capacitor (in the digital case, on the chip side of the series resistor). Filtering of the digital activity and separation towards the analogue part are obtained by the RC-combination.

Due to the limited amount of pins, only the critical digital signals, for the sampling and the readout clock are supplied differential. These are differentially terminated in 100 Ω. One will run with reduced digital swings of $\pm$1 V since this is sufficient for the chips, and it reduces the power dissipated in the terminating resistors to one fourth.

The two supplies are only given 1 pin each and ground uses 2 pins. In a more conservative design a 3-2-1 scheme for GND-VSS-VDD would be better in order to minimize voltage drops and total resistance in the supply leads.

If hybrids would be fitted with VA1RH, the radiation hard version, which has a much higher spread in parameters, separate shaper biasing would be necessary. At an early point also an additional seven-chip hybrid was foreseen, which required 7 lines allocated for the shaper biasing.

The capacitors for the test pulse are integrated in the PCB, by building a parallel plate capacitor by two squares fitted on top and bottom layers. These are in the 0.3 pF range, calculated by a parallel plate approximation.

Temperature monitoring is done by a single thermistor terminated to ground.

The supply for the silicon detector will have to go via the hybrid. Three lines are needed from a floating supply. The reference is connected to ground on the hybrid, the two other

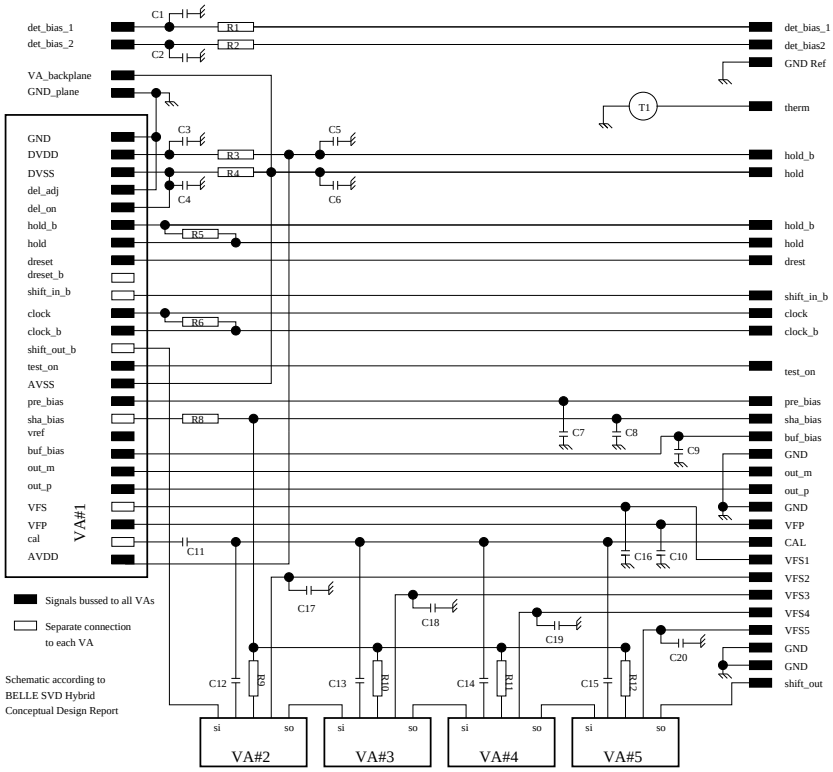


Figure 3.13: Schematic of the VA1 Belle readout boards defined by the Belle collaboration.

branches are decoupled to the reference on the hybrid. The two supply lines are brought to the front end of the hybrid, one on each side of the 5 chips, and are bonded to the supply for the p and n side of the DSSD. Three lines are needed because one does not want to put the full detector voltage of about 100 V over the oxide in the coupling capacitors on the n-side of the detector. Instead the p-side is biased at -20 V and the n-side at $+80$ V.

The component list is shown in table 3.4, and a description of the input connector is found in table 3.3.

3.3.4 The composite hybrid material and layout considerations

The AlN ceramic is 43.0 mm by 33.5 mm with a thickness of 0.38 mm. Typical cutting tolerance of the ceramic width and length is ± 0.075 mm, whereas the accuracy of the thickness is ± 0.025 mm. The placement of slots and holes are to a ± 0.050 mm precision. The manufacturer is American Technical Ceramics. The conducting layer is a thin film layer on top of the ceramic. This layer is covered by an 1 mil Dupont Pyralux PC, which is a polyimide insulating layer. The AlN material is chosen for several reasons; first its mechanical stability being a part of the DSSD support and alignment, and secondly its good heat conduction, which is the reason that the VA1-chips sit on the AlN and not on the PCB part of the composite hybrid.

The PCB has a designed size of 36.8 mm by 32.5 mm and a nominal thickness of

Pin	Signal	Type	Direction
1	hold_b	diff. dig.	In
2	hold	diff. dig.	In
3	shift_in_b	digital	In
4	clock	diff. dig.	In
5	clock_b	diff. dig.	In
6	dreset	digital	In
7	test_on	digital	In
8	Therm	analog	Out
9	GND	power	
10	out_p	diff. ana. current	Out
11	out_m	diff. ana. current	Out
12	GND	power	
13	VDD	power	
14	VSS	power	
15	CAL	analog pulse	In
16	sha_bias	analog bias	In
17	pre_bias	analog bias	In
18	buf_bias	analog bias	In
19	VFP	analog bias	In
20	VFS1	analog bias	In
21	VFS2	analog bias	In
22	VFS3	analog bias	In
23	VFS4	analog bias	In
24	VFS5	analog bias	In
25	VFS6	analog bias	In
26	shift_out	digital	Out
27	VFS7	analog bias	In
28	det_bias2	power	
29	det_bias1	power	
30	GNDref	analog	In

Table 3.3: Pin number and name of the signals on the output connector. Directions IN and OUT refer to the hybrid.

$300\,\mu$m $\pm$ $38\,\mu$m. Typical cutting tolerances are $\pm 127\,\mu$m. The manufacturer is KAM Circuits, England. The conducting material is $35\,\mu$m copper with a few micron of nickel before the gold finish, which facilitates bonding. The top layer is a 4 mil track and 4 mil spacing design, even though this is relaxed to 5 mil bond pads and 3 mil spacing to overcome bonding problems in case of over-etching of the PCB. The vias are 0.25 mm (10 mil) and the inner walls should be at least $35\,\mu$m metal. All areas except for bonding pads, cooling area and solder pads, are covered by a solder stop layer on both the top and bottom side.

Figure 3.14 shows the component placement and mechanical dimensions of the hybrid, whereas figure 3.15 shows the layout of all layers. The PCB covers most of the AlN except for the area where the chips sit. Figure 3.16 shows a side view cut through the hybrid. The pictures 3.17 and 3.18 shows the Kyocera hybrid and a half ladder based on this hybrid.

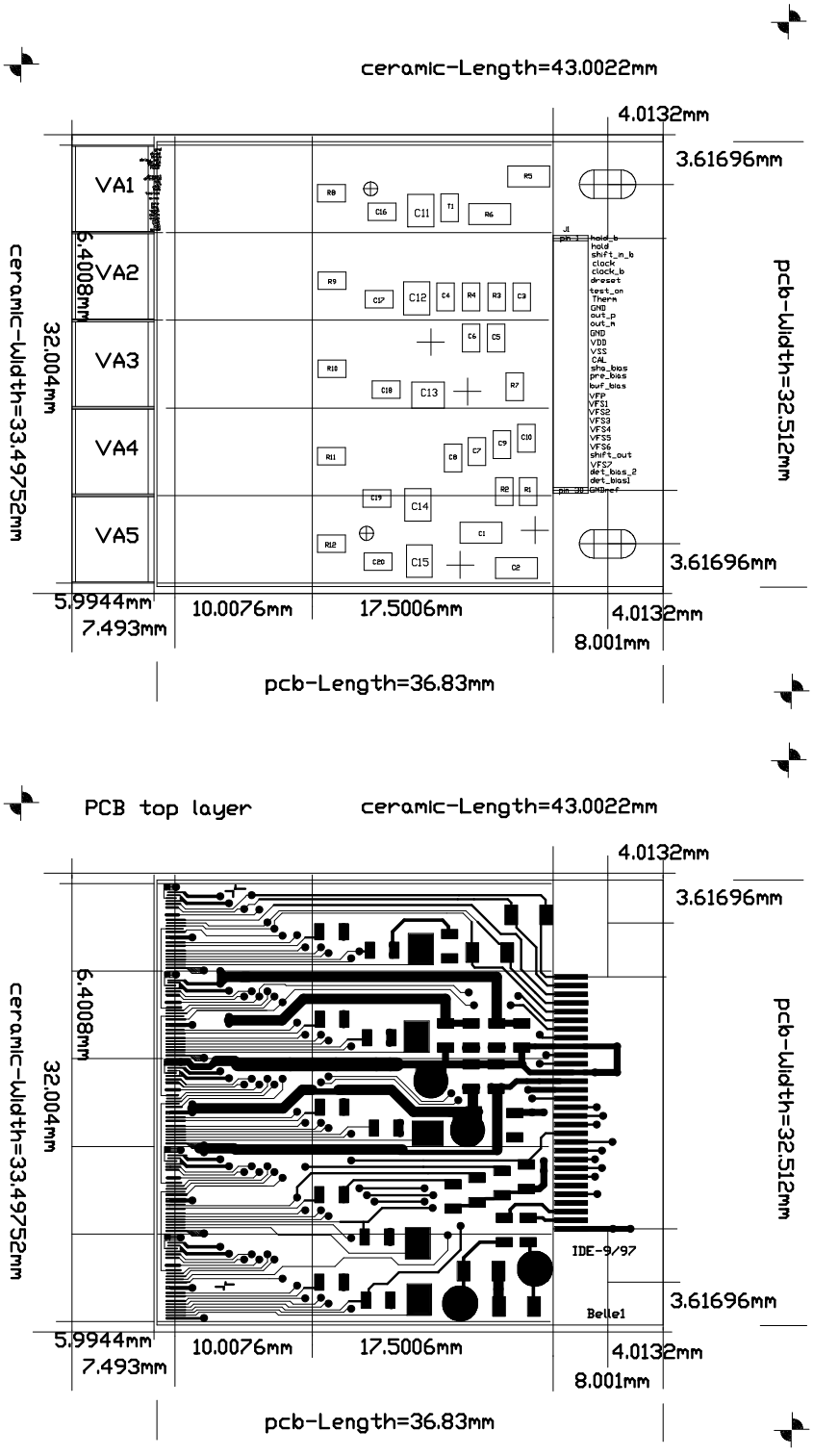
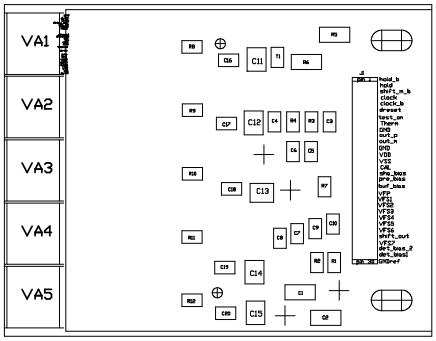
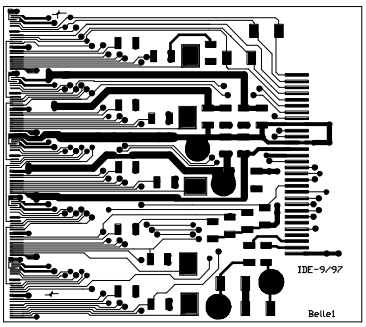


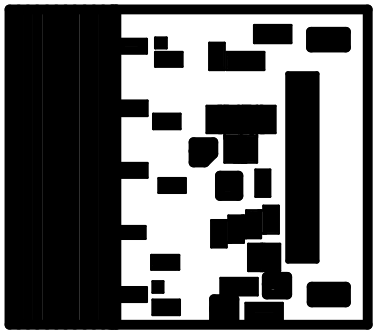
Figure 3.14: Belle composite (AlN/PCB) hybrid. Showing component placement and mechanical dimensions.



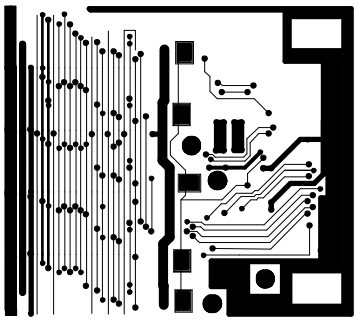
PCB top layer



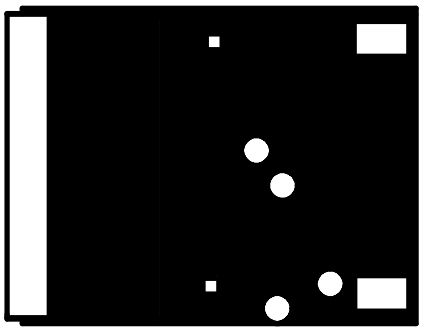
PCB solder stop



PCB bottom layer



Ceramic insulator



Ceramic conductor

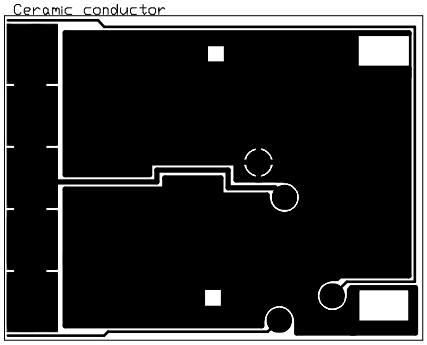


Figure 3.15: Belle composite (AlN/PCB) hybrid. Showing conducting and insulating layers.

Designation	Value/Rating	Size	Function
VA1-VA5	-	-	VA1 read-out chips.
J1	Connector	-	25 mil nano-strip 30 pin.
C1-C2	0.033μF 200V	1206	Detector bias decoupling.
C3-C6	1 μF	0805	Power supply decoupling.
C7-C10	1 μF	0805	VA bias line decoupling.
C11-C15	0.5pF	-	Integrated calibration capacitors.
C16-C20	1 μF	0805	VFS decoupling.
R1-R2	100KΩ	0805	Detector bias filter.
R3-R4	100Ω	0805	Series resistors digital supply.
R5-R6	100Ω 1/4 W	1206	Clock and hold termination.
R7	50Ω	0805	Calibration termination.
R8-R12	needs test	0805	RH1 shaper bias matching resistor.
T1	10KΩ	0805	Thermistor for temperature meas.

Table 3.4: Component list for the Belle read-out hybrids.

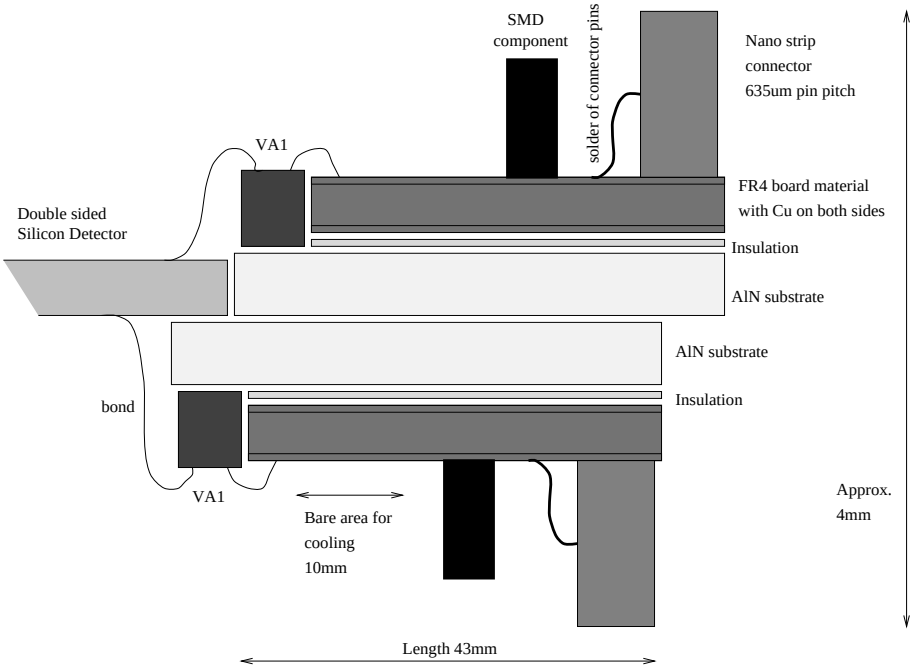


Figure 3.16: Cut through one end of a Belle SVD ladder. The figure shows the build up of the readout hybrids.

The heat removal will unfortunately have to go through a cooling bar, which has to sit on the PCB in a 10 mm wide area parallel to the chips. This area is the left 10 mm of the PCB, as can be seen in the upper plot of figure 3.14 and in figure 3.16. This is the reason why no components are found in this area, and that the solder stop layer for the PCB, one of the plots of figure 3.15, is withdrawn from the PCB in this area. The chip heat has thus to go through the AlN, and up through the insulator, the glue and the PCB, before it can

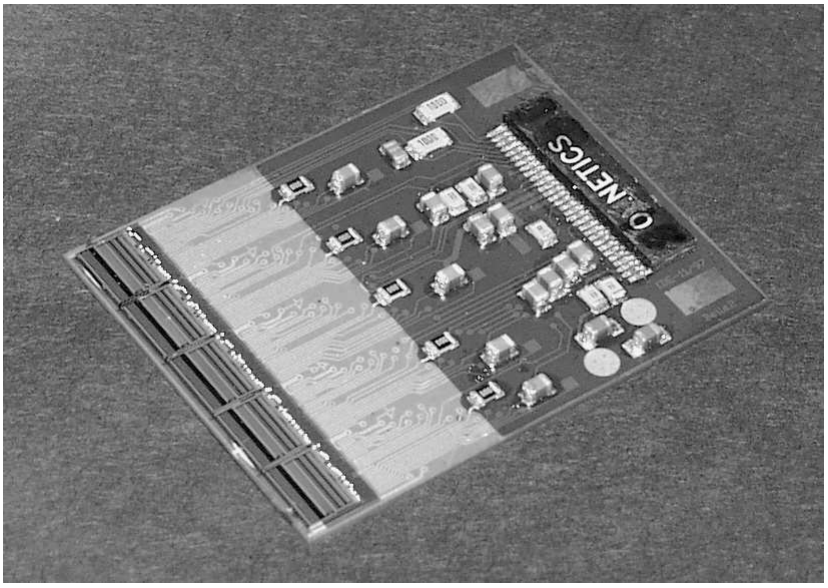


Figure 3.17: Picture of a Kyocera hybrid for the Belle SVD. Picture by Belle SVD group.

be removed. Care has been taken to minimize thickness of the insulator (the Pyralux) and the glue (provided as 25 μmm sheets that can be cut to the desired shape), and to find versions of these with high thermal conduction, such that the heat conduction will be good. The by far thickest element to interrupt the cooling path between AlN and the cooling pipe is the 300 μm PCB in FR4 (fiber-glass epoxy). It has a low thermal conductivity of about $0.35\,\mathrm{W/(m \cdot K)}$. This is substantially improved by introducing a lot of plated through vias in the 10 mm wide cooling area, which easily double the thermal conductivity [34].

All high current paths exist on the PCB, the ceramic conducting layer only routes the detector voltages, the VA backplane voltage and a ground for shielding purpose. This is due to the fact that the resistivity of the 35 μm Cu-traces is very low.

The few connections between the AlN electric layer and the PCB are through 2 mm holes in the PCB. Four such holes exist, for the two detector supplies, ground and the analogue -2 V for the chip backplane. Around the hole in the top layer is a metallized ring with the necessary electrical signal. By using a blob of solder, conducting glue or a bond, a connection is established from the top layer of the PCB down to the round gold pad on the AlN.

3.4 Realization of back-end readout in Cleo-III RICH and Belle SVD

In the B-physics experiments described, it is a common feature that the rate of interesting events is only of the order of $1 - 5$ kHz. This greatly simplifies the read-out electronics, because there is no need for front-end data buffering as in the case of the LHC experiments.

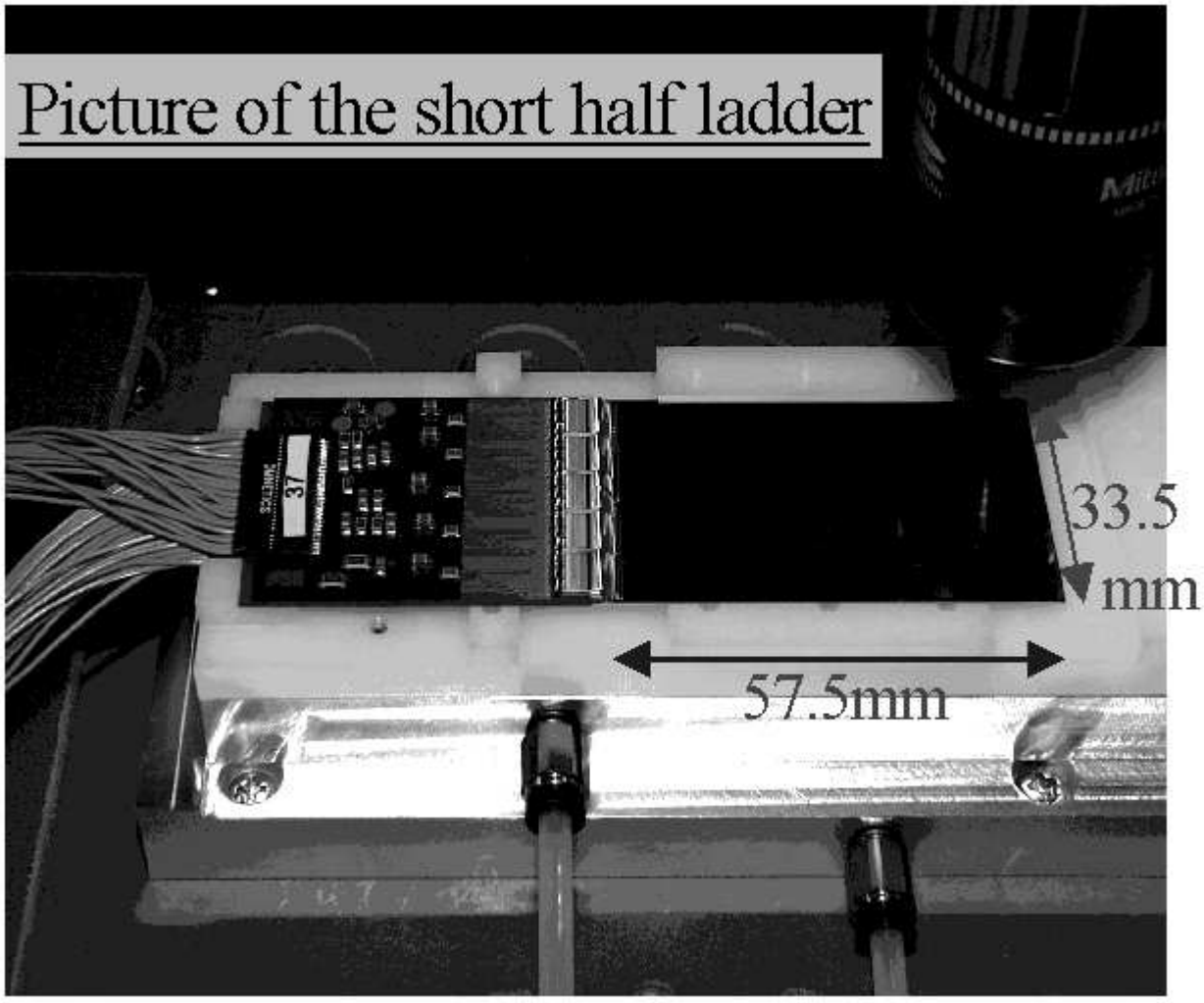


Figure 3.18: Picture of a Belle half-ladder inside an xy laser-test facility. Picture by Belle SVD group.

The acceptance of new triggers can be inhibited during the readout phase, provided the readout is fast.

The typical trigger latency in an experiment today is around $2\,\mu$s, which means that it will take this time to decide if the event is interesting or not. This decision is typically based on muon and calorimeter response, and is called a level-1 trigger. Higher level triggers are used to reduce the rate of events even more, but these occur at later stages. In addition is the typical hit rate for a channel in the B-experiments so low that there is very little chance of several hits in a channel within a $2\,\mu$s time window. This allows us to use slow shaping amplifiers, that will give the signal value (peak) of a channel just at the time when we know if the event was interesting, and we can use the trigger to issue the sample/hold for the front-end chips. It is in fact the slow shaping or rise time of the signal that is 'buffering' the data until we know if it should be read out.

The trigger rate gives about $200 - 1000\,\mu$s to read-out the front-end channels serially, which allows us to disable/inhibit the triggers arriving during the readout period without losing too many events. With typical serial read-out rates around 5 MHz it will take in the order of $130\,\mu$s to read-out a Belle hybrid. The longer the readout time is, at a given average trigger rate, the more dead time there will be. In Belle there is a requirement that no subsystems should inhibit the triggers for more than $200\,\mu$s to keep the dead time at an acceptable level, which is 10%. The back-end read-out systems are usually designed such as to add no extra dead time.

3.5 VA1 chip statistics

The statistics from wafer and board testing of VA1 chips for the Belle experiment is summarized here. Typical values for the most important chip parameters: pedestals, gains and noise are presented. The conclusion is that the result of the wafer testing can be trusted and furthermore that the noise characteristics of the chips when probed on a wafer are comparable to the noise of finished hybrids. It is found that the pedestal pattern of a chip is as distinct as a finger print and can be used in the process of identifying the exact chips from a wafer that are used for a hybrid. This is used as a test of the logistics and book-keeping involved in the manual process of wafer testing and putting chips on specific boards.

The basis for the analysis is 120 Belle Kyocera hybrids, each containing 5 VA1 chips. All chips were taken from a total of 8 wafers. In the mounting of the boards, only chips with all 128 channels fully functional were used. In the wafer-testing a total of 821 chips are used. When comparing results between wafers and boards the material is 545 chips on 109 boards, mainly because the remaining boards have one or more chips where there are problems with the logistics such as missing data-sheets or similar.

3.5.1 Wafer testing and yield

The wafers are pre-tested at delivery from AMS and some chips are marked as bad. The probe testing only tests those chips that passed the pre-testing. For the 8 wafers used in this analysis, the table below summaries the number of bad channels. The most important criteria are pedestals and gains. The gain for each channel should be inside a $\pm 30\%$ range around the mean for a large set of chips, and the pedestal spread should be inside a $\pm 20\%$ band of the total output range. The noise cut is set at 500 electrons. The fraction of accepted chips is around 84% after the probe testing. This means that mounting a 5 chip hybrid without probe testing would give only $0.85^5 = 0.42$, or in the order of 40%, working boards without need for chip replacement. In the last batch of 80 Belle boards only two boards needed rework due to chip problems. This is about $97 - 98\%$ board yield after probe-testing. The most common rework problem encountered was due to channels killed in the mounting by ESD, and can of course not be attributed to the cuts set in the probe testing.

Wafer	0 bad channels	1 bad channel	2 bad channels	More than 2	Total chips	0 bad fraction (%)
W18	94	1	0	25	120	78.3
W22	70	5	2	20	97	72.2
W28	65	5	1	6	77	84.4
W30	104	3	0	2	109	95.4
W31	86	7	2	8	103	83.5
W32	88	2	1	6	97	90.7
W33	98	5	3	4	110	89.1
W34	83	12	0	13	108	76.9
Total	688	40	9	84	821	83.8

Table 3.5: VA1 wafer yield

3.5.2 Pedestal statistics

When looking at the pedestal spread the numbers should be normalized to a fraction of the full chip output range. This is motivated by the fact that all channels are to be sampled by the same ADC with a certain input range. We do not want to lose resolution due to the pedestal spread occupying a large fraction of the ADC input range.

The chip output is a differential current and the total swing is 10 times the ibuf-current. For the selected operating current of 200 μA for Belle, (140 μA nominal) the chip output range is 2 mA. The test system will convert this to a voltage using 3.3 kΩ resistors, giving a range of $\pm$3300 mV, which is a normalized $\pm$50% range. A good chip should have a average pedestal close to zero.

The average pedestal of the chips (based on all 545 wafer tested chips) is -0.60%, shown in the upper plot of figure 3.19.

For the internal spread in the pedestals of a chip, the standard deviation, σ, and range, R, are used to quantify the spread. R is the difference between the two channels with maximum and minimum pedestal value. It is found that the standard deviation of the pedestal values of a chip is 0.47%. The average range for all the tested chips is 2.37%. Figure 3.20 shows both σ and R after normalizing to the percentage values of the full range. Note that the distributions of these are not Gaussian, but if the natural logarithms of σ and R are plotted, they are more or less Gaussian.

The exercise is repeated for all the 545 chips after they are mounted giving similar results. The raw average pedestal data from both wafer and board testing is found in the two lower plots of figure 3.19 to illustrate the similarity between wafer and board testing. The σ and R show similar good correlation. An even better illustration is figure 3.21 showing the correlation plot between the average pedestal value of a chip measured on wafer and then later on the board. A very good correlation is found. The pedestal values of a chip are in fact so unique that they can be used as a fingerprint in mapping what specific chip from all of the tested wafers, was mounted at a specific position on one of the boards.

To match chips from board and wafer testing a simple correlation based on an inner

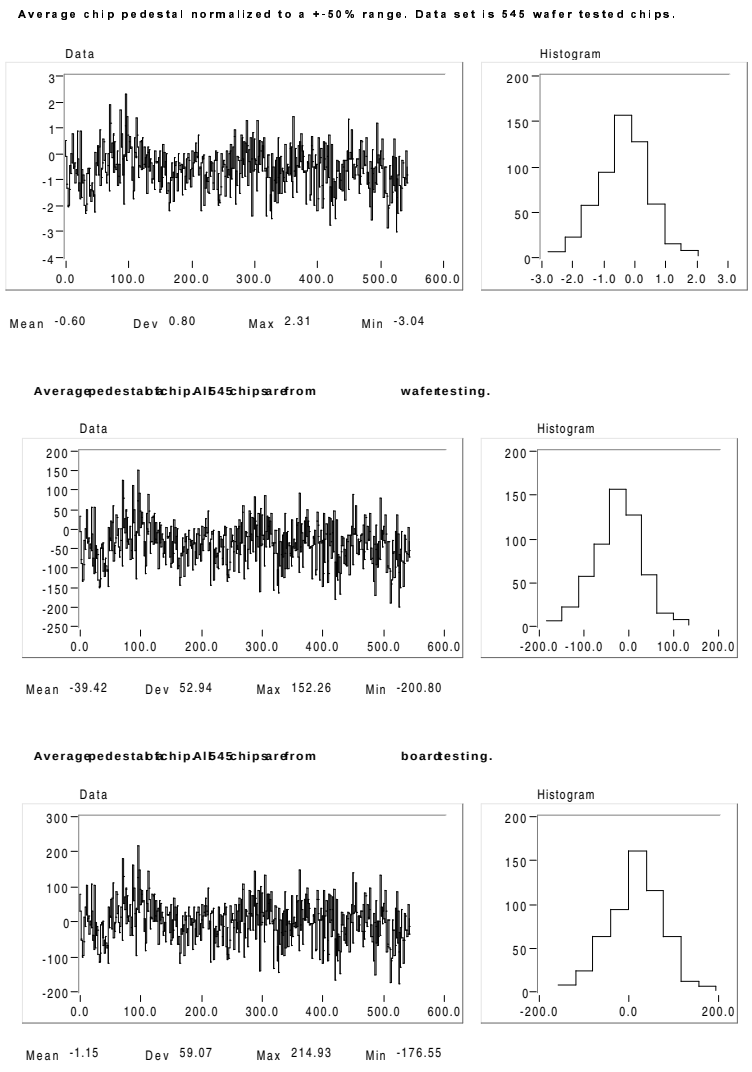


Figure 3.19: Average pedestal value for 545 VA1-chips. Measured both on wafer (mid plot, in mV) and on finished boards (bottom plot, in mV). The upper plot shows the wafer result but normalized to full chip output range so that the full Y-axis span the possible range -50% to $+50\%$.

product is used. The pedestal pattern (or a fraction of it containing N channels) of a chip after subtracting the DC-value (the mean of all pedestals) is regarded as a N-dimensional vector ($\vec{P}$). The vector is normalized to a length of 1, $\vec{p} = \vec{P}/|\vec{P}|$, and the inner product taken as $c = \vec{p}_w \cdot \vec{p}_b$, where the subscripts indicate the vector for the wafer or board measurement. The result is a number between -1 and 1, where 1 indicates a complete match of pedestals (ignoring DC shifts). Figure 3.22 shows as the upper plot the inner product between a chip on a specific board towards all fully good chips on all wafers. In fact the robustness of the method is not easily seen by the upper plot, since the chips with

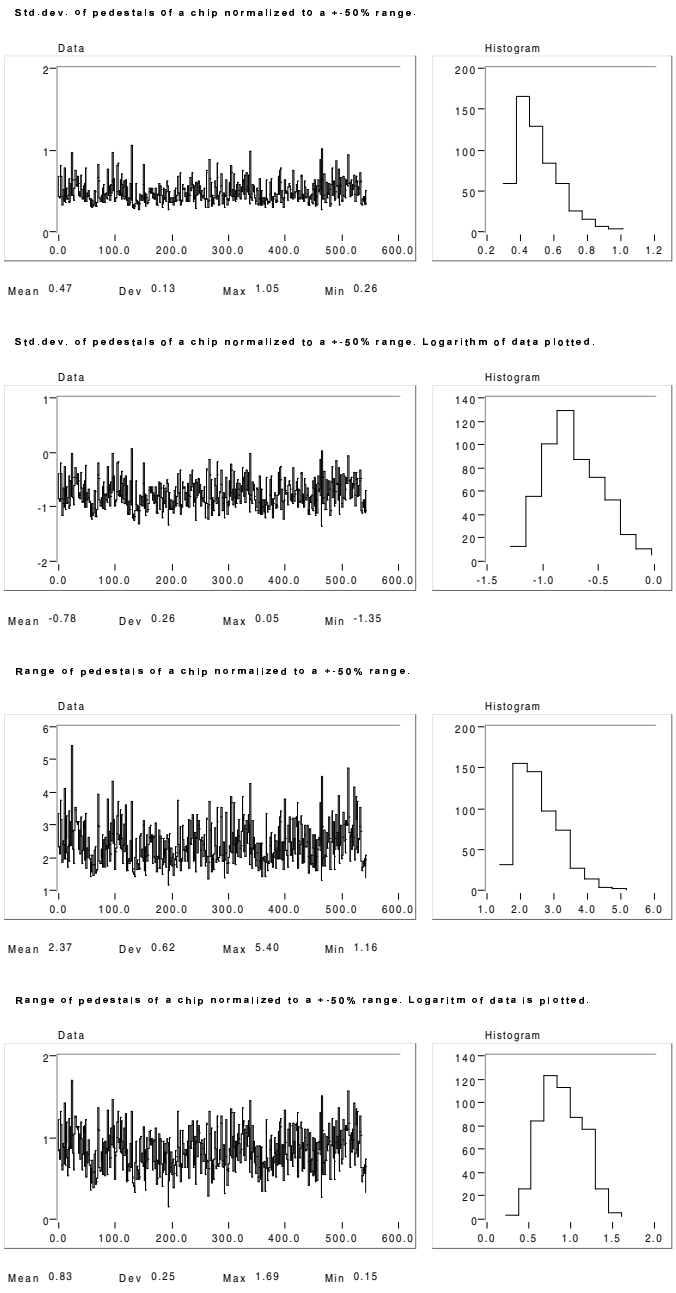


Figure 3.20: The standard deviation and range of pedestals (inside a chip) for all 545 chips. Both the distribution and the distribution of the logarithm are shown for the standard deviation and range

inner product of about 0.7 instead of very close to 1 could be thought of as pretty good matches, which they are not. The lower plot instead shows $1/(1-c)$, since this gives a scale that favorises cross products close to 1 with a distinct peak, more reflecting the relative

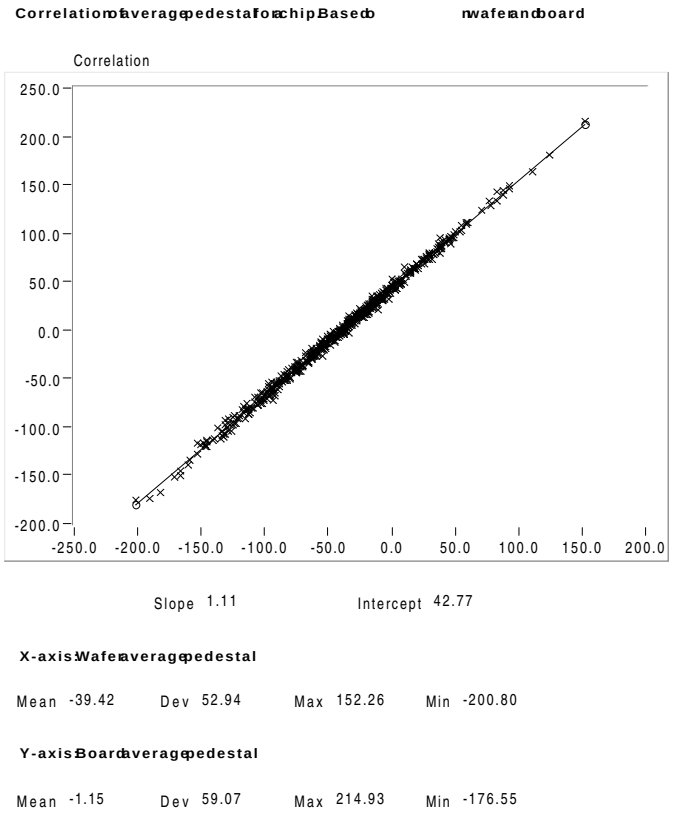


Figure 3.21: Average pedestal correlation between chips on wafer and board.

strengths of the possible matches. This is done for visualization purpose only.

Figure 3.23 shows the pedestal pattern of a specific chip before and after mounting on a board. The same characteristic pattern is found. The figure also shows the difference between the two patterns, and this reveals a typical characteristic. The difference is not zero but a linear function of the channel number added to a small fraction of the pedestal pattern itself. The slope and intercept of this line are found more or less to be the same for all chips. This effect is understood. The chips have been tested with slightly different VSS supply voltage. This gives a slightly different gain in the two cases, explaining the small fraction of the pedestal pattern in the difference. The slope is due to the different current consumption giving a slightly different sagging in the internal VSS bus of the chip.

3.5.3 Gain statistics

The gain of a channel is measured as the first derivative of the signal profile at zero input charge. For a charge sensitive amplifier, like the VA chip, delivering a current output, the proper unit for the gain would be μA/fC. The VA-DAQ setup uses a step voltage to inject

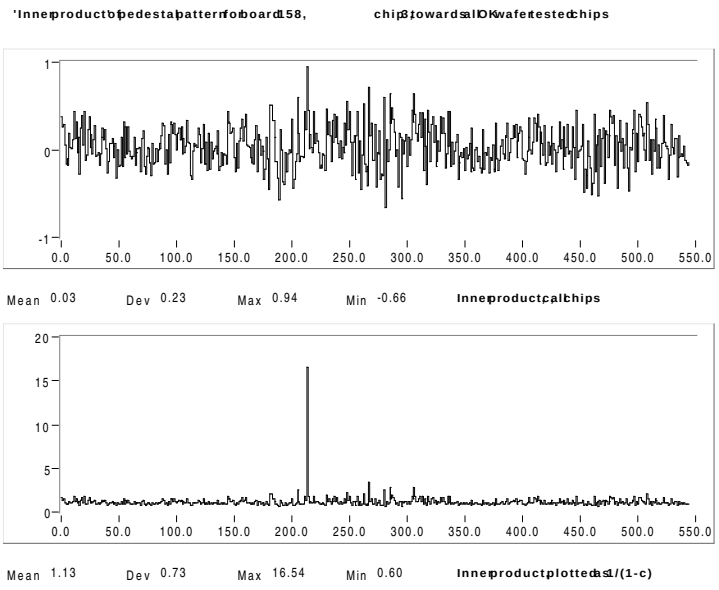


Figure 3.22: Matching of a chip on a board to all wafer tested chips.

the charge through a capacitor, with the capacitor not being known to good accuracy. In addition is the differential output current of the chip converted to a single ended voltage with a trans-impedance amplifier, since the ADC accepts a single ended voltage. The gain is therefore more easily measured in mV/mV (no unit), with the nominator mV indicating the ADC input voltage and the denominator mV indicating the size of the step voltage used to inject a charge.

The relation between the chip differential current signal, I_{sig}, and the voltage into the ADC, V_{ADC} is given by $V_{ADC} = RI_{sig}$, where R is the resistance in the trans-impedance amplifier. The VA-DAQ system uses $R = 3.3\,\mathrm{k}\Omega$. The relation between the input charge to the chip, Q, and the voltage step, V_{step}, applied to the test capacitor, C, is $Q = CV_{step}$. The gain measured in mV/mV, $G_V = V_{ADC}/V_{step}$, is related to the actual chip gain $G = I_{sig}/Q$ (measured in μA/fC) by the relation $G = G_V/(RC)$.

When chips are tested on a wafer the capacitor is mounted on the probe card and will be the same for all the tested chips as long as the probe card is not changed. The typical capacitor used is 1.8 pF. If the same VA-DAQ is used for the wafer testing, also the R will be the same, and the product RC will be constant for all the tested chips. G_V is given to a better precision than G, as long as the C is not accurately known. Most often is the spread in gain as a fraction of an average gain the important parameter, and in this case will of course a fraction between two G_V numbers have the same precision as the fraction between two G numbers.

The average gain of the wafer tested chips both before and after mounting is given in figure 3.24. On the wafer testing the average gain is 106.4 ± 4.6, the standard deviation being 4.3% of the average. On the board testing the standard deviation contributes 11.6%

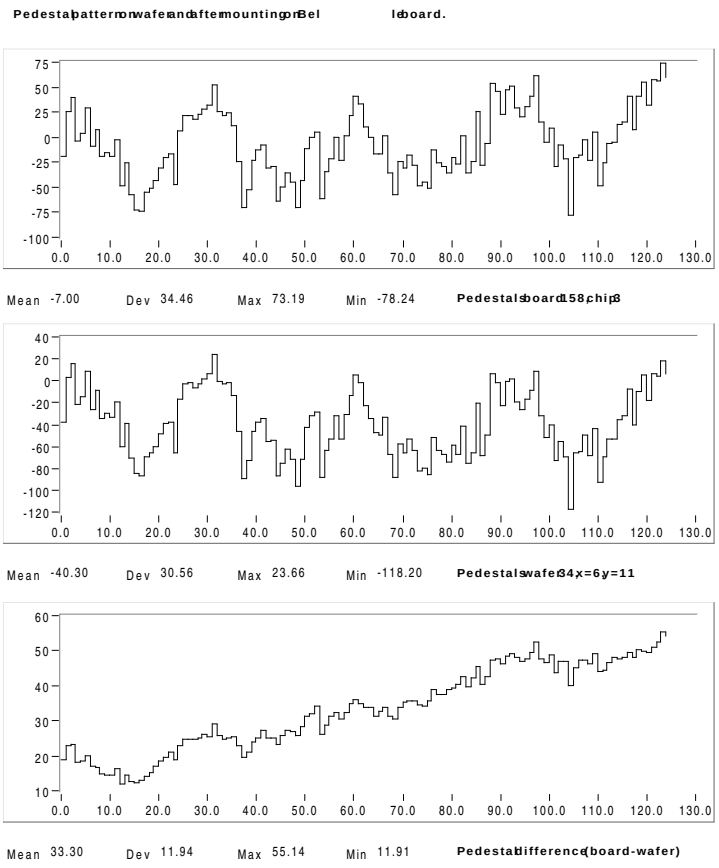


Figure 3.23: Pedestal patterns of a chip on wafer and after mounting on a board.

(2.22/19.09). This is due to the fact that on the board testing a separate capacitor is used to pulse each chip, and that there is a certain spread in the value of this capacitor. If we assume the capacitor on the probe testing to be 1.8 pF to a good precision, the integrated capacitors used for each chip on the Belle boards will have an average value of $\frac{19.09}{106.38} \cdot 1.8\,\mathrm{pF} = 0.32\,\mathrm{pF}$, where the fraction is the average gain for the chip measured on the board divided by the same measured on the wafer.

In fact, we can estimate the spread in the integrated board capacitors if we assume its spread as well as the spread in the gain to be Gaussian. The spread in gain measured on a board (11.6%) should in the Gaussian case be a square sum of the spread as it was measured on the wafer (4.3%) and the spread in the capacitor value (unknown). The calculation reveals the spread in the capacitors to be 10.8%.

It is possible to do better than this and for each chip plot the actual fraction between average chip gain measured on wafer and on the board, as it is done in figure 3.25. This figure indicates the average fraction to be 5.64, compared to the division of the total averages of all chips before and after mounting, which is 106.38/19.09 = 5.57. The figure also shows the standard deviation to be 0.60, which is 10.6%. The fact that the two

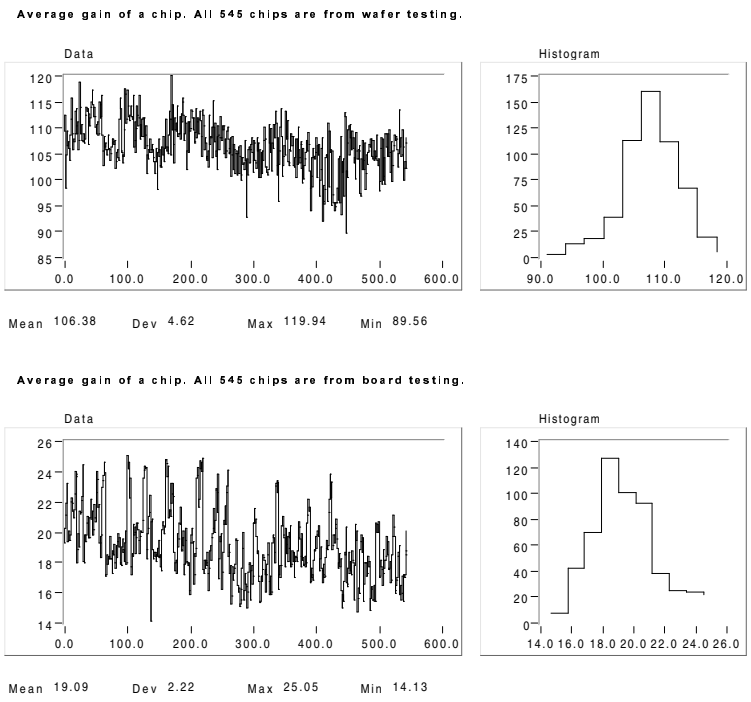


Figure 3.24: Average gain value for 545 VA1-chips. Measured both on wafer and on finished boards.

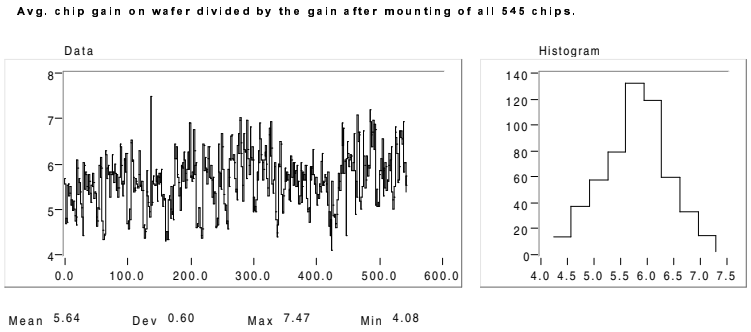


Figure 3.25: Fraction between average chip gain on wafer and on board for 545 chip. Can be interpreted as the fraction between the fixed probe card capacitor and the separate capacitor for each chip on a board.

alternative calculations give the same result, a spread of about 11% in the capacitor value, confirms the Gaussian assumption, as we already know by looking at the histograms in figure 3.24 and figure 3.25.

So far we have only been looking at the average gain of chips, however it is also interesting to look at the spread within a chip. This is done in figure 3.26. It shows the standard

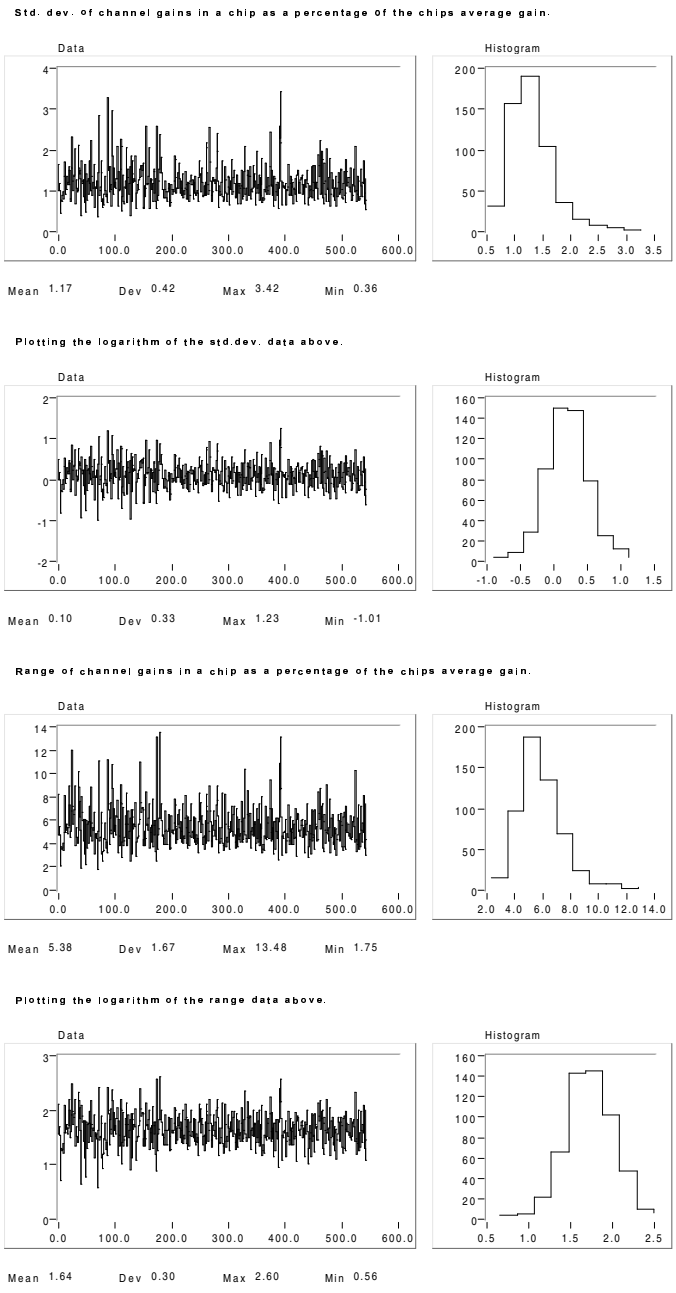


Figure 3.26: Standard deviation and range of gain for all channels of a chip, measured as a percentage of the average gain in the same chip.

deviation and range of channel gains in a chip, for all the 545 chips. Both quantities are measured as a percentage of the average gain of all chips. Both plots use chip data from the board testing. Also the natural logarithm of the measured quantities are shown, indicating that the distribution of the logarithm is the one closest to a Gaussian. The average σ and

R for the gain are 1.2% and 5.4%.

The motivation for using data based on board testing in the standard deviation and range statistics is that the board testing is much more accurate than the wafer testing. The gain measurement is done with the chip in test mode, making it much more susceptible to pick-up noise and generated feedback via the enabled calibration input. In the probe setup all traces are much longer and the input (calibration) is not very well shielded from the output. By using the **Signal profile** of VA-DAQ one can show the accuracy of the gain measurement of a channel to be around 0.25% for board testing, and around 2.5% for the wafer testing. One could think that the latter number swamps the average gain results above, which is not the case, since a 2.5% channel gain measurement accuracy is reduced to a $2.5\%/(128)^{1/2} \approx 0.2\%$ accuracy in the average gain measurement value of a 128 channel chip. This 0.2% effect does not have any influence on the average gain calculations where the spreads are in the 5% order or larger, at least not in a Gaussian world where the inaccuracies add in quadrature. An 0.2% term added in quadrature to a 5% term is essentially 5% (5.004%).

3.5.4 Noise statistics

The average chip noise was measured both in the wafer testing and for each chip on the boards. The results are given as an equivalent input charge (ENC) in electrons. The raw noise measured is for each channel a noise voltage into the ADC. By dividing by the channel gain in mV/mV, the number can be thought of as an equivalent input step noise voltage, to be pulsed on the step capacitor. By using $Q = CV$, where Q is charge, C the test capacitor and V the step voltage, the equivalent noise charge Q is found in fC. This is easily converted into a number of electrons, since the elementary charge corresponds to about $1.6 \cdot 10^{-4}$ fC.

For the wafer measurements the capacitor is the same for all chips, and assumed to be 1.8 pF. The board results are different, since the logged data all have assumed a value of about 0.3 pF, and not the real value of the capacitor. The noise results for the boards should for each chip be scaled by a fraction of the real capacitor value over the assumed 0.3 pF. The previous section in fact used the gain measurements from wafer and boards to find the fraction between the test board capacitor and the board capacitors. Since we know the test board capacitor to be constant and 1.8 pF, the board capacitors are easily calculated. Figure 3.27 shows two plots, both being correlations between the average chip noise based on wafer and board measurements. The first plot is before the correction of the board data by using the real capacitor value, the second plot shows the correlation after this correction. After the correction the correlation is improved, which is also a support for the validity of the board capacitor calculations in the gain statistics section.

Figure 3.28 shows the results of the noise measurements for wafer and board testing. The results are better on the wafer testing, around $195e^-$ due to a better value of the vfp-voltage, which lowers the noise. This is a feature of the VA-DAQ test system. In both wafer and board testing it will force the same bias values (as given by a definition file) onto the tested chips, but the monitoring of the actual voltages and currents are done on

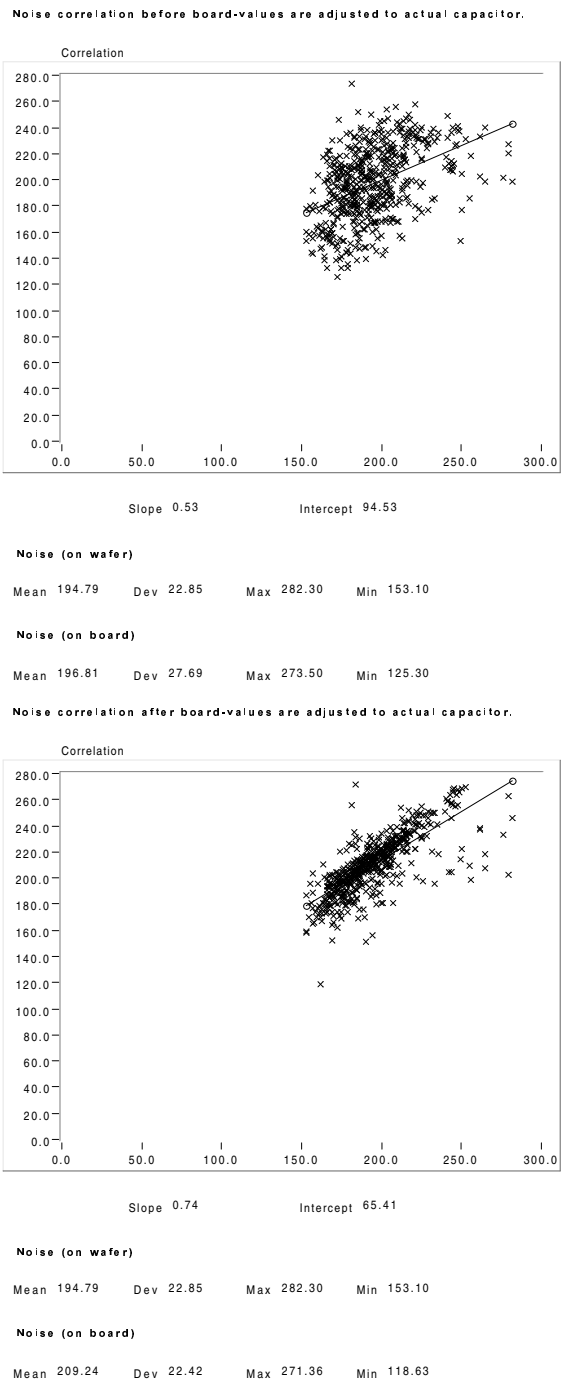


Figure 3.27: Correlation of average chip noise from wafer and board testing. First plot before capacitor correction, and second plot after the correction.

the VA-DAQ system, and not on the unit under test. Due to voltage drops over cables, the effective bias voltages at the chip level can be slightly different. In case one wanted to

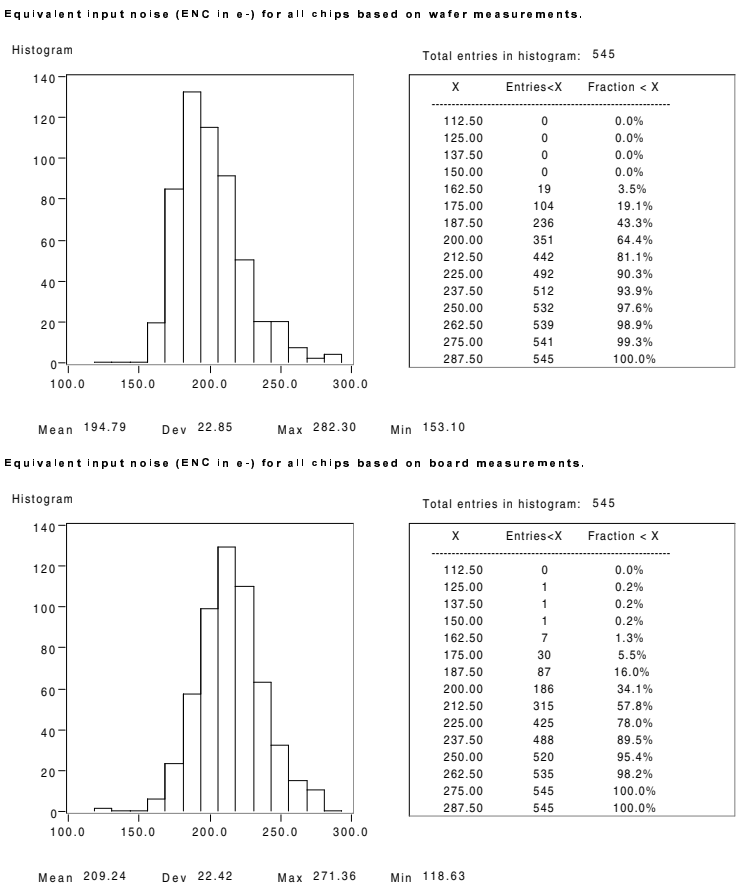


Figure 3.28: Noise measurements for wafer and board tested chips. The result as an equivalent input charge in electrons.

assure exact same testing conditions, one should adjust the biases until the values at the chip are identical. This would give two different sets (definition files) of bias voltages to apply to VA-DAQ for wafer and board testing.

In addition are bias settings optimized to stretch the peaking time towards 2.5 μs, and not to minimize noise. The best obtainable results with VA1 is about 165e$^-$.

3.5.5 Conclusion of VA1 statistics

In the process of making a board one could argue that it is only the internal spread of a chip that matters, since one could bin together chips with more or less the same average gain. This will be sufficient when the user is not very interested in the absolute value of the gain, but only the spread, which is typically the case.

To bin together chips that have approximately the same average pedestal and gain will of course increase the amount of logistics and handling during the selection phase of chips for a board. If it turns out that the internal spread in gain and pedestals of a chip is much

larger than the chip to chip spread, it would of course not pay off to do this binning.

The pedestal statistics is summarized in figure 3.29. It contains three plots. The first shows the spread in the average pedestal of all the chips as a fraction of the total output range. The distribution is more or less Gaussian, with $\sigma = 0.8\%$. The average DC value is slightly offset from zero. This small offset has in fact no meaning, since the DC level can be shifted to zero in the trans-impedance amplifier. This is done in the second plot of the figure. The third plot shows the distribution of range in the chips, and the accompanying table shows the fraction of chips with the range below a certain threshold. It is immediately observed that for 99% of the chips the total range is 4% or below. This is comparable to the spread in the average, where 99% of the chips are within $\pm 2\%$ of the average. The implication is that binning chips in groups after the average pedestal has a function, since it will reduce the spread on a mounted board by roughly $\sqrt{2}$.

For the gain the summarizing figure 3.30 shows as the first plot the average gain in a chip, measured as mV/mV. Using the average value of 106.4 mV/mV it is easily calculated that the average gain is 17.9 μA/fC. The second plot shows the same plot, but normalized such that the average for all 545 chips is 100%. The distribution is Gaussian, with a standard deviation of 4.4%, and 96% of the chips within $\pm 10\%$ of the average. The third plot shows the distribution of the range. For 98% of the chips are the gain range below 10% of the chip average, indicating half the chip to chip spread. This is an even stronger motivation for binning chips.

Figure 3.31 shows the average pedestal and gain over one wafer. White indicates that no chip is in the specific position on the wafer. It is seen that the VA1 chips occupy double rows on the wafer, with single rows in between. These are multi-chip wafers, with the single rows interleaved being VA2 chips. The maps show that the pedestal and gain usually vary little for neighboring chips. This implies that if binning of chips is not found worthwhile, it will often help a lot on the spread of a finished board, that the chips are selected as neighbours on the wafer.

Even with little effort in optimizing vfp for low noise, the conclusion of the noise measurements is encouraging. Average noise values of $195e^-$ on wafer testing with non-ideal biasing, for a VA chip with an estimated minimum of $165e^-$, are very good. It indicates that there should be no problems in measuring valid noise data with the current probe station setup. For chip testing in test mode, where feed-back starts to be a problem, it is seen that much more averaging is needed for the probe testing compared to the board testing, to get results of similar accuracy. By using better shielded probe cards and decoupling closer to the probed chip, this can probably be improved.

The book-keeping of which chips from a wafer goes to a specific place on a board was found to contain several errors. These were detected by using the pedestal fingerprint. On 118 boards 26 clear map errors were found. About 20% of these are with data sheet files, where the test person has either selected a wrong board number or a wrong wafer position when writing the result of the test to file. The rest of the errors are in placing chips from the wafer on the board. There are two such common errors. The position of chips on the board are mirrored compared to the map, compatible by holding either the board or the map upside down when writing down the position. The other error is one-off

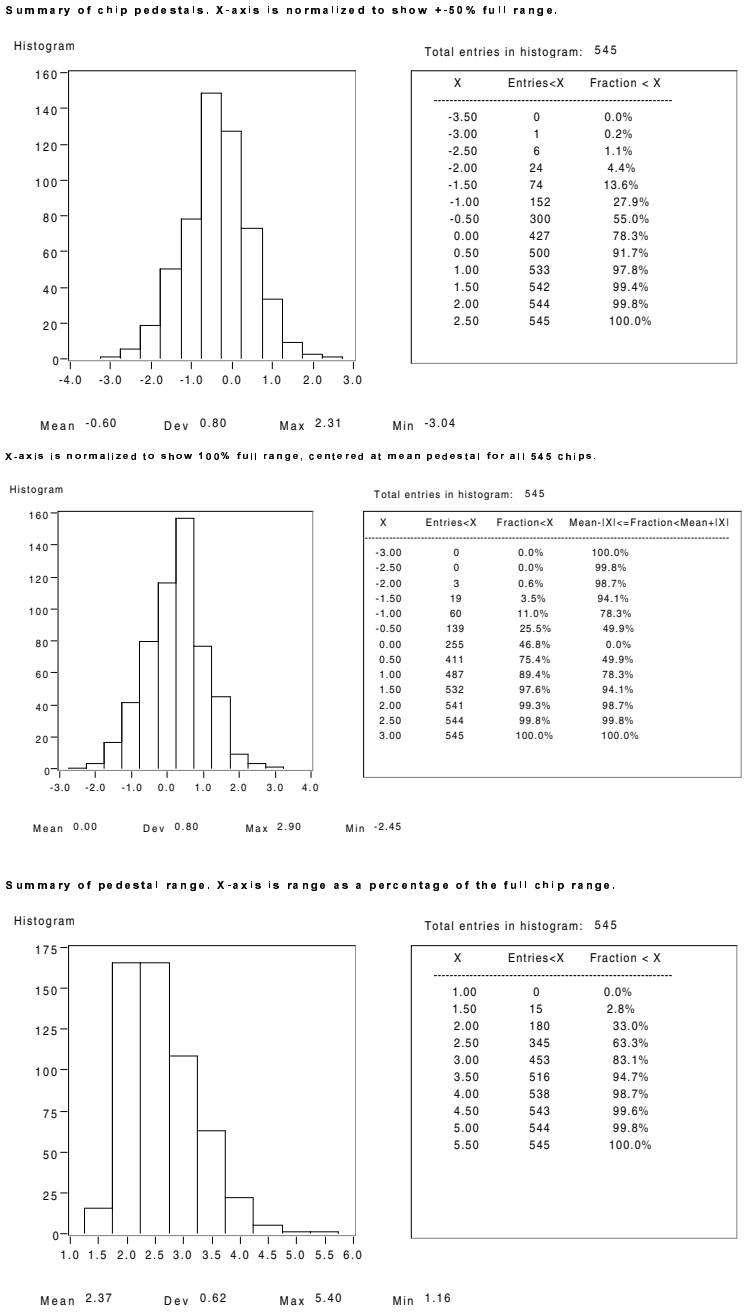


Figure 3.29: The plots show pedestal parameters normalized to a 100% range. The first plot is the average pedestal of a chip, the second is the same average pedestal but shifted so that the total average for all chips are at 0. The last plot shows the distribution of the pedestal range of the the chips.

errors, meaning the map shows a position and the board has the chip in the neighbouring position. The last kind of error is usually found in groups, several neighboring chips have

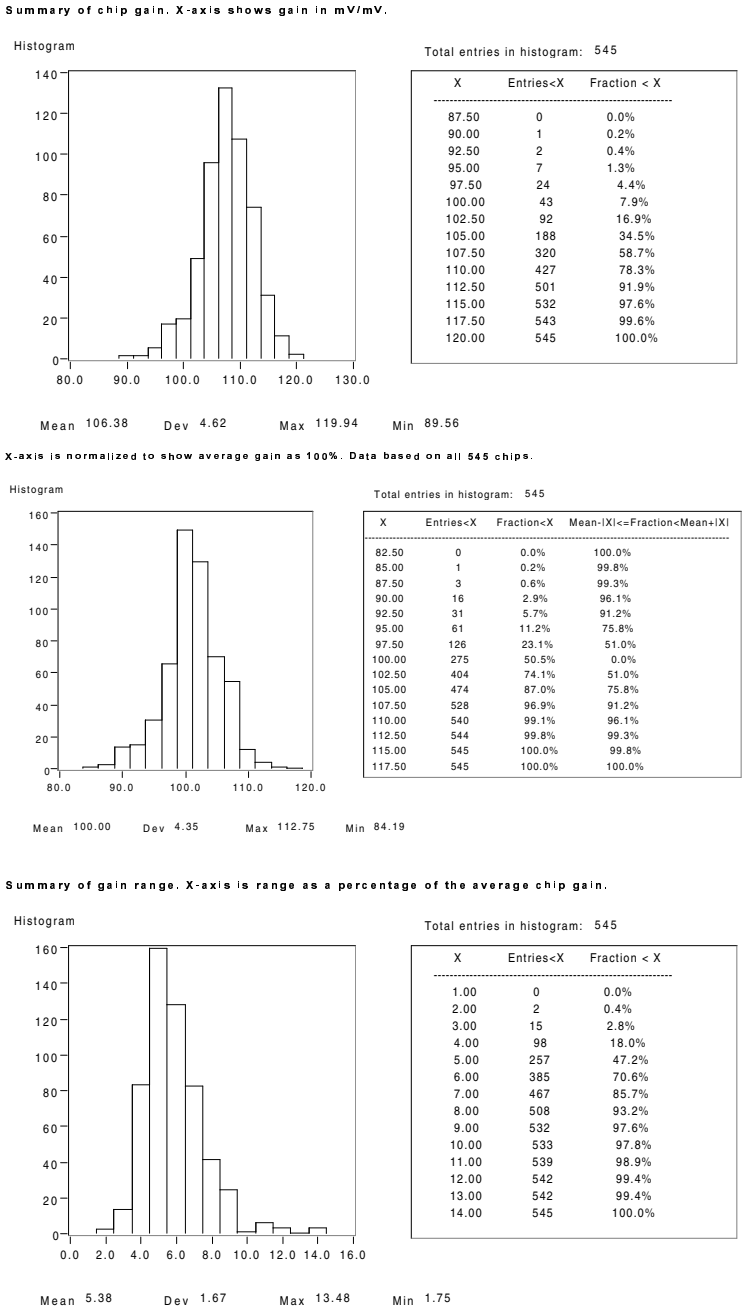


Figure 3.30: The plots show gain parameters. The first is the average chip gain in mV/mV, the second plot the same, but after normalizing to 100% as the average for all chips. The last plot shows the distribution of the range of the chips.

a real position one position offset from what is indicated in the map.

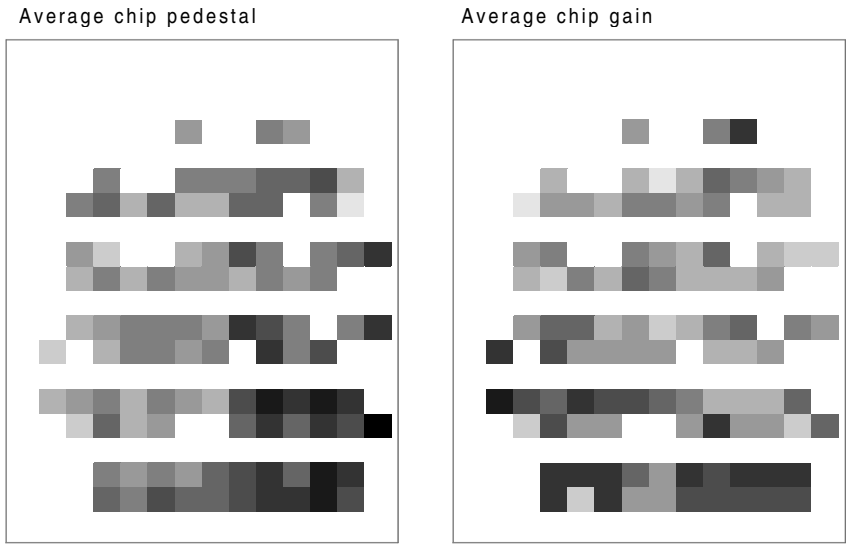


Figure 3.31: Spread in average gain and average pedestal throughout a wafer.

3.6 VA-RICH chip statistics

The VA-RICH boards were tested with a simple test system, based on a general DAQ-system and a special made interface card. The DAQ has a few number of digital output lines and 12 ADC's for sampling. The DAQ contains a Motorola 56001 DSP, which was programmed with a set of functions to be separately called by the PC. The interface card in the PC is an ISA bus card connected to the DAQ by a flat-cable. Even the supplies for the DAQ are taken from the ISA-bus of the PC.

Some problems were seen with this system. The current to voltage converter on the interface card was too noisy, which required a lot of averaging in the testing. This I-to-V converter does not have a very low input impedance resulting in voltage swings on the VA readout lines. Another problem is with the VA-RICH board itself. For the last board of a five chip readout chain, the VA-output lines are very close to the calibration input. This will give a positive feedback, which systematically increases the gain. The effect is clearest seen in the second chip, since the traces run alongside each other for a longer distance. This effect is an inductive effect between the current in the VA-output and the calibration line. There is also a capacitive coupling between the voltage swing of the VA output and the part of the calibration signal on the inside of the calibration capacitor. Based on the statistics from board types 1,2 and 3, which are consistent (same gain), it is possible to show a systematic increase in gain of about 2.5% on board type 4 and 9% in chip 0 on board 5 and 23% in chip 1 on board 5.

A total of 1008 boards are included in the statistics, giving a total of 2016 tested 64-channel VA-RICH chips. The chips were not wafer tested before assembly of the VA-RICH

board. This was due to a good wafer yield for VA-RICH chips, and the relative easiness of chip removal on a VA-RICH board. On the VA-RICH board each chip sits well apart from the other chip.

3.6.1 Conclusion of VA-RICH statistics

As in the case for Belle, the pedestal data is normalized to show a fraction of the output range. The average ibuf value used for all boards was 134 μA, corresponding to a total range of $\pm$2100 mV. The data sheet unfortunately logged only the average pedestal and pedestal range on a board basis, which is a 2 chip unit. The interesting parameters for each chip are the average pedestal and range and their standard deviation.

The distribution of the average pedestal is Gaussian, which means that one and two-chip units have the same average pedestal and the two-chip unit will have a standard deviation reduced by $\sqrt{2}$. An analysis using Belle wafer datasheets to build two-chip units gave the same average pedestal for one and two-chip units, which is logical because one can show the two summations to be identical. The factor $\sqrt{2}$ depends on the quality of the Gaussian distribution, and the simulated two-chip building using Belle data gave the proportionality of the standard deviations for one and two-chip units to be $\sqrt{2}$ to 99.5% accuracy. The analysis is more interesting for the chip range. Both the mean range and the standard deviation of the mean range are increased by a factor of $\sqrt{2}$, to within 2%, in building two-chip units, and the distributions have the same shape.

This result is used to scale the data, and is presented as 1-chip parameters in figure 3.32. The upper plot shows the pedestals moved to center the distribution around 0, and the second plot shows the range.

The gain statistics is based on the first chip on all boards of type 2, 3 and 4, on boards produced after mid of 1997 and with all 64 channels working. The number of chips are 527. The gain is measured as the current output (μA) divided by the input charge used, which is about 5.6 fC. Here it is assumed that the capacitor used to pulse each chip is 1.8 pF. Since the capacitors are not calibrated, the resulting spread found in the average gain involves the spread in the capacitors. The result is summarized in figure 3.33. The first plot shows the gain in μA/fC, the second shows the gain after it has been normalized to 100% for the average. The third plot shows the gain range in percent. A channel was defined as bad if the gain was outside $\pm$12.5% of the chip average gain, which means that these are not included in the statistics. The average gain is 8.3 μA/fC with a standard deviation of 6.5%. The average gain range is 10%.

To measure the noise characteristics of the VA-RICH boards 10 boards where tested with the VA-DAQ system. The average noise value for the 20 chips were 160 e^-, at vfp of $-$500 mV. In this calculation the three first channels of the second chip are not included in the noise measurements. The noise levels at the input of the ADC are in this case around 0.75 mV. The 14-bit VA-DAQ readout system has a noise roof given by the ADC quantization noise and the readout chain of about 0.18 mV. The resulting measured noise is the root mean square of these two, meaning that the real noise of the board is about 155e^- and the non-perfect readout system adding 5e^-. The data from these 20 chips also

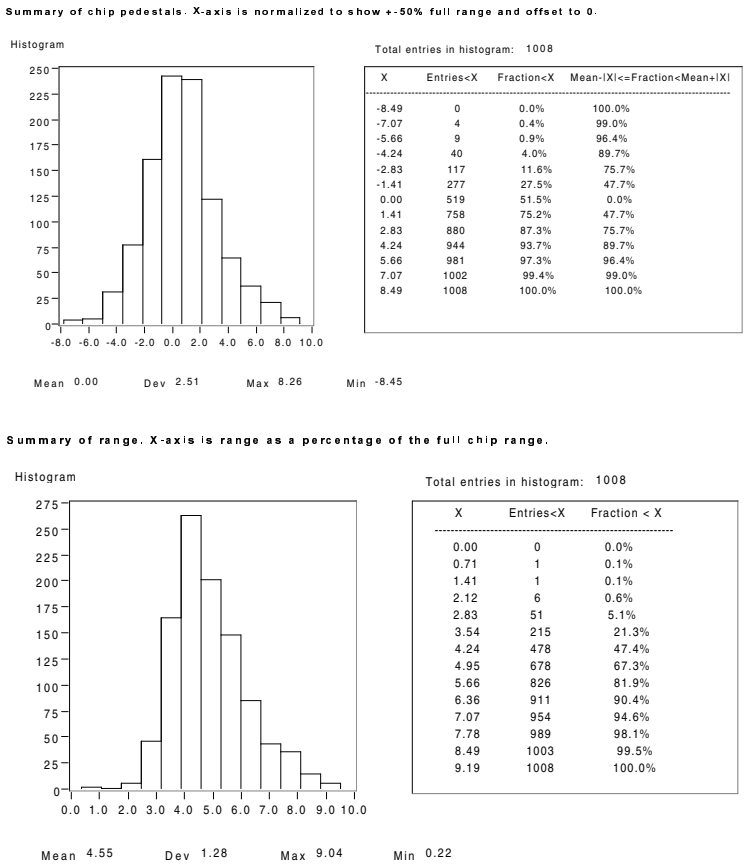


Figure 3.32: Calculated VA-RICH average chip pedestal distribution. Normalized to a percentage of the full range, and shifted so that mean is centered at 0. The lower plot shows the chip pedestal range. The values are based on x-axis rescaling of VA-RICH board data.

confirms the values found for pedestals and gains and their spread and range, by having all values within a $\pm 20\%$ range of the values found in the more comprehensive analysis above.

The noise profile for a chip clearly shows the effect of the different capacitive load due to different routing lengths from the chip to the connector. The plot show spikes for typically every other channel, reflecting that some channels need a longer route to reach the outer connector row, as seen in the upper plot of figure 3.10.

Figure 3.34 shows the similarity of noise profiles of two boards. Note that the second plot in this figure has two channels with a very low noise value, indicating a bad bonding of these two channels. The channels have therefore a very low capacitive load, and the noise is more or less the channel noise at zero capacitive load. This implies that bad channel bondings are located by setting a lower cut on the channel noise in an automatic test procedure. The advantage of this procedure is that bad channel bondings are located without the need of pulsing the detector inputs of the chip.

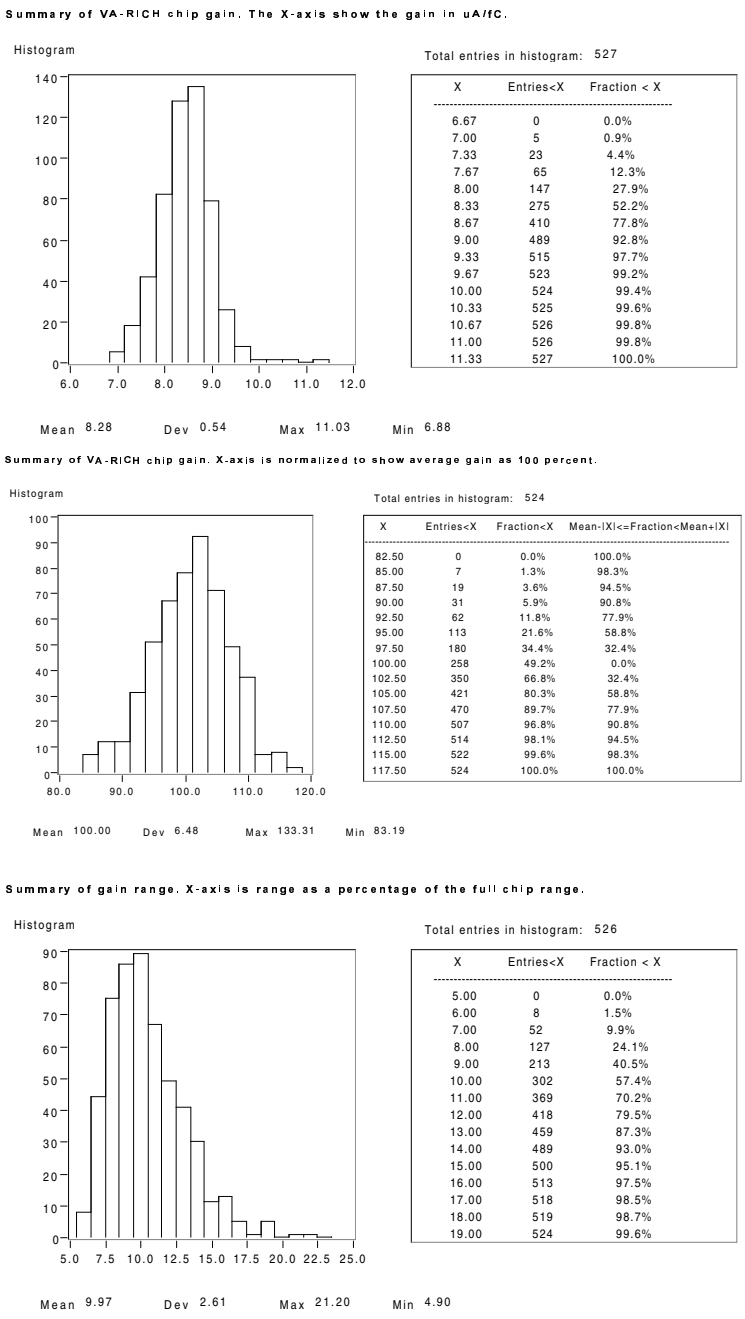


Figure 3.33: Average gain for 527 VA-RICH chips. The plots show the gain in μA/fC and in a 100% scale, and the lower plot the range in percent.

A lower envelope of the noise profile of the channels of a chip more or less contains all channels with the input track routing completely in the top layer and with no vias. The amplitude of this envelope is around $30e^-$, which must reflect the track length difference of these channels. A calculation based on a strip-line gives around 0.5 pF/cm for these

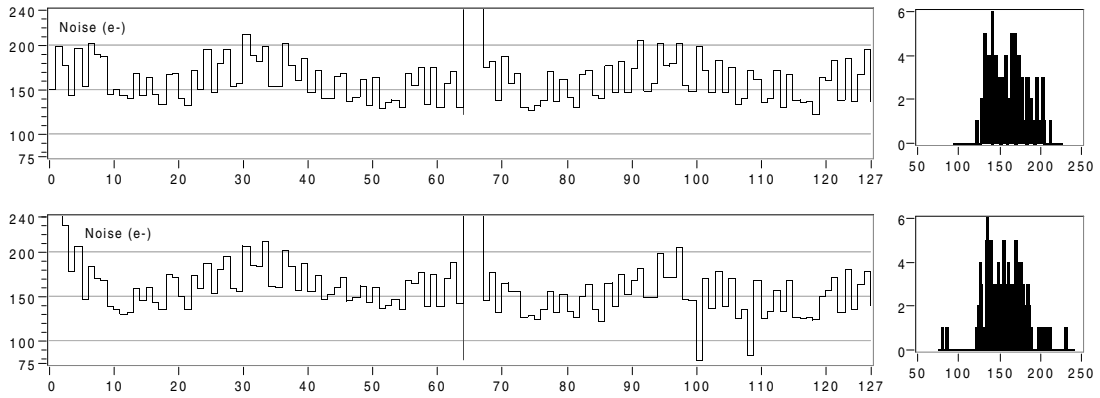


Figure 3.34: Noise profiles of two VA-RICH boards. A lower noise cut can be used to locate bad channel bonds.

tracks, indicating around 0.5 pF for the shorter input tracks and 1.5 pF for the longer, based on the measured track lengths. This seems to indicate a slope of $30e^-/pF$. The real capacitance must be higher due to coupling between neighbouring lines, and the actual slope should be below $30e^-/pF$. With the lower channels around $115e^-$ (after subtracting system noise) a first approximation is, ENC $= 100e^- + 30(e^-/pF) \cdot C_{in}$ for the chip. This is a crude approximation in the case the chip is bonded up to the VA-RICH board. It does not explain why the un-bonded channels seems to indicate a constant part of the ENC at $80e^-$.

3.7 Summary

Front-end readout boards have been produced and extensively tested for both Cleo-III RICH and for Belle SVD. The boards are implemented using very different technologies, motivated by the different needs of the two applications.

In the case of the RICH readout board the challenge is in the amount of routing needed on a small area, since all 128 channel inputs must be routed from the connectors to the chip. This facilitates the need for a 4-layer board, and great care needs to be taken to shield the inputs from the digital activity and to ensure a low stray capacitance, both vital in reducing the noise. The readout board will not have any function in the mechanical support. Cooling in addition to the radiation and convection to the surrounding gas is not necessary since only around 150 mW is dissipated in a rather large area. The solution is therefore to use a standard cheap FR4 PCB material, which is a material with rather poor mechanical and thermal properties.

For the SVD readout boards other factors are important. The boards will have to provide the mechanical support of the DSSDs of the ladders, which need to be aligned to a high precision. In addition is removal of the heat of the front-end necessary since 1.5 W is dissipated in a small area. The described prototype design use a ceramic substrate

of aluminum-nitride (AlN), with good mechanical and thermal properties. Only a single electrical layer in gold (Au) is printed on this substrate, not requiring any fine pitch lines. Laminated on top of the AlN-Au is a thin polyimide film, possible due to the thin film process. The PCB and the AlN-Au are glued together with a film adhesive stenciled to the correct shape. This ensures a thin glue layer. The film has good thermal properties and is suitable for joining materials of different thermal expansion. The total hybrid fulfills all requirements; good thermal and mechanical properties, a short production time of a few weeks, and low cost. This makes this innovative buildup a very good choice for fast prototyping in small series. The Kyocera version of the board used in the detector has a cost and a turnaround time at least a factor of five higher.

Measurements on large samples have been used to get good statistics on VA1 and VA-RICH chip parameters. These measurements have shown that the chip to chip spread of channel parameters are typically in the range one to two times the internal chip spread. This suggests binning of chips if tight limits are imposed on multi-chip boards.

The statistics has also verified the use of the VA-DAQ readout system. All parameters can be measured to a high precision, and especially the noise can be measured down to what is expected for the chips from theoretical calculations. The latter point is very important, it shows that the VA-DAQ is well engineered so that no noise is induced by the readout system. The noise is at the theoretically possible minimum, given by the parameters of the sensor (capacitive load) and the front-end chip (its input transistor).

Probe testing of chips on wafers shows that all parameters can be measured to a high precision, and that the same chip parameters are re-measured at the finished boards. The noise measured by probe-needle cards with a probe-station shielded by an aluminum cage is similar to the measurements on the finished boards. This proves that a good test environment for wafer testing of chips has been designed. Wafer measurements also suggest, as expected, that neighbouring chips on the wafer have similar overall parameters. In an application where it is not found worthwhile to bin chips after average parameters, it will help on the total spread to use chips close to each other on the same wafer.

The interesting use of the pedestal pattern as a fingerprint for chips can be used to check the logistics in the mounting process. In an application where the boards can be equipped by any chip that passed the wafer test, no logistic is needed. All chips marked as good can be used. An automatic program can be used to locate which wafer and the position on the wafer that a specific chip, on a board under test, originates. This saves a lot of time on logistics in a manual mounting process.

Of course the final test of the success of the readout boards must come from the results obtained with the full detectors:

For Cleo-III RICH results have been presented at three major HEP conferences; the 29th International Conference on HEP [31] in 1998 in Vancouver, Canada, the IEEE Nuclear Science Symposium [35] in 1997 in Albuquerque, US, and the 7th Pisa meeting on Advanced Detectors [36] in 1997 in Elba, Italy. The 1998 paper concludes that excellent results have been achieved with full RICH chambers, even under not optimal test beam conditions at Fermilab. The necessary π-K separation needed to get three sigma confidence is 12.8 mrad, and the paper quotes 13.5 mrad and 11.8 mrad for planar and sawtooth LiF radiators,

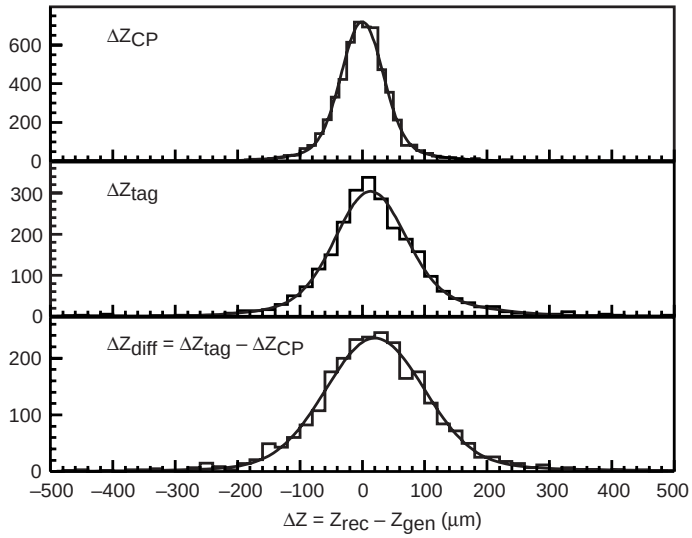


Figure 3.35: Showing the vertex resolution (distance between Monte-Carlo generated position and the reconstructed position), ΔZ, in the lowest plot. ΔZ has a mean of $24\,\mu$m and a width of $\sigma = 105\,\mu$m.

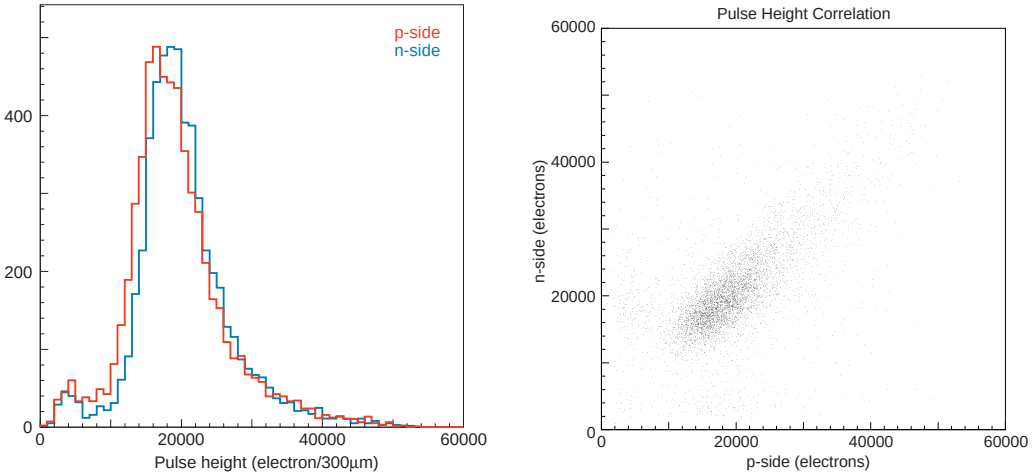


Figure 3.36: Pulse height distribution and pulse height correlation for p and n sides of the Belle SVD by cosmic rays.

respectively. The noise in the readout boards (including the Belle test readout system) have been measured to be ENC = $130e^- + (9e^-/\text{pF}) \cdot C_{in}$. The constant part is slightly above theory and the values by VA-DAQ, while the slope is lower. The actual values achieved are around $200e^-$, indicating around 8 pF of total load. The Cleo-III will start data taking around end of 1999.

The Belle SVD has been fully assembled, using the hybrids based on the Kyocera pro-

cess. The operational SVD has already taken data based on cosmic particles. Preliminary results were reported at the LCPAC99 [37] at KEK, Japan, in February 1999. It concludes that the estimated vertex resolution meets the design goal of $95 - 100\,\mu$m, as shown in figure 3.35, where the lowest plot for ΔZ has a width of $\sigma = 105\,\mu$m before much optimization has been done. Analysis of cosmic data is in progress, showing preliminary SVD hit efficiencies above 94% using a CDC as a reference. Figure 3.36 shows pulse-height distribution of cosmic hits on p and n sides and associated correlation plots. The pulse height distributions indicate equal and close to full charge collection for both p- and n-sides.

The use of VA electronics for these experiments have demonstarted the maturity of this technology. The chips are produced at high yield and with noise characteristic limted by noise theory of the sensor/front-end physics and not the design. The chips are however constrained by dead time and data collection speed, and read-out must be interleaved. In addition are they in the radiation weak AMS process. This is acceptable for relative low rate and low radiation experiments like the B-physics experiments. The next chapter concerns the ATLAS detector, which requires new chips due to the extreme rate and radiation level. Here a lot of problems must be solved, concerning pipelining and continuos readout during data taking, and understanding of new radiation hard ASIC processes. Many child diseases such as front-end instability and low wafer yield have been seen. The requirements for thermal and mechanical stability are even more difficult than for Belle, with a silicon strip area of close to 50 square meters compared to less than 0.2 square meters.

Chapter 4

Silicon detector-systems for the ATLAS SCT

My main contribution to the ATLAS Semi-Conductor-Tracker (SCT) has been in the design and production of hybrids for the barrel modules. This activity has been pursued by the author with the great help of O. Dorholt as the expert on the CAD layout tool. The results in this chapter reflects the status of the project roughly at the beginning of 1999.

The most important function of the hybrid is to provide the electrical means of reading out the front end chips. The hybrid is an integrated part of the module, however, and its mechanical, thermal and radiation length properties are very important in achieving a satisfactory working module. This is very critical in a detector such as ATLAS where the read-out hybrids sit within the active detector volume.

Several hybrids have been designed and produced, based on different technologies, and they are being summarized in table 4.1. All have been produced at Gandis Workshop at CERN, except for the FElix32 design [7] that was produced at AME in Horten, Nor-

Chip	**Process**	**Designed**	**Comment**
FElix32+Mux	AgPd/oxide/alumina	2/95	Analogue.
FElix128+Mux	Au/oxide/alumina	7/95	Analogue.
FElix128	Au/oxide/alumina	5/96	Analogue. Not produced.
SCT128A	Au/oxide/alumina	10/96	Analogue. Electrical testing.
SCTA128HC	Au/oxide/alumina	6/98	Realistic module.
SCTA128HC	Au/oxide/alumina	3/99	In production.
SCT128B	Au/oxide/alumina	3/97	For realistic module.
SCT128B	Au/oxide/beryllia	3/97	Single sided module built.
ABCD	Au/oxide/beryllia	12/97	Single sided module built.
ABCD	Al/poly/PG	12/97	Full module built.
ABCD3	Al/poly/TPG	10/98	Module being built.
ABCD3	Au/oxide/alumina	12/98	Hybrid with chips tested.
ABC+CAFE	Al/poly/TPG	progress	Awaiting chip completion.

Table 4.1: Hybrids designed by the Oslo group for ATLAS SCT barrel module development.

way. The AME design was a thick film process based on AgPd conductors on an alumina substrate. All thick film hybrids produced at CERN have been based on Au conductors on either alumina or beryllia substrates. The thin film hybrids have been produced in cooperation between Gandis Workshop and a French company and is based on Al as conductors and polyimide as insulators. These are mounted either on a PG substrate, or for the remaining hybrids on a TPG substrate.

The earlier designs were aimed at an analogue readout scheme, the two first ones for the chips FElix32+Mux32 and FElix128+Mux128 [7]. A third design based on the full FElix128 (integrated output multiplexer) was never produced due to the non-working readout part of this version of the FElix128 chip. Later analogue designs were based on DMILL analogue chips being developed in parallel with the binary DMILL readout chips SCT128B and ABCD. Two hybrids were produced based on the SCT128A and on the later revision SCTA128HC. Only the SCTA128HC is a realistic design for building a real analogue module, similar to the binary modules presented in this chapter.

The binary front-end is the baseline in the ATLAS SCT, and the rest of the described hybrids are made for binary front-end chips. The SCT128B and ABCD designs on BeO have both been used in making working single sided modules, with results being presented in [38] and [39].

The ABCD design was modified for the Al/polyimide process to make the first Al/polyimide on PG hybrid. This design has been assembled into a working double sided hybrid, in which results are to be published at a later stage.

The ABCD chip has been revised, the newest version being called ABCD3. An improved polyimide hybrid has been designed and produced for being placed on a TPG substrate. Here the technology is based on confining the TPG in an epoxy frame and the hybrid being inserted in one big kapton piece constituting the cabling in between. Connections between the kapton cable and the hybrid are by bonding, but the solder footprint for the old cables have been kept on the hybrid allowing the TPG hybrids to be used in other module designs.

Two new designs are being made. The first is a BeO design for the new ABCD3 chip, to have a SCT baseline design based on the ABCD3 in addition to the ABC+CAFE design by other ATLAS groups. In this way baseline BeO designs exist for both competing chip solutions; integrated and separated front-end and pipeline chips. The second design is a TPG hybrid for the ABC+CAFE, such that a TPG/Al/polyimide design exists for both competing chip sets. In this design, as opposed to the TPG/Al/polyimide for the ABCD3, the solder connector option is removed and only the bond pads are left, which allows the hybrid to shrink to a width of 22.55 mm. The old size of 28 mm was limited by the connector footprint decribed in the Inner Detector TDR.

Before describing the details of the SCT barrel module involvement an overview of the LHC and the ATLAS experiment is given in the following sections.

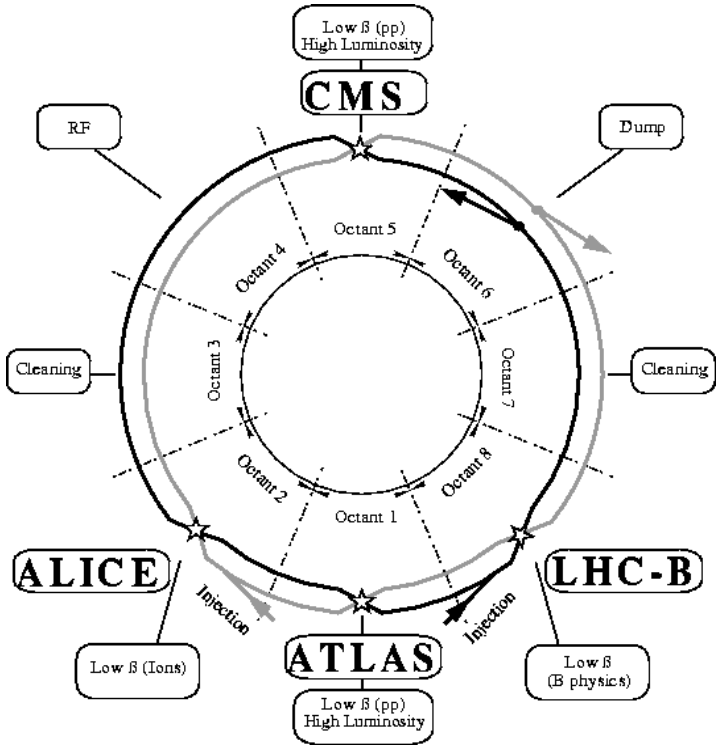


Figure 4.1: Interaction points at the Large Hadron Collider.

4.1 The Large Hadron Collider

At CERN, the next big leap in the energy frontier of particle physics will be taken by the Large Hadron Collider, LHC. Designed to collide protons at a center of mass energy of 14 TeV, it will be the tool to search for the origin of the spontaneous symmetry-breaking mechanism in the electro-weak sector of the Standard Model (SM), responsible for the masses of particles in the SM. The design goal of the collider is to provide a luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, necessary since the interesting processes to study in the SM and in the Minimal Super-symmetric extension to the SM (MSSM), have very low cross-sections. This is achieved by having the 7 TeV bunches separated by 25 ns, giving a collision frequency of 40 MHz.

The Collider will be installed in the old LEP-tunnel, with an approximate circumference of 27 km, shown in figure 4.1. The two high luminosity general purpose pp-experiments ATLAS and CMS will be located in the points 1 and 5, respectively. Two more experiments are planned, ALICE, a heavy ion (Pb-Pb) experiment with a center of mass energy of 1150 TeV for the investigation of quark-gluon plasma, and LHC-B for B-physics studies. To further reuse existing facilities, the Linac, Booster, PS and SPS will be used for particle injection to the LHC [41].

4.2 Physics for the LHC

The designs of the general purpose detectors ATLAS and CMS are guided by three major physics questions [42]:

- What is the source and mechanism of electro-weak symmetry breaking in the Standard Model? This leads to the requirement of being sensitive to the full mass range of the Higgs boson, which should have a mass in the range $80 - 1000\,\mathrm{GeV}$. In the minimal version of the SM only one Higgs particle will exist, and the sensitivity is required to study the decay of a Higgs particle to $\mathrm{b\overline{b}}$ using b-tagging, to two gammas, and to four charged leptons via ZZ, just to mention a few. In the case of MSSM, the Higgs sector will contain 5 particles, requiring sensitivity to a range of other processes as well.

- Can we unify all forces and find a consistent theory of matter all the way to the Planck scale? This is achieved by super-symmetric theories since they stabilize gauge couplings. Locally super-symmetric theories include gravity, and super-symmetry appears natural in String Theories.

- Is it possible to explain the masses, couplings, mixing angles and CP-violations in the SM? These questions are tested experimentally by very detailed measurements of the SM, searches for extension of the SM, searches for compositeness and detailed studies of b-quark systems. The B-physics is for instance strongly affecting the inner detector design by requiring precise determinations of primary and secondary vertexes.

The most interesting processes to study in order to answer these questions are addressed in the following sub-sections. In addition is it interesting to note that the sets of processes for which sensitivity is required, can be given as a list of design considerations, or equally well as a list of sub-detectors from outermost radius and in [43, chapter 1]:

- Stand-alone muon momentum measurements.

- Hermetic jet and missing $\mathrm{E_t}$ calorimetry.

- Electro-magnetic calorimetry with photon/electron identification.

- Tracking for lepton momentum and for b-quark tagging at high luminosities. In addition τ and heavy-quark vertexing and reconstruction of selected B-decay states, at lower luminosities.

4.2.1 Electro-weak symmetry breaking

Today the theoretical knowledge leaves the electro-weak sector largely unconstrained, which allows two classes of theories; weak or strong coupling of the sector. If the sector is weakly coupled one or more Higgs bosons will exist below one TeV, in the other case much more complex behavior is expected.

The search for the Standard Model Higgs relies on its decay $ZZ^* \rightarrow 4\ell$, over a mass range of 130 to 800 GeV. Below 130 GeV the Higgs decays dominantly to $b\overline{b}$, problematic to find due to massive $b\overline{b}$ background. Instead the most promising channel in this energy region is $H \rightarrow 2\gamma$.

If the sector is more strongly interacting and the Higgs-mass around one TeV, the mass spectrum is very broad. It leads to strong scattering of gauge boson pairs, eventually violating unitarity for the s-wave scattering amplitude, which can can be manifested in final stage gauge boson pair channels such as:

- Modifications of longitudinal components of the SM scattering amplitudes of the $W^{\pm}$ and Z bosons at several TeV. Here a characteristic signature is production of W^+W^+ and W^-W^- pairs, and the best process is $pp \rightarrow W_L^+W_L^+$, which is not suffering from gg or $q\overline{q}$ background.

- The Higgs is replaced by technicolor models with $W^{\pm}Z$ or $Z\gamma$ resonances at a few TeV.

4.2.2 Beyond the Standard Model

So far the SM is very succesful in explaining interactions up to the highest achievable energies of today. LHC will however provide precision measurements on the SM and its extensions:

- Precision measurements on the W and t masses that can constrain new physics and the consistency of the SM.

- Even at low luminosities will 50000 $t\overline{t}$ pairs be produced per day, which also allows studies of rare top-decays, another window to new physics.

- Production of gauge-boson pairs as a test of three-vector boson couplings. This coupling is a part of the SU(2) symmetry of the SM. It can however contain underlying non-standard physics for WWZ- and WWγ-vertices in the SM Lagrangian. At LHC these vertices contribute to gauge-boson pair production, Wγ, WZ and W^+W^-. For example the Wγ production provides a signal in the detector of a high p_T lepton (that triggers the experiment) and a high p_T electro-magnetic cluster, identified as a photon. The irreducible background is from events containing a real lepton and γ, such as $pp \rightarrow \gamma Z \rightarrow \gamma\ell\ell$. Using the distribution of the transverse photon momentum it is possible to study an anomalous vertex coupling if it is there.

- Search for new gauge-bosons. The detectors are capable of identifying new gauge-bosons, W' and Z', decaying leptonically, up to a gauge-boson mass of about 6 TeV, provided that the cross-sections and branching ratios are not too small.

- Search for compositeness. Deviations from the SM are expected if the quarks or leptons contain more fundamental constituents. For quarks this would be seen as

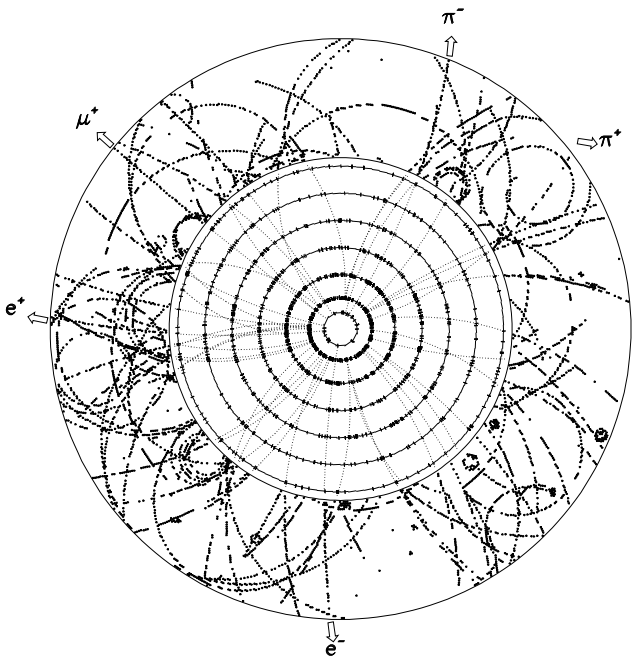


Figure 4.2: Projection of B-event in the barrel sector of the Inner Detector.

deviations from the QCD expectations for jet production at high transverse momenta, where the valence quark scattering dominates. It can be shown that the quality of a compositeness measurement strongly depends on the calorimeter energy linearity and its extrapolation to higher transverse momenta.

4.2.3 B-physics

The LHC is also a B-factory, producing $5 \cdot 10^{12}$ $b\overline{b}$-pairs yearly. This allows precision measurements, especially in the search for CP-violation in B-decays, which was also described in chapter 3. In addition is the investigation of B_s^0-mixing, the search for rare B-decays and B-hadron spectroscopy of special interest. Figure 4.2 shows a B-event in the barrel sector, decaying to leptons and pions.

4.2.4 Super-symmetry

The MSSM includes the SM and adds super-symmetric partners to all particles. The MSSM also contains two Higgs doublets. The experimental search for super-symmetry follows two paths; the search for Higgs particles in the MSSM and the direct search of supersymmetric partners of the quarks, leptons and bosons (squarks, sleptons, charginos and neutralinos).

The MSSM needs two Higgs doublets to generate mass for the up and down type of quarks. This will give five physical states, or 5 Higgs particles, called H^+, H^-, h, H and A. These are pursued experimentally through the channels:

- $A, H \rightarrow \tau\tau$,

- $h, H \to \gamma\gamma$,
- $H \to ZZ \to 4\ell$ and
- $t \to bH^+$.

The production and decay of sparticles will result in various signals, a few are:

- The lightest super-symmetric particle (LSP), which is almost always neutral and a good cold dark matter candidate, will leave the detector and give a missing transverse momentum.
- Several large p_T-jets from cascade decays.
- Several leptons from decays of charginos and neutralinos.

4.3 The ATLAS Detector

One of the large detectors to be built for LHC is A Toroidal LHC ApparatuS, or ATLAS, shown in figure 4.3. This multi-purpose pp-detector lends its name to the fact that the outer magnet system of ATLAS consists of air-core toroids, to minimize multiple scattering.

The outermost sub-detector, the muon spectrometer, defines the outer dimension of the ATLAS detector. The radius being about 11 m and a length of about 26 m, in addition is the third layer of the forward muon chambers fixed to the cavern walls approximately 42 m apart. Not only are the dimensions enormous, so also the total weight of about 7000 tons.

The calorimetry is Liquid Argon (LAr) based for the electro-magnetic calorimeter and also for the hadronic calorimeter out to a radius of 2.2 m. At larger radii is the hadronic calorimeter based on a much cheaper iron-scintillator design, called the Tile calorimeter.

The inner detector is confined within a radius of 1.15 m and with a length of 6.8 m, in a 2 T field set up by the solenoid inner magnet system. The Inner Detector is responsible for vertexing, tracking, momentum measurement and enhanced electron identification, and will be described in more detail in the next section.

4.4 The ATLAS Inner detector

The main objective of the inner detector is to track charged particles from the beam pipe and out to the electro-magnetic calorimeter. A cross section of one half of the inner detector is given in figure 4.4. It shows the three important subsystems of the Inner Detector [44]:

- The Pixel detector. The detector is based on high-granularity silicon pixel detectors to provide precision position measurements as close to the interaction point as possible. The detector covers the full acceptance and with three points per particle determines the impact parameter and vertexing of short lived particles like b-quarks and taus. The number of electronic channels are about 140 millions.

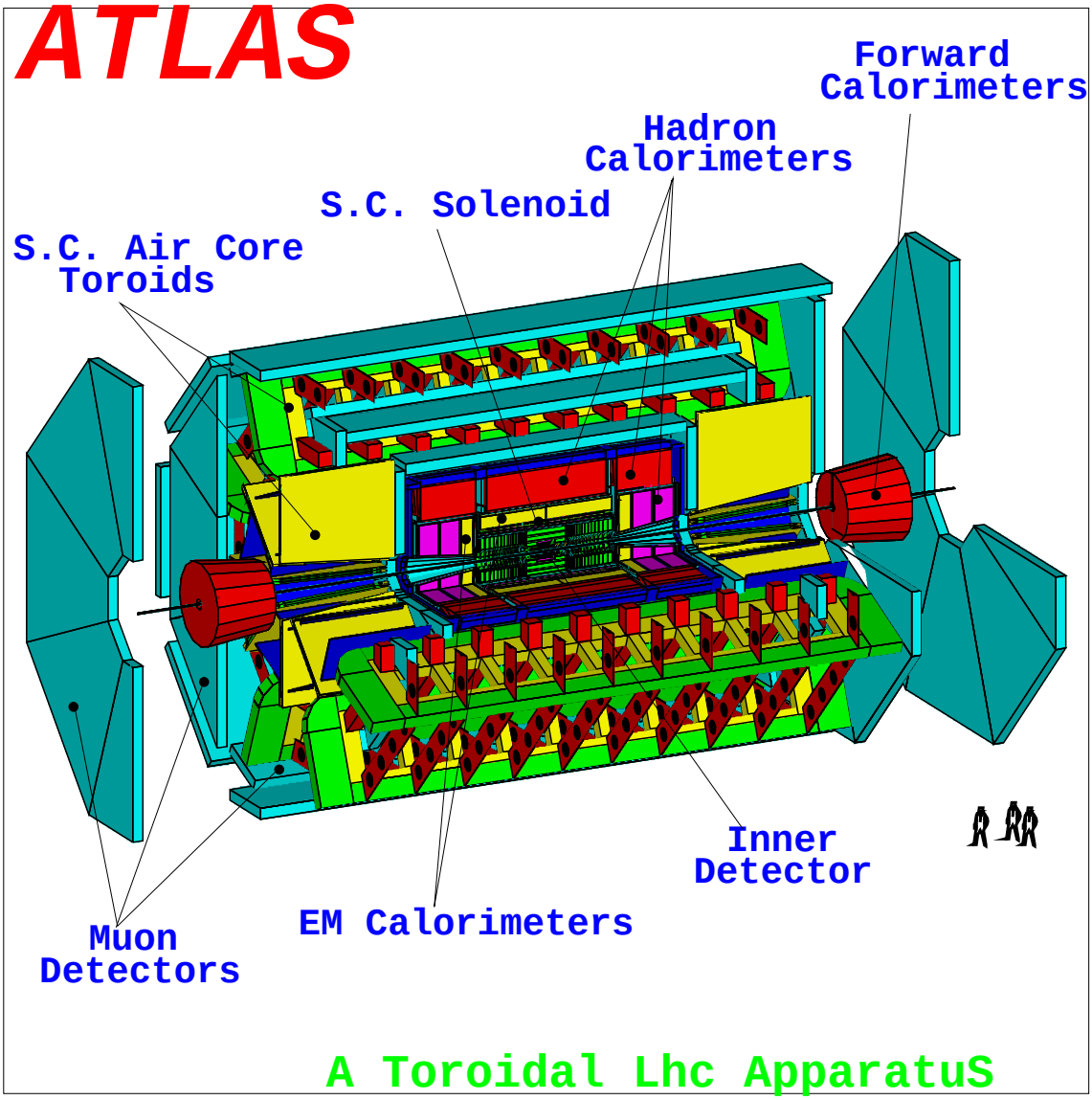


Figure 4.3: 3D layout of the ATLAS detector.

- The Semiconductor Tracker, SCT. The detector will give four precision measurements per track in the intermediate radius range, necessary in the momentum and impact parameter measurements. The granularity is high enough to ensure good pattern recognition. The selected detectors are silicon strip sensors, with active strip lengths of 12.8 cm and a pitch of 80 μm. This is the sub-detector considered in this thesis and will be further described in the next sections.

- The Transition Radiation tracker is based on straw tubes, 4 mm in diameter. The straw gas is Xenon, which facilitates electron identification by using double threshold readouts. The transition radiation photons created by the electrons are caused by a

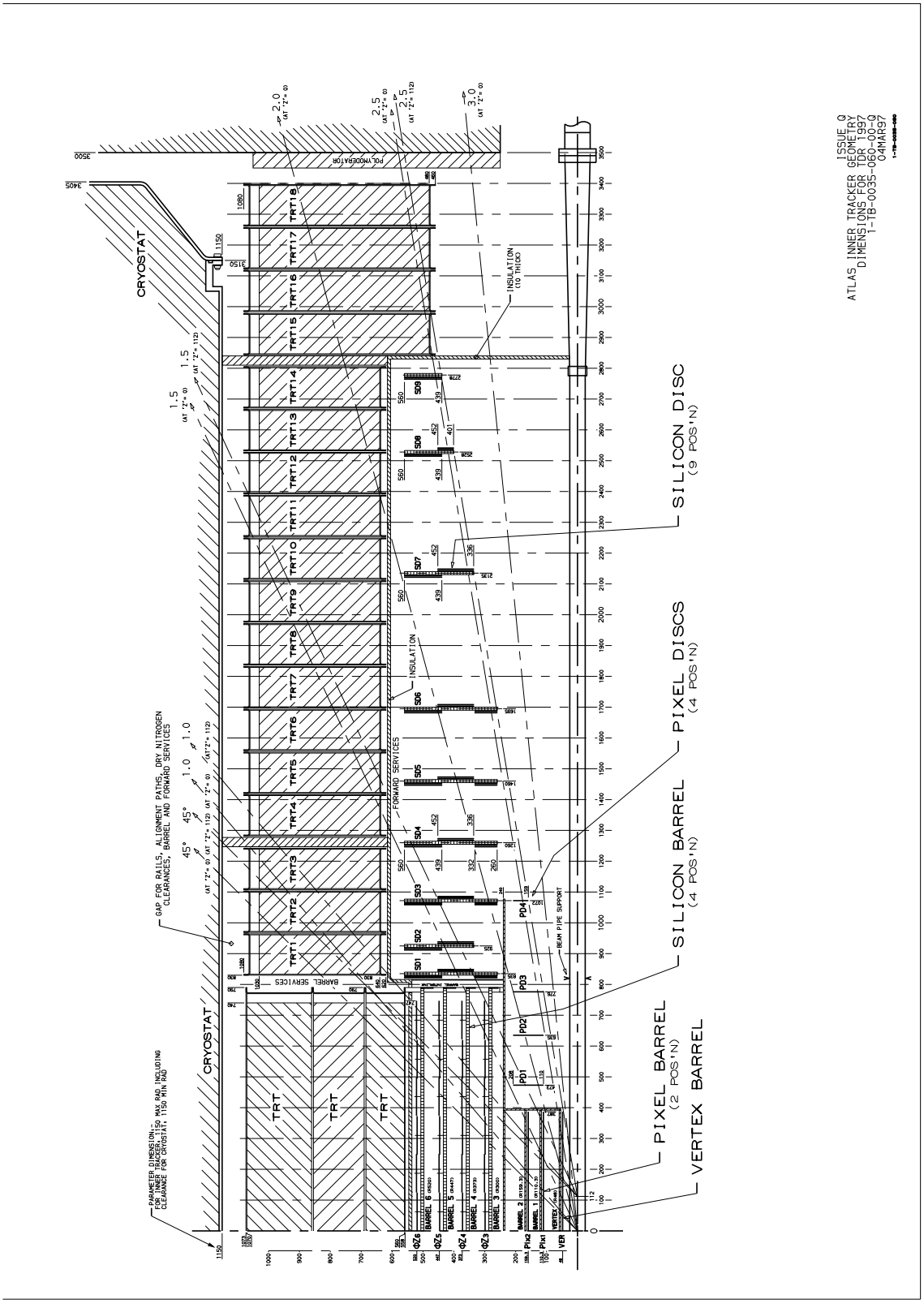


Figure 4.4: One half of the Inner Detector.

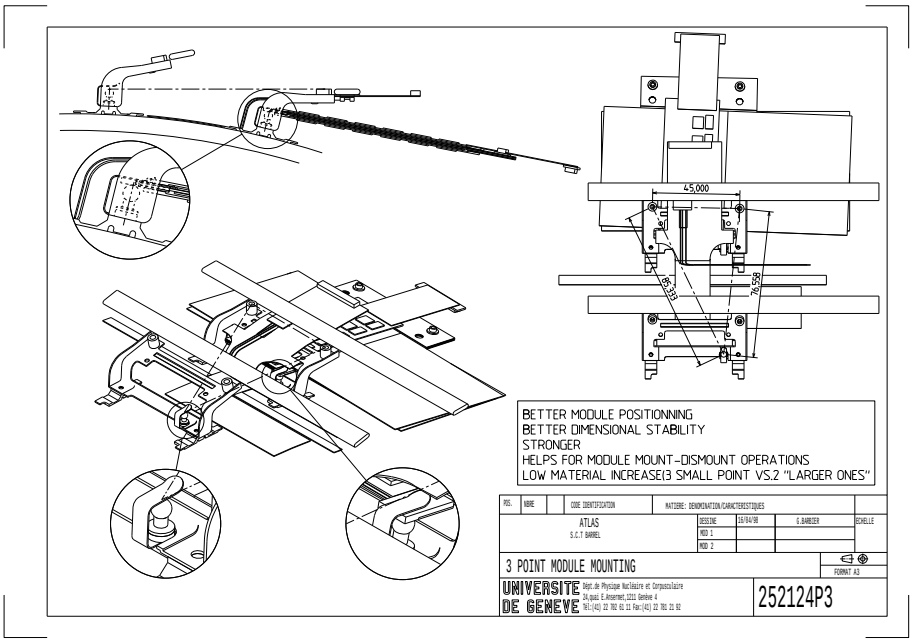


Figure 4.5: One mounting option for modules onto the carbon-fiber cylinder.

radiator in between the straws. The barrel section contains 50000 straws, divided in two and read out at the ends. The end-caps contains 320000 radially oriented straws. The total number of points per particle is on the average 36.

4.5 The Semiconductor Tracker

The Semiconductor Tracker, SCT, is organized as 4 concentric cylinders in the barrel region of about 30.0, 37.3, 44.7 and 52.0 cm radius. The detector modules, approximately 6 cm width by 12 cm length, are mounted onto carbon-fibre cylinders. In each forward direction the modules are mounted onto 9 wheels, each wheel having up to three rings of detector modules. The wheels are interconnected by a space frame. The cooling system of the SCT is based on evaporative cooling by fluor-carbons (C_4F_{10}, C_3F_8 or CF_3I) at a temperature of about -15^oC. Figure 4.5 shows one alternative of attaching modules onto the carbon fiber cylinder.

The basic building block is as mentioned before the module. In the barrel section it consists of four single sided silicon micro-strip detectors. Each detector has a size of 6.36 cm by 6.4 cm with 768 readout strips with 80 μm pitch. Each side of the module consists of two detectors glued and wire bonded edge-to-edge to form an unit with 12.8 cm long strips. Two such units are glued back to back with a baseboard for heat transport in between, with the strips at a 40 mrad angle, which is enough to ensure the desired z-resolution (along beam axis). The readout chips are mounted on a hybrid sitting as a bridge above the sensors, and bonded to the strips at the midpoint of the 12.8 cm long strips. A drawing of

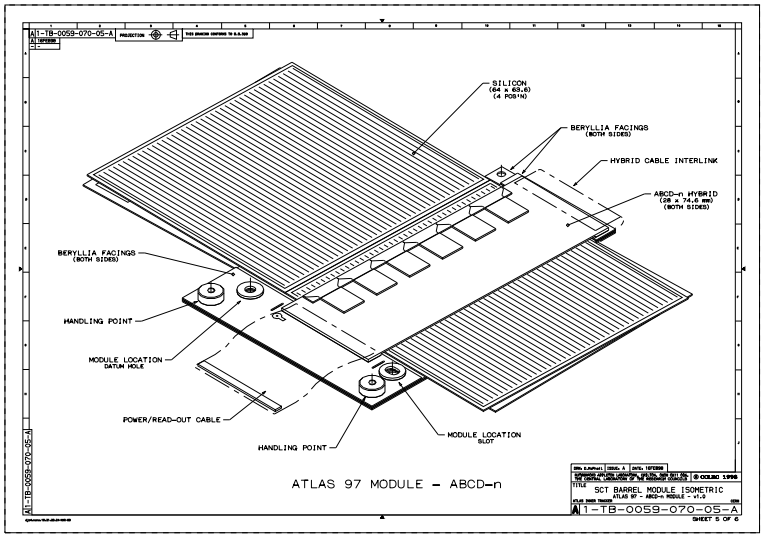


Figure 4.6: An ATLAS SCT silicon strip module for the barrel part.

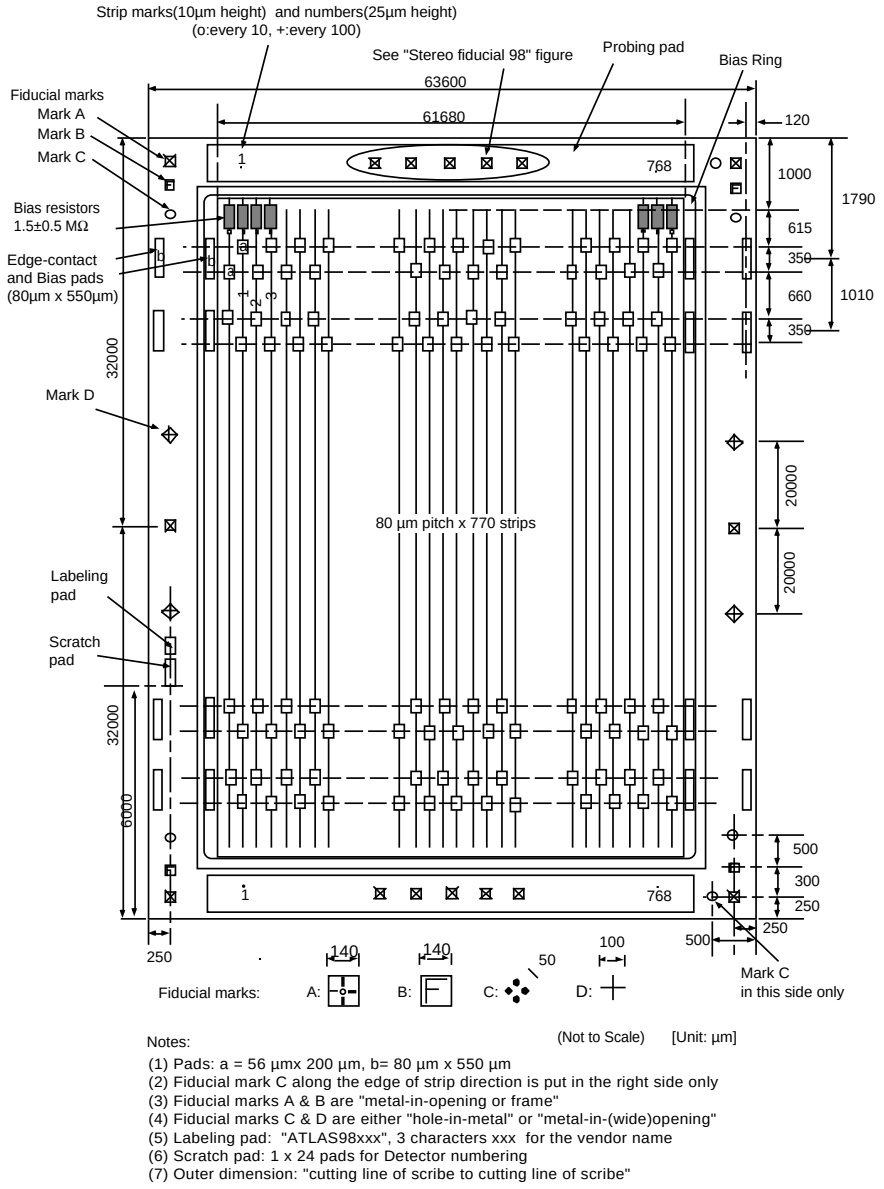
Item	Value	Description
Size	63.6 x 64.0 mm^2	At cutting scribe line.
Thickness	$285 \pm 15\,\mu$m	Uniformity required to be $\pm 10\,\mu$m.
Implant strips	768 readout + 2	$18\,\mu$m wide and 62 mm long.
Implant type	p-type $> 10^{14}/cm^2$	Implant depth $1 - 1.5\,\mu$m
Substrate type	n/type $2 - 8\,k\Omega/\Box$	Upper limits on C and O concentrations.
Readout strips	$1\,\mu$m within implant	Aluminum - AC coupled to implant.
Readout resistance	$< 20\,\Omega$/cm	Low strip resistance (series noise).
Total cap load	< 1.2 pF/cm	Measured at depletion and at 1 MHz.
Readout capacitance	> 10 pF/cm	Dominate inter-strip capacitance.
Strip capacitor dielectric	si oxide + si nitride	Reduces pinholes.
Biasing	$1.5 \pm 0.5\,M\Omega$	Poly-silicon resistors.
Leakage	$< 2\,\mu$A/strip	After irradiation (shot noise).
Maximum voltage	350 V	After irradiation.
Bond pads	200 x $56\,\mu$m	These are ordered in two rows.
Bad strips	max. 1% on average	No device with more than 2% bad strips.

Table 4.2: Specifications of the ATLAS SCT barrel p-in-n detector [45].

a module is shown in figure 4.6 [44].

The main design consideration for the ATLAS SCT silicon strip sensor is the radiation tolerance. Intensive studies have shown that p-in-n detectors can survive 10 years of operation without violating the maximum safe operating voltage of about 350 V. The main specifications for the silicon strip detectors are summarized in table 4.2, and a layout description shown in figure 4.7. Figure 4.8 shows the layout of one corner of a detector.

Silicon micro-strip detectors have been used for several years in many particle physics experiments, the challenge in the ATLAS SCT project lies in the difficulties introduced by scaling this an order of magnitude in size, speed and radiation levels. The size increase



Notes:
(1) Pads: a = 56 µmx 200 µm, b= 80 µm x 550 µm
(2) Fiducial mark C along the edge of strip direction is put in the right side only
(3) Fiducial marks A & B are "metal-in-opening or frame"
(4) Fiducial marks C & D are either "hole-in-metal" or "metal-in-(wide)opening"
(5) Labeling pad: "ATLAS98xxx", 3 characters xxx for the vendor name
(6) Scratch pad: 1 x 24 pads for Detector numbering
(7) Outer dimension: "cutting line of scribe to cutting line of scribe"

Figure 4.7: Layout description of the ATLAS SCT barrel p-in-n strip sensors.

coupled with the position resolution puts very strong demands on the rigidity of the support. Furthermore, the size requires one to put the electronics within the active detector volume, with the implication this has on the radiation tolerance of the read-out chips. The quality of the tracking is limited by the amount of material within the active volume, and this material must be minimized.

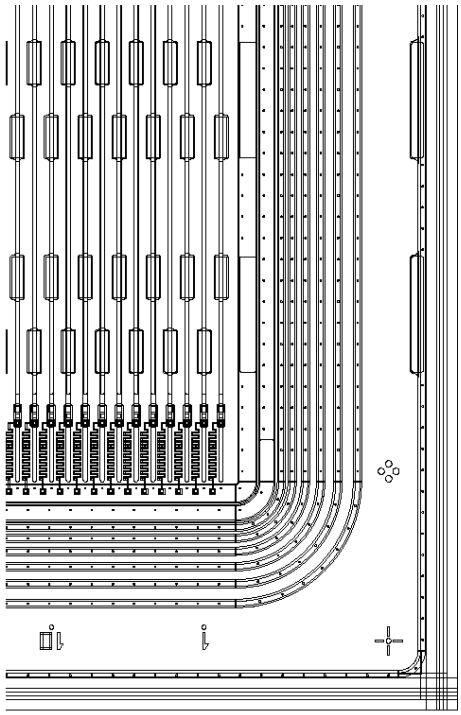


Figure 4.8: A corner of an ATLAS SCT silicon microstrip detector. Six rounded guard rings are seen towards the edge. The polysilicon resistor for each strip is seen in black at the end of the strip. Each metal strip has two bond pads for redundancy.

4.6 Readout concepts and chips

The collision frequency of 40 MHz makes is impossible to transfer data from the front-end circuits in between collisions at this speed. For the SCT with just above 5 million channels it would mean a data rate in excess of 25 Tbyte per second. To avoid this rate the front-end chips buffer/pipeline the data from each bunch cross-over (BCO) for about 2.5 μs. Trigger logic will decide within this time span if the event was interesting or not, and if it was found interesting the data corresponding to the correct BCO will be retrieved from the end of the pipeline. Most of the data exiting the pipeline is not accompanied by a trigger and therefore regarded as background.

The first level trigger has an average rate of maximum 100 kHz, effectively reducing the data rate by a factor of 40. In ATLAS there will be three levels of triggers. The mentioned level 1 trigger will have a fixed delay of about 2.5 μs and will be taken based on calorimeter and muon spectrometer data only. The level 2 trigger also adds inner detector data. The buffering of level 2 is based on digital memories and has a latency of 1 to 10 ms. The level 3 trigger is based on a switched processor farm capable of building full event data, and will be able to write 10 to 100 Mbyte of data to disk per second. The schematic overview of the trigger decision logic is shown in figure 4.9.

In the early phase of the project several readout concepts where put forward, named

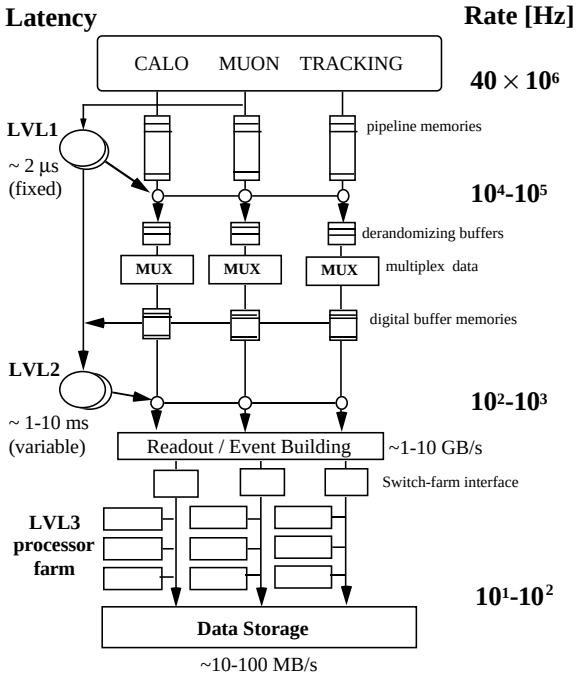


Figure 4.9: Schematic overview of three-level event trigger selection in ATLAS.

analogue, digital and binary. The first case involves reading out sequentially an analogue value for the channels of the hit chip. The digital case requires an ADC in the front-end chip such that the converted digital value can be transferred over a faster digital link. In the end, the binary scheme was chosen. For each BCO the signal output of each front-end channel is compared to a fixed threshold. If the signal is above a set threshold a hit is marked in the pipeline for the corresponding strip. The pipeline memory will buffer the hit pattern until the level 1 trigger decision has been taken.

Several chips have been constructed for the binary read-out scheme. These have mainly been based on two different approaches, either front-end and pipeline in two separate chips or in the same chip. The noise and power requirements at 20 ns shaping time forces the need for a bipolar front-end [46]. The pipeline is however easily accommodated in much simpler and cheaper CMOS technology.

The separate chips solution evolved through chips like LBIC and CDP to todays two-chip solution; the CAFE in the CB2 process by MAXIM (for the front-end amplifiers) and ABC in the RICMOS-IV process by Honeywell (the pipeline).

The second approach is to use new technology offered by rad-hard BiCMOS processes like DMILL (silicon-on-insulator hardening) 0.8 μm commercially available by Temic/MATRA MHS. The ABCD chip (several iterations) has emerged through designs called SCT128B and SCT32B. To get a deeper understanding of the functionality of the read out chips, the ABCD chip is described in further detail in the next section.

4.6.1 The ABCD chip and the readout protocol

The signal processing chain of the chip is as follows [47]:

- Charge integration in 128 parallel front-end amplifiers connected to 128 silicon strips of a sensor, followed by a fast shaping. The gain should be 160 mV/fC and the peaking time 20 ns.
- Threshold discrimination, provided by an internal DAC. In the ABCD3 there will be a separate threshold DAC for each channel to overcome problems caused by process variations. The default threshold is 1 fC, close to 30% of a MIP, and the DAC resolution is 0.025 fC.
- The outputs of the discriminators are latched and sampled by the pipeline at the start of a clock cycle.
- When the chip receives a level 1 trigger it must copy the corresponding data set and its neighbours from the pipeline to the readout buffers, which also serves as the de-randomizing buffers.
- Data can be transferred out of the chip when the chip receives a token, as described by the ATLAS protocol.

The main design goal is less than 1500 e^- of noise after receiving the total anticipated 10 year radiation dose. The ENC noise is here given with the detector (12.8 cm) connected.

Two other important design goals for the front-end are time-walk and double-pulse resolution. The energy deposition is Landau-distributed and signals far above typical MIPs of 3.6 fC can be found, giving pulses with faster peaking than the nominal. A design goal is that this peaking time-walk is within 16 ns so that one is guaranteed that the particle is time stamped to the correct BCO (bunch-cross-over). The double pulse requirement is 50 ns, meaning that particles with this time separation should give two distinct pulses to the discriminator.

The physical size of the first ABCD chip was 6.35 mm by 7.5 mm, increasing to 6.5 mm by 8.2 mm in the ABCD3 soon to be produced. The layout of the ABCD chip is shown in figure 4.10, and table 4.3 explains the most important chip signals.

The chip supplies have large or double pads at both chip sides to lower supply inductance and to provide redundancy.

The clock and command signals for each chip arrive from both the associated opto-board and from the opto-board of the neighbouring module. The chips of the module can select which clock/command to use, giving redundancy in the case of an opto-board failure.

A module consists of 12 ABCD chips, where the readout progresses by token passing, requiring some form of redundancy in case one of the chips should fail. Each chip is therefore equipped with an extra set of token/data inputs/outputs, so that it can be bypassed in the case of chip failure. Only one chip per hybrid is configured as a master, and will pass around the token to collect the data from the other chips, before sending out

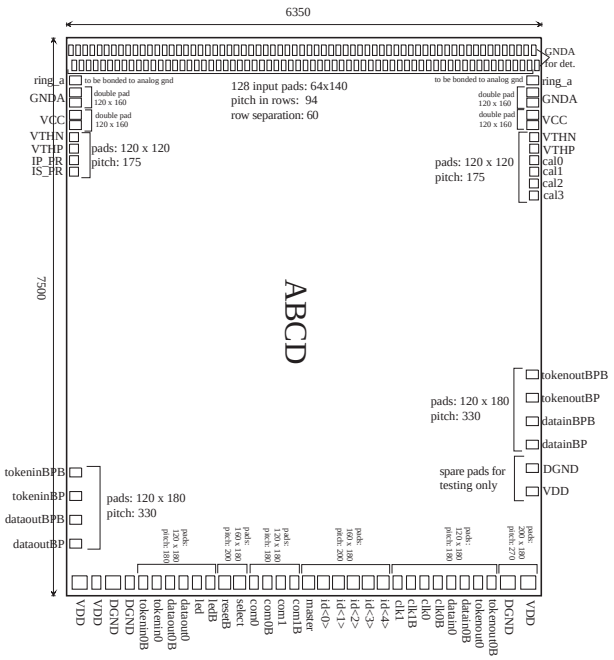


Figure 4.10: Layout of the ABCD chip.

Signal	Type	Description
VCC	supply	Analogue chip supply.
AGND	supply	Analogue ground.
ring-a	screen	Analogue screen connect to AGND.
VDD	supply	Digital chip supply.
DGND	supply	Digital ground.
VTHx	analogue in	External provided threshold.
calx	analogue in	External provided test pulsing.
tokeninx/tokenoutx	digital in/out	Token part of the data stream.
datainx/dataoutx	digital in/out	Data part of the data stream.
led/ledb	digital out	Data from the master chip to the opto board.
clkx	digital in	Clock for down-loading commands to the chips.
comx	digital in	Data for the down-loaded commands.
master	digital in	Decides if the chip is a master.
id[x]	digital in	Decodes the chip position on the hybrid.
select	digital in	Select which clock/command set to use.
resetb	digital in	reset the chip.

Table 4.3: The signal lines of the ABCD chip from the chip specification.

the full data package to the opto-board, which will send it on a opto-cable out of the inner detector.

There exists a possibility of providing the threshold and the test pulsing of the front end externally, in case the internal DACs for these purposes should not be working.

First changes to the ABCD were made since the detector option was changed from n-in-n to p-in-n. It was also clear that results obtained by SCT128B, produced by LETI before DMILL was commercially available, could not be fully used. With the SCT128B that used another substrate best results were obtained by letting the chip substrate float. The ABCD2 gave in the beginning poor results, and it was not able to work with the highest gain (design value of front-end current) without oscillating. This was attributed to an unwanted coupling between front-end and the digital back-end. Better results were obtained by metallizing the chip backplane and connecting it to analogue ground. Even better results were obtained by thinning the substrate before metallizing. In this way it was possible to operate the chip at the highest gain without oscillation. Some other results were also not so encouraging. Process variations were rather large, and it was decided that an acceptable solution would require separate threshold DACs to compensate for channel-to-channel variations. The ABCD3 chip will incorporate separate threshold DACs. Simulations with the actual process parameters also indicate that the phase margin of the front-end is too small. This means that the front-end is close to oscillation. The phase margin will also be improved in the ABCD3. The size increase is mostly due to new resistor technology, the separate threshold DACs and an increased input pad pitch of 48 μm.

4.7 The ABCD hybrid schematic

The schematic for the ABCD hybrid is given in figure 4.11. All connections to the chip symbols indicate a bond, except for the **master** and **id[x]** connections. The **master** bond should only be made for the leftmost chip on the hybrid, the one controlling the actual readout and delivering data packets to the opto board. The **id[x]** defines the geographical placement of the ABCD chip on a module. The id[0] is the least significant bit in a 4 bit chip address. Each of the 12 chip has its own number, the chips on the top hybrid are numbered 0 to 5 and on the bottom hybrid from 8 to 13. This strange numbering just ensures that the three lower order bits are the same on the top side and bottom side hybrid of a module. If a bond is made the id[x] line is tied to ground, and is hence logical low, if the bond is not made the internal pull-up resistor on the chip will hold it at logical 1. For instance will chip 5 have address=id[3]id[2]id[1]id[0]=0101, being the binary number 5. The id[4] bit is special, being 0 on modules called even and 1 on modules being odd. Every other module along the barrel axis is even and odd.

Most of the lines on the hybrid involves the passing of the token and data between the chips. These are differential low voltage swing (LVDS) signals. To achieve full redundancy to a single chip failure, two groups of tokens/data (total of 8 lines) must pass between the two hybrids. The addition of bond pads into these tracks are introduced since the top and bottom hybrid of a module are made identical. The top hybrid will have only the left group of bond pads bonded, whereas the bottom hybrid will have the right group bonded. This ensures that the chips connected to these lines will not have to drive unnecessary long tracks (capacitances), and to reduce noise. The redundancy scheme is indicated in

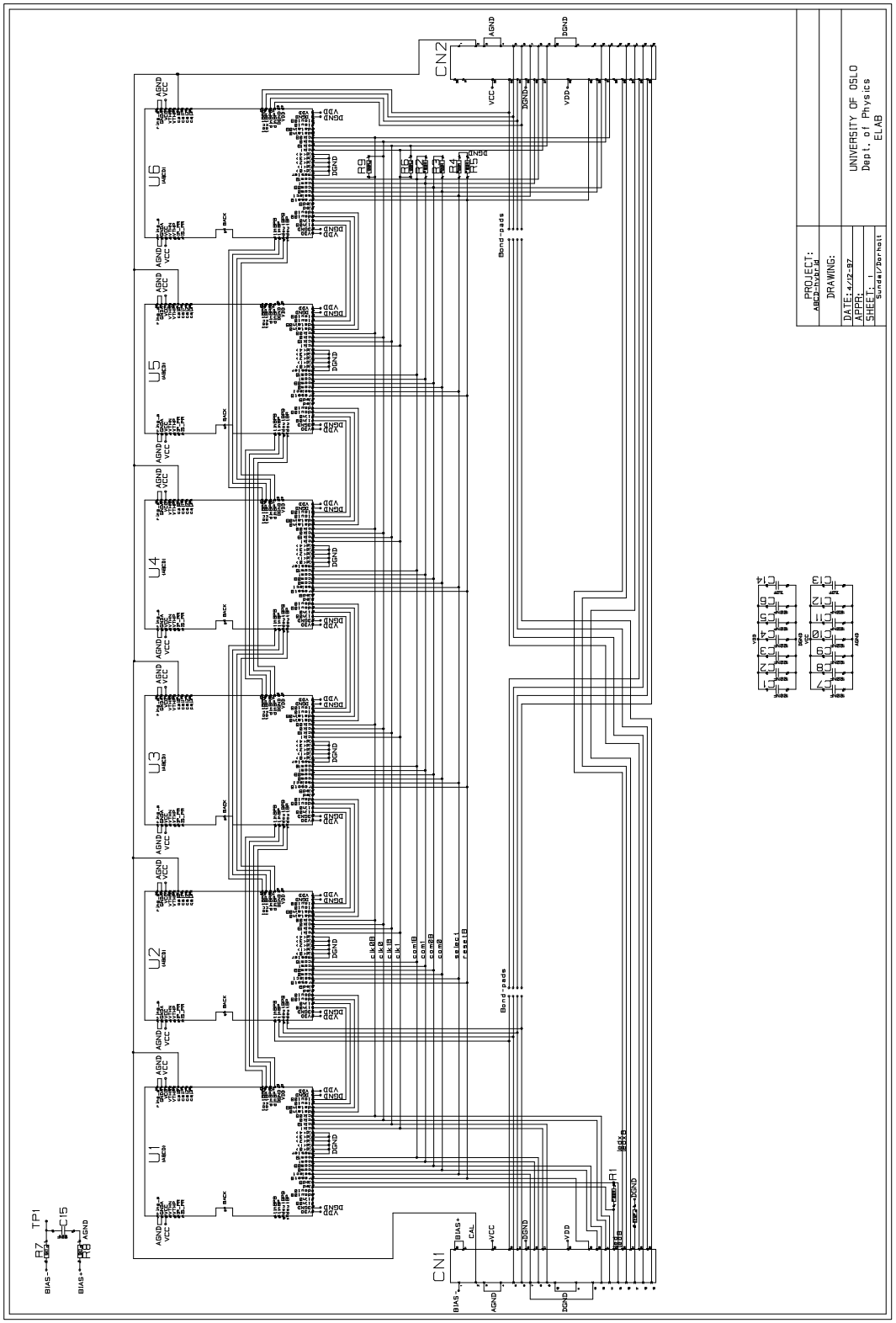


Figure 4.11: Schematic of the ABCD BeO hybrid.

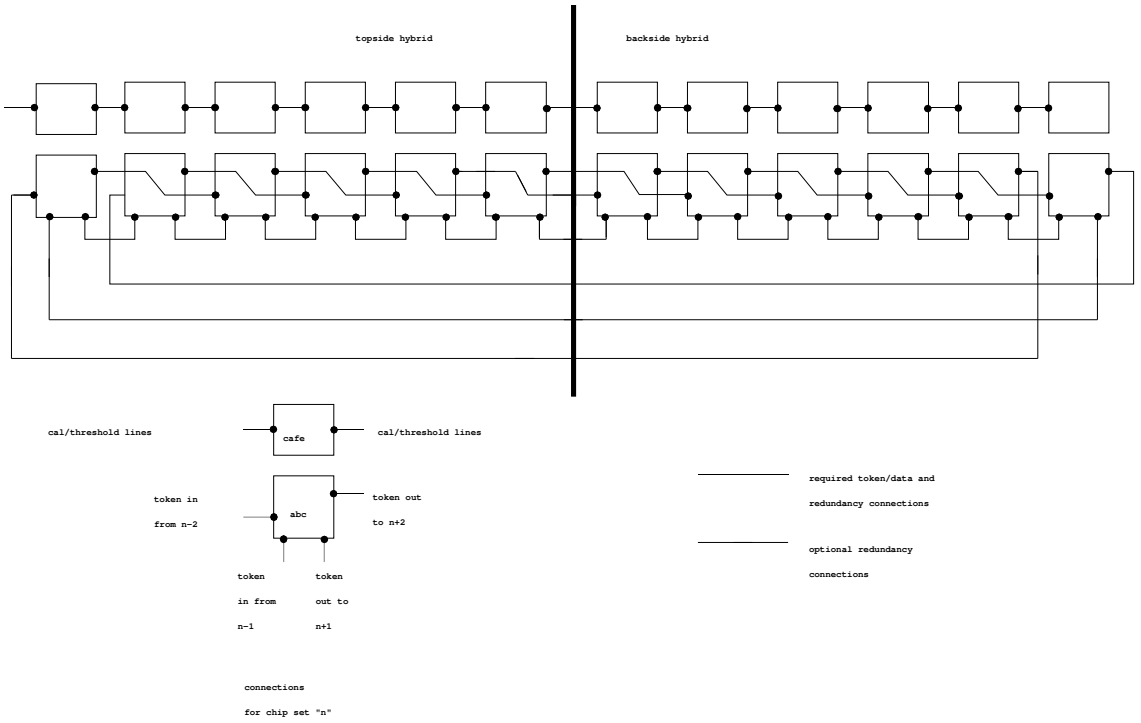


Figure 4.12: Redundancy scheme for chip data/tokens in the two hybrids of a module.

figure 4.12. The differential clock and command signals arrive from the opto-board and must be terminated in 100 Ω resistors.

The pig-tail connection to the first hybrid will not contain any of the data/token lines, but instead two groups of led/ledb lines. The master chip (first chip) on the top hybrid will transfer data to the opto-board over the led/ledB connection for all 6 chips on the top side, whereas the ledx/ledbx will pass the same data from the bottom hybrid straight through the top hybrid. Also the led/ledb signals are of LVDS type. The connection between the hybrids are through a short wrap-around kapton cable.

The ground for the analogue and digital part of the front-end arrives separately on the cable. The grounds can however be joined together by bondings at positions between the chips. Results by both SCT128B and ABCD have all been best with the analogue and digital ground connected together at the hybrid.

Biasing of the detector is brought in on the upper end of the input connector for the top hybrid. It is well separated from other tracks on the kapton pig-tail to avoid high voltage breakdown. The detector bias is decoupled with two resistors and one capacitor on the upper left end of the hybrid. The full detector decoupling scheme involves one more capacitor and two resistors, which needs to be placed on the pigtail cable close to the hybrid, for this particular hybrid solution.

The detector decoupling has been through heavy discussions in the last few months. It was found more or less impossible to have the metallized ABCD2 chips working in a single sided module, when going from 6 cm to 12 cm long detector strips. By introducing

a resistor in series between the backplane and its decoupling resistor, better results were obtained. My feeling is that this should not be taken very seriously before the results with the ABCD3 are available. This is probably an effect of the small phase margin in the ABCD2. The newest thick-film/ceramic hybrid for the ABCD3 was made such as to optimize the electrical properties and not the material budget. Thicker ground/power planes were used and a single ground plane, based on earlier results. Results from the Geneva group [51] with the new hybrid and thinned metallized ABCD2 chips reveal a little improvement over the old ABCD hybrid. Again this is felt by the author to be more dependent on the quality of the ABCD2 and not on the actual reduction in impedance and resistance of the chip ground.

4.8 Electrical and optical connection strategy

In a large system like the SCT, one of the major problems is to minimize common mode noise, which is potentially very dangerous for both front-end and high-integrity digital data transmission. The common mode noise is typically pick-up noise due to cross-talk between nearby lines or other forms of unwanted signals coupling capacitively or inductively to our system. The most important method to ensure good common mode rejection is to be careful with supply and grounding strategies.

In ATLAS one has chosen a more or less optimal solution to this problem. Each module is supplied by floating power supplies over a separate cable, grounded together and decoupled in a star ground configuration very close to the front end chips. This is also referred to as a 'groundless' system, because there is no common ground for whole sub-detectors, only for individual modules.

To protect the analogue front-end in this system is a rather confined problem, because the sensitive analogue circuitry does not extend further than to the discriminators of the front end chip. This noise can couple to the front end either via the detector or from the digital circuitry to which the front-end is connected. The last problem is taken care of by the ASIC designers, by presenting a high impedance path to the front-end for signals originating in the digital parts of the chip.

External noise can couple to the detector either via the backplane, or via the readout strip and to the input transistor. The backplane is regarded as the most dangerous part, since it involves a large area where all emitters of the silicon strip diodes are connected together electrically. The backplane should be well filtered with respect to the reference ground of the input transistors of the front end chips. In addition should the filtering be as close as possible to the chips to avoid loops or long tracks to introduce unwanted inductive and capacitive couplings.

The whole SCT sub-detector is surrounded by a Faraday shield to shield the SCT and TRT from each other.

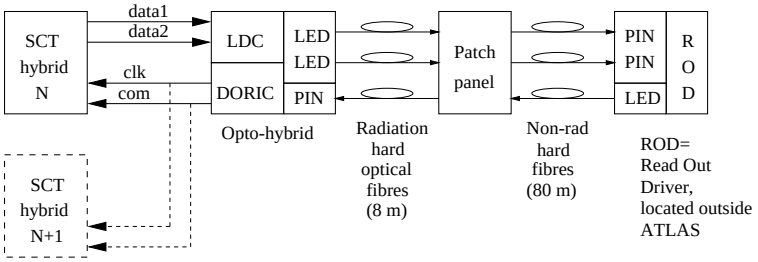


Figure 4.13: Schematic description of the optoelectronic parts for reading out an SCT module.

4.8.1 Optoelectronic components

The module is not connected directly to the power tape low mass cable, but to a copper-on-kapton pig-tail cable from the top hybrid, by a soldered connection. The pig-tail itself is fitted with a connector for attachment to the low mass cable. Also connected to the pigtail cable is the small opto-hybrid, containing all opto-electronic components for the module. The opto-hybrid with an approximate size of 10 by 10 mm, contains three important parts.

The dominant part is a package containing two LEDs for transmitting the module data out of the inner detector over two optical fibers, and one PIN diode for receiving the clock and commands for the module. To ensure long lifetime of the LEDS, the opto-hybrid will have its own cooling contact. To further extend the lifetime a NRZ data transmission protocol is used that minimizes high current-on times for the LEDs, since LEDs only age when they are on.

The second opto-hybrid part is a dedicated LED Driver Chip, LDC, that accepts the two module data streams at LVDS levels and drives the two LEDs.

The third part is the DORIC3 chip to demultiplex the data and commands arriving over the opto-cable. The PIN diode output is converted to a voltage in a trans-impedance amplifier and then multiplied by an AC coupled differential gain stage. Logic levels are produced by a comparator, and the larger part of the chip extracts and synchronizes clock and commands by use of a bi-phase mark decoder. The output clock and command are driven to the module as LVDS signals. A separate control line will tell DORIC to also output clock and command for a neighboring module, to which it is connected. This is a part of the redundancy scheme, since we will not accept the loss of a full module if a PIN diode or a DORIC chip should break down.

Figure 4.13 shows schematically the opto-components described. In addition it shows that expensive radiation hard opto-cables are only used within the detector, whereas from the patch panels to the Read Out Drivers (RODs) in the electronics hut, much cheaper non-radiation hard cables are used.

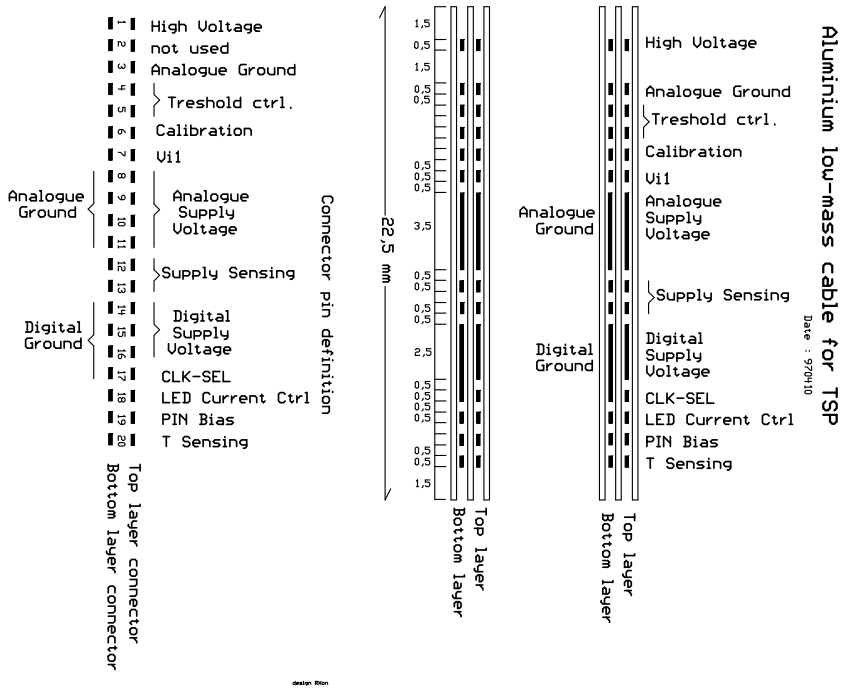


Figure 4.14: Low mass cable for support of one SCT module.

4.8.2 Low mass cables and pig-tails

The cables used for powering the module and also providing some control and monitoring are of aluminum on kapton. Figure 4.14 show an overview of an aluminum power tape cable. In the inner part of the detector the aluminum is 50 μm thick and each of the three kapton layers are 25 μm. Studies have verified all properties of aluminum, kapton and epoxy glues to doses far above the expected LHC dose.

The supplies are analogue and digital low voltages supplies (3.5 V and 4.0 V) for the front end chips. The digital supply is also used by the digital components, LDC and DORIC on the opto-hybrid. A high voltage supply for the silicon detectors and a 10 V supply for the PIN diodes are also present.

For control purposes there are lines both for analogue and digital parts. There are lines for providing the threshold, a control current and calibration pulses for the front-end chip. With a working ABCD chip, none of these analogue lines are required. There is also a biasing line for the current in the LEDs. The digital control line is to allow the DORIC to drive clock/commands for the neighboring module.

For monitoring purposes, space for temperature and front-end supply sensing is allocated. The sensing allows one to exactly set the wanted front end voltages since the typical voltage drops over the cables are easily above 0.5 V.

4.9 Potential hybrid technologies

The read-out hybrid is an integrated part of the module, and the same overall goal exists. The material must be minimized such that tracking is not ruined by multiple Coulomb scattering in the hybrid material. The material optimization is however constrained by the fact that the module should operate correctly. Sacrifizes can not be motivated if they jeopardize the electrical, mechanical or thermal properties of the module.

The main objective of the hybrid is to function as the carrier for the front-end chips. The hybrid must be mechanically stable to hold a fixed position with respect to the sensors, otherwise the bondings in between would snap. It also needs to be a good heat conductor to transport the chip heat to the cooling pipes. The electrical properties of the hybrids must be excellent to achieve high integrity signals from a system of mixed high speed digital and low level analogue signals. The last point has received a lot of attention for the ABCD2.

There are three main technologies to choose between for the ATLAS SCT hybrids [49]:

- Thick film on ceramic substrates.
- Laminated copper-on-kapton hybrids on-top of beryllia/beryllium/TPG substrates.
- Aluminum-on-polyimide(kapton) hybrids laminated onto PG/TPG.

The first solution is the industry standard and it has been used in several physics experiments, like the silicon detectors for LEP. It is highly reliable for long term operation, examplified by known reliability of soldering and bonding. The community has long experience in assembly and use of such hybrids. The second solution includes two hybrids and the cables in one kapton piece. This is highly interesting for the barrel section, where the pig-tails and wrap-arounds feels very clumsy for the thick film solution. In the forward modules the possibility of having holes through the substrate make the thick-film solution more attractive. This is attributed to the fact that the modules are end-tapped and a single substrate is the natural configuration. The third solution is a new process under R&D by CERN and French industry. It has the best electrical and thermal properties, and can offer an integrated fan-in. However no experience with long term stability exist.

My work has mainly been linked to the thick-film on beryllia solutions. The goal has been to find thick film processes and techniques that allow the production of a hybrid with acceptable radiation thickness, since this is the main design goal. Calculations and measurements have been performed to check that this gives acceptable electrical parameters.

4.9.1 Passive hybrid components

All hybrid solutions require in the order of 20 passive components to be mounted. For all of them it applies that they are selected in the smallest series that can accomodate the required component value, to minimize hybrid size and material.

Some resistors are needed for the purpose of line termination. LVDS signals are used for clocks and commands. These should be terminated differentially in 100 Ω. Due to the very

low swing, these resistors can be in very small series like 0402, minimizing material, since very little heat is dissipated. The only other resistors are series resistors for the detector biasing. These resistors are in the order of 10 kΩ and the detector decoupling capacitor about 10 nF/500 V in 1206 series, giving the knee frequency of the low-pass filter of a few kHz. The series resistors will also reduce the current flow in the detector in case of shorts or break-downs.

Upon entering the hybrid the analog and digital supplies are decoupled. The decoupling scheme would typically be a SMD mounted tantal capacitor. The tantal capacitors are rather big and clumsy. In the series EIA3528 (3.5 mm by 2.8 mm by 1.9 mm thick) KEMET has 4.7 μF at 10 V. It is now possible to get 2.2 μF X5R as a replacement for 4.7 μF tantal. The size is 1206 or about 3.0 mm by 1.5 mm. The ceramic X5R capacitors have fewer breakdown modes, should be more radiation hard and there are no problems with voltage polarities.

The remaining capacitors are for local decoupling of each front-end chip. In the ABCD hybrid two X7R 100 nF SMD capacitors in the series 0603 are fitted next to each chip to decouple analogue and digital supplies. The material for the chip decoupling capacitors should be X7R. Another commonly used type is Z5U, should not be used for applications below zero degree centigrade, which is the case in ATLAS. The main material is barium-strontium-titanate, $Ba_xSr_{1-x}TiO_3$, with x in the range 0.6 to 1.0. This is a ceramic material and should be highly radiation hard. The reduction in the nominal value of the capacitor at $-25°C$ is less than 10%, which is uninteresting for decoupling purposes. The most important failure mode is crack formation. For uniform heating the capacitor is better to withstand compression than tension. A favourable property since the thermal coefficient of expansion (TCE = 10 ppm/K) is higher than that of a beryllia substrate and its aluminum-oxide layers (both TCE = 6 ppm/K) [48].

For the mounting, solder is preferred over conducting glue. The chips and the fan-ins are the only exceptions. The chips should be glued to its pad with a conducting glue, for example silver epoxy. The radiation hardness of epoxy glues have been verified inside the community [44, chapter 11].

In thick film processing, resistors and capacitors can be printed, using the same printing steps as for conductors and insulators, by using other printing pastes to achieve the wanted conductivity or dielectric value. This is not found worthwhile due to the additional cost introduced. The material contribution by surface mounted components is not very large. The contribution of about 30 decoupling capacitors to the radiation length, averaged over the module area, is around 0.03%.

4.10 An example thick film on ceramic hybrid

In the center-tapped bridge type module, the length of the hybrid will have to be at least the 63.6 mm of the detector, adding about 5 mm in each end for the contact to the support structure, which provides the cooling and space for the connection of the pig-tail and wrap-around cables. The width of the hybrid is limited by the place needed to route the internal

buses on the hybrid and the space for the chips. In the Inner Detector Technical Design Report (TDR) [44] 28 mm was specified. This width was limited by the proposed footprint for the pig-tail cable. Copper-on-kapton hybrids which incorporate cables and hybrids into one integrated piece, will however not need more than 22.5 mm. The same applies for the aluminum-on-polyimide hybrids, where the connections between cables and hybrids are made by bondings. This width can not really be further reduced since it is required to have a good cooling contact.

The starting thickness of the beryllia substrate is 890 μm (35mil) before machining. The piece is machined such that it obtains a bridge shape. The thickness of the bridge is 380 μm (15mil). When the hybrid sits across the detector there will be a height difference of about 0.5 mm, which should give enough headroom for hybrid bending and room to avoid heat exchange by convection. The substrates are guaranteed by the vendor to the specified thickness $\pm 50\,\mu$m.

4.10.1 Hybrid materials and layout

The choice of ceramic is relatively simple. The two most used substrates are alumina and beryllia. Except from the cost, a beryllia substrate is much better with respect to radiation length (about twice as good), thermal conductivity (6 times as good) and thermal expansion (closer to silicon than alumina). With alumina these figures are so bad that a working module with respect to acceptable values of radiation length and thermal conductivity would not be possible. The higher price of the beryllia is mostly connected to the fact that its dust is poisonous.

The conducting elements used commercially today are mainly silver-palladium (AgPd), silver (Ag), copper (Cu) and gold (Au). Copper oxidizes in air at high temperatures and the printed layers need to be fired in a nitrogen atmosphere, which increase the cost of this process.

Silver-palladium has a very high sheet resistivity around 25 m$\Omega/\Box$ for a typical conductor thickness of 15 μm. This can give a considerable voltage drop on the supply line to the current hungry front end amplifiers. Typical sheet resistances for the other materials are a factor 10 lower for ordinary thicknesses.

Gold and silver are both good conductors. Gold has been the traditionally favorable choice for at least three reasons:

- It is cheaper, because the insulation printing requires three prints for silver and two for gold. The thickness of each print is usually around 15 μm.

- Even when silver is used, a mask with gold for the bonding padsis needed. This is not easily done since diffusion problems imply that the the gold and silver cannot be in direct contact, requiring a diffusion barrier. This barrier is typical AgPt. To have only a part of a layer in gold, and the rest of the layer in silver implies a print with short stubs of track of AgPt joining the silver and gold. If one full layer of gold is printed it must be the top layer since a silver layer above a gold layer can

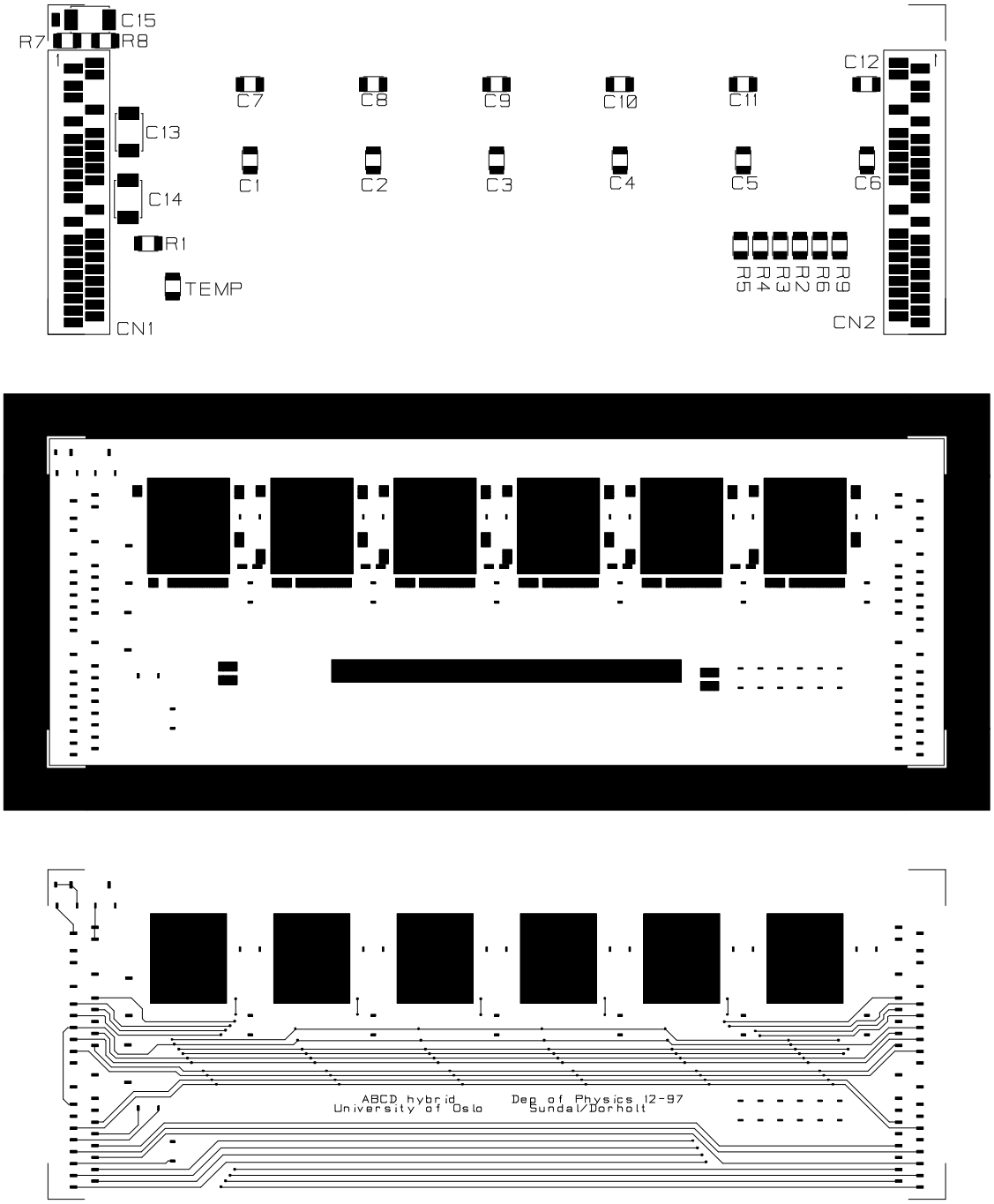


Figure 4.15: BeO hybrid for the ABCD chip. The first plot shows the solder pads with component names, the next layer is the insulation between solder pad and top routing layer and the bottom plot is the top routing layer.

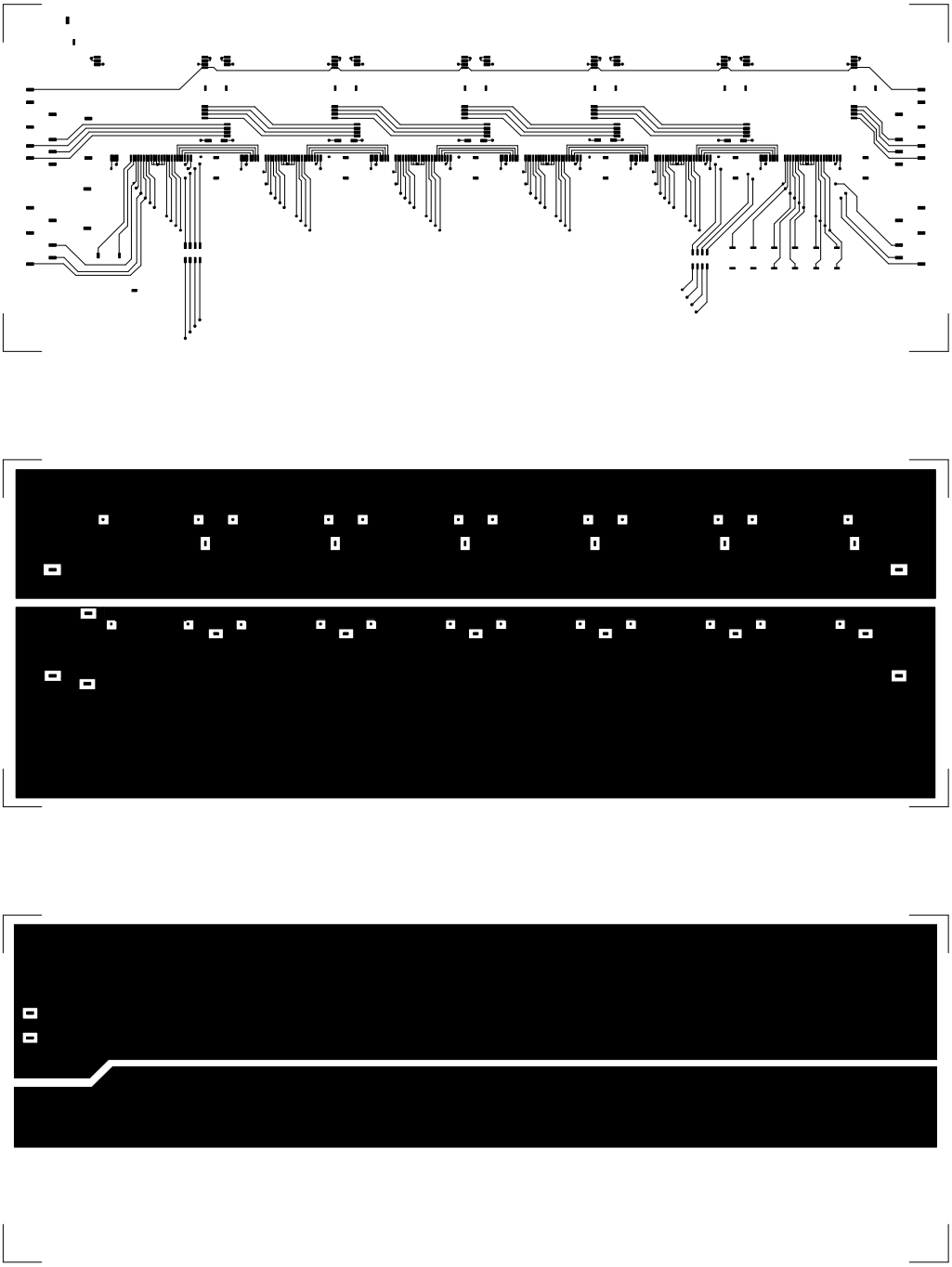


Figure 4.16: BeO hybrid for the ABCD chip. Bottom three electrical layers. From top; bond layer, ground plane and power plane. The bottom shield, which is a full plane, is not shown.

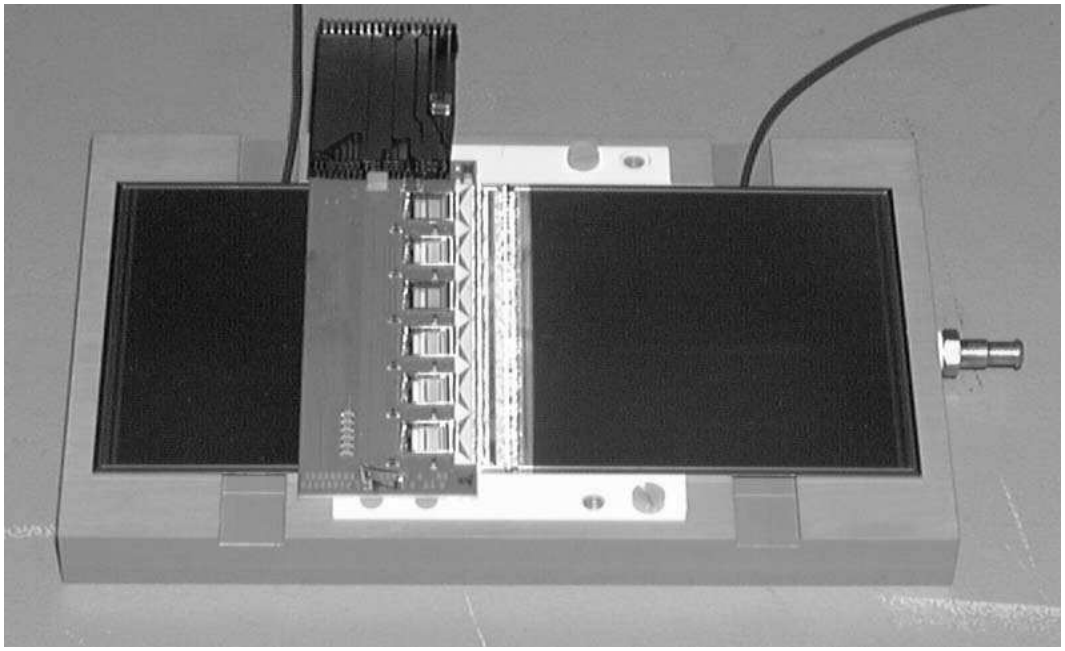


Figure 4.17: A single sided module based on a BeO hybrid for the ABCD chip. Picture by the Geneva SCT group.

cause problems. In this latter case the diffusion barrier is made by printing the vias between the gold and silver layer in AgPt.

- Gold can be printed down to thicknesses of 1 to 3 μm, which is much less than the typical 15 μm of silver. Some vendors could possibly print the silver down to a thickness of 8 μm. Even though the radiation thickness of gold is very bad, about 2.5 times worse than silver, this is won back by the fact that 8 μm silver is about 2.5 times as thick as 3 μm of gold.

ESL's gold paste ESL8837 can typically be printed to a thickness of 1.5 μm. Two prints of this would give a typical thickness of 3 μm. These are specifications by Gandis workshop at CERN. In this case no etching is done. ESL themselves typically states this to be a 3 μm thickness, when printed and etched in three rounds. A calculation based on the resistivity of pure gold gives about 8 m$\Omega/\Box$, while ESL list 25-35, 10-15 and 7-10 m$\Omega/\Box$ for 1,2 and 3 prints of their paste, respectively. If this gold is only printed, and not etched, which should increase the amount of potential commercial vendors, the design rules need to be relaxed. Typically one would need at least 100 μm track width and 300 μm pitch. The gold is very pure and not specified for Al-bonding. It implies that the layer with the bond pads must be fully printed with another paste, otherwise a separate print of the bond pads in a bondable gold is necessary.

A good bondable gold is ESL8881b. It gives typically 8 μm thick conductors. A good property of this gold is that it can be printed at 100 μm track width and 200 μm pitch, which is favorable since the whole hybrid can be printed (no etching, which increases the

number of potential vendors). In addition are the chip bonds easier, since the bond pads are tightly laid out on the chips. Gandis workshop can even print this gold at 4 μm thickness by thinning the paste. This is probably not a wise solution, since most vendors probably would not like to do this. The solder pads on top are made of AuPd, ESL5837 printed at 18 μm thickness.

Based on all this information a favorable build up of the different layers for the ABCD design is given in the following list (bottom to top), and the layout plots of some layers are presented in figure 4.15 and figure 4.16. Figure 4.17 shows a picture of a single sided module using an ABCD hybrid.

- The bottom shield for stopping capacitive coupling to the detector can be implemented as one print of ESL8837. It must be covered by dielectric before the next electric layer. The shield should have a one-via connection to the ground plane.

- The bottom layer is the power plane split into areas for VCC and VDD. VDD is not using as much current and can be gridded. The plane do not need to cover the whole hybrid. No fine lines are required and the layer can be made using only printing. 3 μm ESL 8837 could be used.

- The ground plane. It could be a whole plane under the chips in the whole length of the hybrid and then gridded for the rest of the hybrid, or it could be gridded all over. 3 μm ESL 8837 could be used.

- The bottom route, where the bonding goes. This is 8μm ESL8881b. Mostly stub routing from buses to the chips, a very few analog lines from end to end. The conducting area is only a few percent (in order to defend the use of such a thick gold). Close to the chips as little as 100 μm track and spacing could be used.

- The top route. All the (long) digital bus lines are found here. In this way these are lifted high above the ground plane to reduce the capacitive coupling between ground and the fast digital signals. Here at least 100 μm track and 200 μm spacing should be used, in order to print this layer with 3um ESL8837.

- Solder pads in 18 μm AuPd (ESL5837).

- For the dielectric two prints of ESL4905CH could be used, giving about 35 μm thickness.

The effect of capacitive coupling between the digital signal lines is reduced in one of two ways. The easiest one is to increase the distance between signal lines and the ground plane, the other one is to print the dielectric using a paste with low permittivity. Paste with permittivity of about 4 exist, compared to 9-10 as typical values. This dielectric is more volatile, which requires the vias between layers to be much bigger. This is a potential problem around the chip bond pads, where very little space is available. Typical electrical parameters can be estimated, if one assumes that the digital buses are micro-strips, 150 μm

wide, 70 μm above the ground plane, 3 μm thick, and that the relative permittivity is about 9. The characteristic impedance will be about 35 Ω, the capacitance about 2 pF/cm and the resistance about 50 mΩ/cm.

In an attempt to cut cost one could go to an automated 3 μm silver process for the printing of all layers, except for the bonding layer which must be in gold and put on top. This gives a saving in both production and material since silver paste cost typically 3 CHF/gram, while gold cost 50 CHF/gram. In this case the design rules will be 300 μm track, space and via sizes. In this process there are only 2 insulation prints between each conducting layer, and the total thickness of an insulating layer increases to about 40 μm, compared to 35 μm for the gold process [50]. There are also indications from the vendors that some of the limitations in the standard silver processes are relaxed [49], that could make silver a more attractive solution.

4.10.2 Radiation thickness of the beryllia hybrid

The radiation thickness of the proposed hybrid is calculated in table 4.4. These numbers are averaged over an area of 63.6 mm by 128 mm or 81.4 cm^2.

Table 4.4 lists material contributions for the hybrids and sensors averaging over 81.4 cm^2 effective module area, with a total of 1.38% of a radiation length. The contribution from each entry as a percentage of a radiation length is given by

$$\%X_0 = \frac{nlwt}{AX_0} \cdot 100\%.$$

A is the effective module area, whereas the rest of the quantities refer to the columns of table 4.4. The columns t, w, l and n refer to thickness, width, length and multiplicity of the item, respectively.

The number column usually refers to the number of items of the given type however it can also include geometrical factors to compensate that the item does not cover the whole area given by length and width.

According to the 070-series of drawings by the SCT community, the baseboard of the module will be made of TPG and the additional facing strips in beryllia. These items are included in the calculations. An exploded view of the module in shown in figure 4.18, the baseboard in figure 4.19 and the beryllia facings in figure 4.20.

A more realistic hybrid with respect to material, that still should behave equally good electrically, would integrate the power as tracks in the bottom route. This is possible since the gold in this layer is much thicker, so that tracks that are not so wide can be used for the supply. In addition have the calculations of the resistance in the power rails on the hybrid indicated that the total amount of gold used in supply and ground can be halved. The removal of the supply plane also means that one less insulation layer is required per hybrid. In addition can the shield be printed on the bottom side, with a via connection through the substrate. On the uppermost insulation layer one can remove material where there are no solder components to be placed, effectively reducing the insulation to 75%. With these changes the hybrid printing is down to 0.18% and the module is 1.26%.

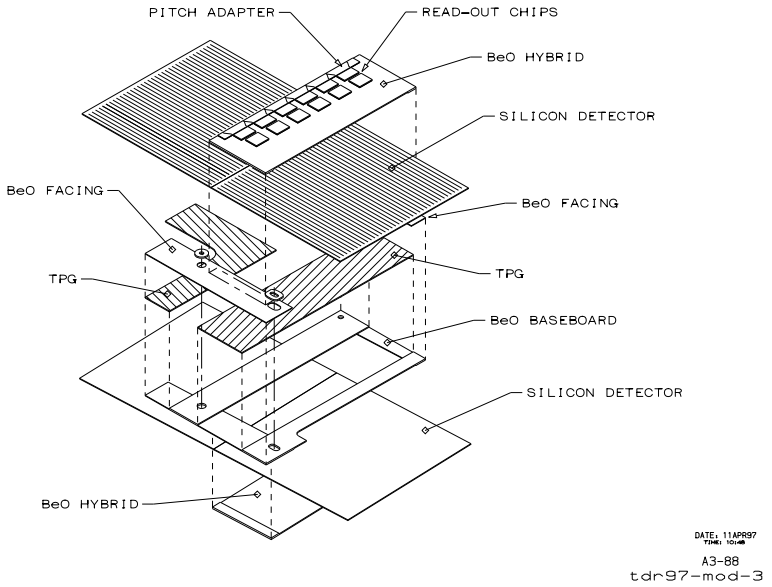


Figure 4.18: Exploded view of an ATLAS SCT silicon strip barrel module.

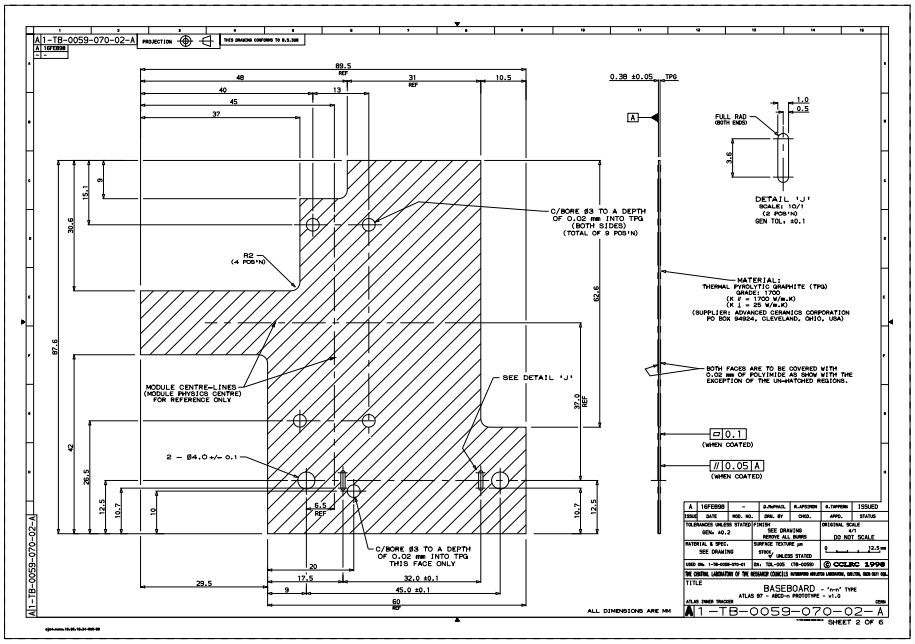


Figure 4.19: TPG baseboard design for the ATLAS SCT barrel module.

A more bold proposal is to produce different hybrids for top and bottom side of the module. This allows the use of 8 fewer signals on the connectors and the width can shrink from 28 mm to 24 mm. This should be a sufficiently wide cooling contact. The saving from the substrate, insulation printing and metal printing is around 0.044%, and the module is down to 1.22%, which is very close to the design goal of 1.2%.

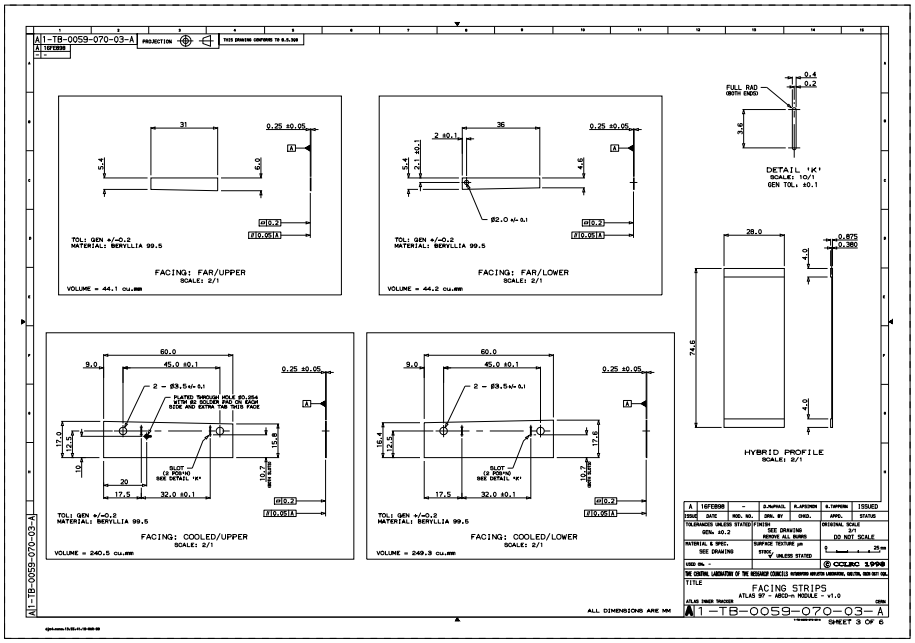


Figure 4.20: Beryllia facings for the ATLAS SCT barrel module.

It is seen from the optimized module that the sensors contribute about 50% of the module. For a hybrid, the substrate, the insulation printing, the conducting printing and the components contribute about the same amount. If dielectric paste with much less barium oxides and zinc oxides and more boron oxides and aluminum oxides could be found, this would help a little. Such a paste would probably just have higher aluminum oxide fraction and the result could not improve much more than from 60 mm to aluminum oxides 70 mm, a mere 20% reduction in the insulation and an 1% reduction in the total sensor and hybrid material.

Table 4.5 and table 4.6 [7] show calculations of radiation lengths for typical conductors and insulators used in the hybrid printing. The weight percentage before firing is less than 100, since there are organic solvents which gives the paste its viscosity needed for printing. The solvents evaporate during firing. The formulas used are given in section 1.2.2.

4.11 Thick-film, thin-film comparison

In describing the aluminum/polyimide hybrid it is sufficient to describe more or less the difference between this technology and the gold/oxide technology. The finished aluminum/polyimide hybrid is thin and flexible, and can be laminated onto various substrates. In our case where the heat removal is important the proposed substrate is TPG, even though the first demonstration module used a PG substrate.

The process is based on photo-lithography like the thick film solution, but the similarities end here. The difference lies in the production. In a thick film process the photo-mask

Part	Material	X_0	t	w	l	n	% X_0
MECH./THERMAL							
baseboard+facings	BeO/TPG						0.166
SENSORS							
the 4 sensors	Si	93.6	0.285	63.6	64.0	4	0.6090
HYBRIDS							
Substrate							
hybrid substrates	BeO	144.0	0.381	28.0	74.6	2	0.1358
bridge ends	BeO	144.0	0.495	28.0	4.0	4	0.0189
Substrate total							0.1547
Printing							
insulation layers	dielec	60.0	0.035	28.0	74.6	10	0.1497
bottom shield	Au	3.5	0.0015	27.8	74.6	2	0.0218
ground plane	Au	3.5	0.003	27.8	74.4	2	0.0436
power plane	Au	3.5	0.003	27.8	74.4	2	0.0436
top layer route	Au	3.5	0.003	0.15	1200	2	0.0038
bottom layer route	Au	3.5	0.008	0.1	1000	2	0.0056
pads for chips	Au	3.5	0.003	6.35	7.5	12	0.0060
pads for cable	AuPd	3.5	0.018	1.52	0.76	60	0.0105
pads for 0603 SMD	AuPd	3.5	0.018	1.0	0.60	104	0.0061
Printing total							0.291
Components							
ABCD chips	Si	93.6	0.35	6.35	7.5	12	0.0263
0603 ceramic caps	X7R	20.0	0.8	0.8	1.6	24	0.0151
0603 resistors	Al_2O_3	35.0	0.5	0.8	1.6	14	0.0031
1206 ceramic caps	X7R	20.0	1.5	1.6	3.2	2	0.0094
1206 main decoupl.	X5R	20.0	1.5	1.6	3.2	4	0.0189
fan-in	glass	123.0	0.381	3.3	61.8	2	0.0155
wraparound cable	kapton	287.0	0.025	24.0	11.0	1	0.0003
pigtail cable	kapton	287.0	0.025	24.0	20.0	1	0.0005
wraparound cable	Cu	14.3	0.005	24.0	11.0	1.6	0.0018
pigtail cable	Cu	14.3	0.005	24.0	20.0	1.6	0.0033
bond wires	Al	89.0	0.025	0.025	3.0	5000	0.0013
conducting epoxy	Ag	8.54	0.025	6.35	7.5	12	0.0206
cable solder pads	solder	9.12	0.2	1.0	1.0	108	0.0291
equiv. 0603 pads	solder	9.12	0.1	0.8	0.8	108	0.0093
Components total							0.1545
MODULE							1.375

Table 4.4: A calculation of the radiation length of an unoptimized ABCD module. The result is averaged over a module area of 81.4 cm^2.

is used to produce a very fine steel mesh, through which a viscous paste, either for an insulating or conducting layer, can be pressed/printed. The paste containing organic solvents for viscosity, binders and the active material, oxides for insulators and gold/metals for conductors. After the printing the hybrid is fired at high temperatures, around 900° C,

Component	Weight % in paste	Weight % after firing	Density % (g/cm^3)	Rad.length (g/cm^2)	Rad.length (cm)
Au	80-90	~98	19.3	6.43	0.33
CdO (binder)	2	~2	~7.5	10.1	~1.35
Average			18.7	~6.48	~0.35

Table 4.5: Composition of a paste for conductors. These are typical values for gold paste.

Component	Weight % in paste	Weight % after firing	Density (g/cm^3)	Rad.length (g/cm^2)	Rad.length (cm)
Al_2O_3	30-40	~47	4.0	28	7.0
BaO, BaO_2	10-20	~20	~5.3	9.6	~1.8
B_2O_3 (glass)	5-15	~13	1.8	39	21
SiO_2	5-15	~13	2.2	27	12
ZnO	5	~7	5.6	15	2.6
Average			~3.3	19.8	~6.0

Table 4.6: Composition of paste for insulation. The calculations are based on ABLESTIK paste no. C8301.

which frees the solvents and melts the rest to a fixed hard glass for the insulators or as a metal traces or planes for the conductors. The resulting tracks are not very well defined. This is shown by figure 4.21. The general dimensions given for the process are verified by these pictures. Figure 4.22 shows a cut through a SMD pad with a very huge via connection down to the ground plane. The lowest plane is the power plane sitting directly on the alumina substrate since this hybrid is printed without a bottom shield. The huge amount of gold in these vias indicates that connections from solder pads to a lower layer should not be done this way since it increases material. A better way will be to route a track from the pad in the pad layer to a small standard via going down to the selected layer. The thickness of the AuPd pads is verified to be 18 μm by this picture. These are all pictures taken by a microscope of a cut SCT128B hybrid, having the same buildup as described for the prototype ABCD hybrid.

The aluminum/polyimide process is instead based on etching. The photo-mask is the basis for where to etch away the aluminum. This makes it a much finer process since the etching is very accurate. A printed thick film hybrid can be etched later to improve the quality of the lines, this will however increase the cost and the described thick film hybrids are designed such that only printing is required. In the aluminum/polyimide design it is possible to go down to 50 μm tracks and spacing, but this is only used in the pitch adapter. Using smaller line widths and spacings will decrease the yield, and is therefore not used unless necessary.

An overview of items where the aluminum/polyimide on TPG hybrid is potentially better than the BeO hybrid are:

- The smaller line widths allows the pitch adapter to be integrated into the hybrid.

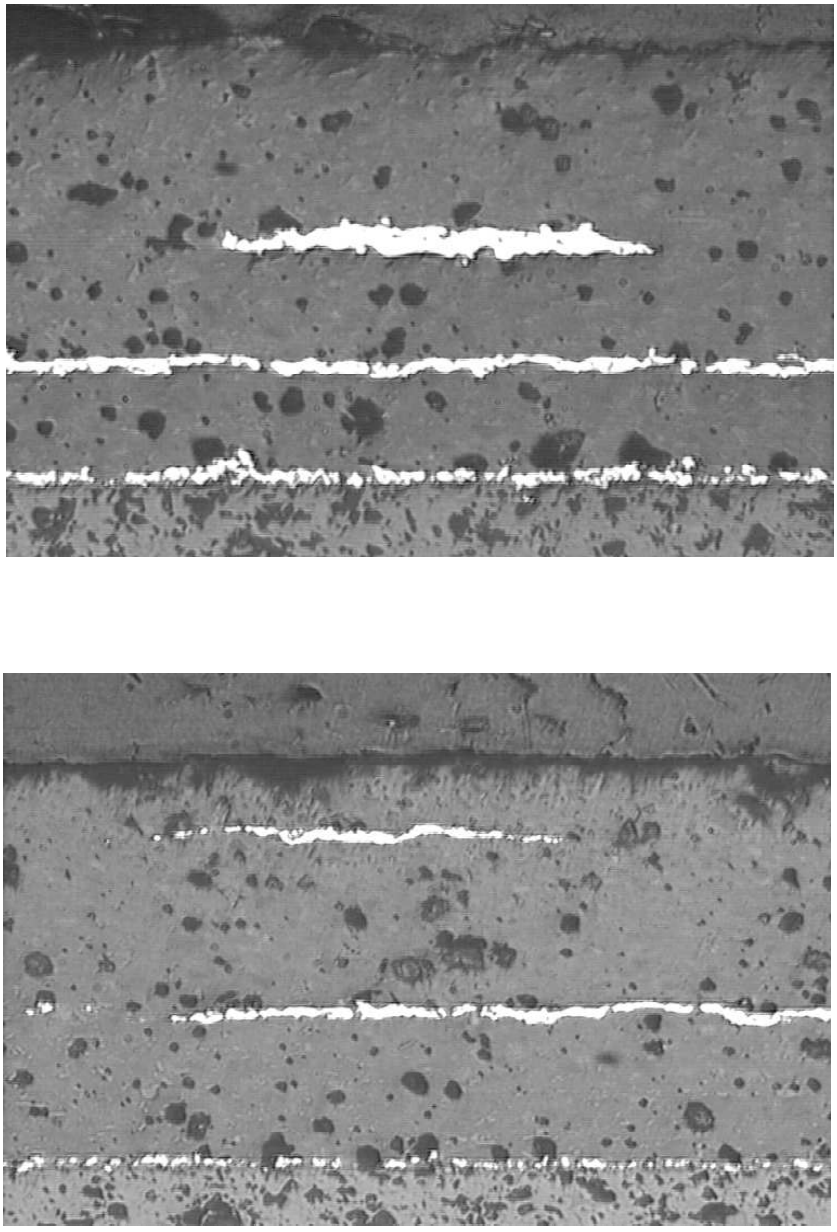


Figure 4.21: Two cuts through the layers of a thick film hybrid. In the upper plot a 100 μm wide line in 8 μm gold is shown and in the lower plot 150 μm wide line in 3 μm gold is shown. The other white layers are power and ground planes in 3 μm gold. Insulation layers are 35 μm.

- Electrical properties such as resistivity of conductors and permittivity of insulators are better.

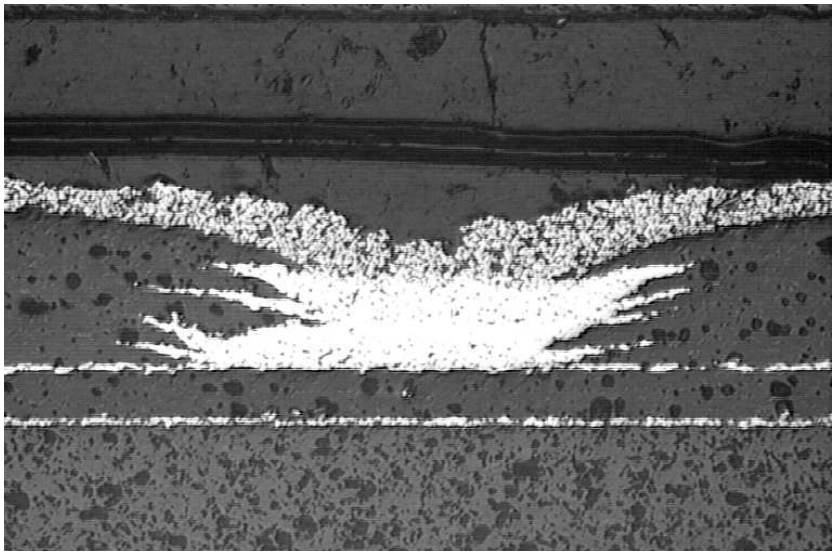


Figure 4.22: A cut through a SMD pad with a very huge via connection down to the ground plane. The lowest plane is the power plane sitting directly on the alumina substrate since this hybrid is printed without a bottom shield.

- The thermal conductivity of TPG is superior to BeO.
- The TPG substrate is conducting and can be the electric shield between the chips and the detector.
- The amount of material is much smaller in the TPG hybrid.

Except for the pitch adapter the design rules used are $100\,\mu$m track and spacing, the same as the minimum usable for a thick film layer in a routing layer ($8\,\mu$m). In the thin gold layers of a BeO hybrid the minimum track and spacing are $150\,\mu$m. The via hole in the Al/polyimide process can be $70-75\,\mu$m, with the annular conducting ring around of $40\,\mu$m, making the whole via structure $150\,\mu$m wide. In the thick film process the vias are printed as separate via-fills to fill the opened holes in an insulation layer. The size of the hole and the printed fill are both $200\,\mu$m in diameter. The thickness used is typically $5\,\mu$m for the Al and $15-20\,\mu$m for the polyimide, compared to $1.5-8\,\mu$m Au and $35\,\mu$m glass/oxide.

Some additional design rules also apply, not used for the BeO hybrid. The solid metal planes must be hatched. This to ensure adhesion of polyimide not only to the metal but also to the underlying polyimide layer. This prevents de-lamination. In addition can a via not extend through several layers, but it will have to be staggered, meaning that a via only goes through one polyimide layer before it must be routed by a short track to a new via bringing the signal through another polyimide layer. The polyimide is in addition not allowed to have big openings, which means that all bond pads and solder pads must be put on the top layer. At least two ways exist to make bonding feasible onto the aluminum.

One is to use 0.2 μm Ti, followed by a micron of Ni before a finish with 0.2 μm Au. The other solution is to use a micron of Ag as the bondable material.

The electrical properties of the Al/polyimide hybrid should be better than those of the Au/glass hybrid. The resistivity of Al is 5.3 m$\Omega/\Box$ calculated for a 5 μm thick conductor. Measurements based on 15 SCT128B and 8 ABCD hybrids show resistivities of 15 and 14 m$\Omega/\Box$, respectively, with typically less than 10% spread between hybrids. These measurements were done for the 3 μm thick power and ground planes, where it is important to have low resistivity. The low resistivity is needed to present the front-end amplifiers with a 'single point' ground and to assure identical supply voltages for all chips on the module.

A calculation based on pure gold gives that only 1.6 μm Au thickness should correspond to the measured 15 m$\Omega/\Box$. The microscope pictures, however verifies the gold thickness of 3 μm. This confirms that the gold more or less is locked in a matrix with the binder in a granulary way such that not all the gold contributes to the electrical conduction. It is important to note that the resistivity of Al is almost three times below that of gold, but with the gold more than a factor 10 thicker in radiation length, even though it is thinner.

The supply sagging over the module decides the lower limit on the amount of material that is necessary in the power/ground planes. A calculation based on the ABCD design, with the analogue and digital grounds connected together throughout the hybrid, reveals a drop of very close to 100 mV for both supplies of the last chip on the bottom hybrid as compared to the first on the top hybrid. This is divided into 120 mV on the analogue and 90 mV on the digital if the supplies are not grounded together. This was the motivation for proposing a reduced mass BeO hybrid with the power reduced to half the material, since this will give a 200 mV power difference on the two extreme chips of a hybrid. This is an acceptable drop as long as the first chip is powered 100 mV above nominal so that the last chip is 100 mV below.

The distribution of power to the bottom hybrid through the top hybrid is not a desirable choice. It is maybe the easiest or only solution mechanically, but far from optimal electrically. The best solution would have been to stretch the pigtail over the first hybrid so that the interconnect is between the two hybrids. The supply sagging would be reduced to one fourth. The wrap-around cable is an additional worry. A proposal of replacing the wrap-around with bondings from the hybrids to the baseboard and electrical feed-throughs in the baseboard has been put forward.

The insulation layers of polyimide is thinner than for the glass. The permittivity of the polyimide is however only 2.8 compared to $9 - 9.5$ for the glass/oxides, giving effectively smaller capacitive couplings since the insulation thicknesses are about $15 - 20$ μm and 35 μm for the polyimide and glass, respectively.

The TPG substrate is inserted into a frame of epoxy to prevent de-lamination. This frame is about 1 mm thick and the width of the frame is 1 mm. The thickness of the frame and the TPG is about 0.5 mm. When inserted into the frame, both sides are covered with about $3 - 4$ μm of epoxy, so that the TPG is fully enclosed. The first polyimide layer sits directly onto this thin epoxy with a very good heat contact. Since the thermal conduction of the TPG is around 1700 W/(m $\cdot$ K) compared to 280 W/(m $\cdot$ K) of BeO, the TPG hybrid will be better thermally, giving lower temperatures and gradients along the front-end chips.

TPG is conducting and can be used as the shield towards the detector, as opposed to the BeO hybrid where this shield must be printed as a separate layer in the process. This saves one layer of aluminum and one layer of polyimide in the production of the thin film hybrid.

The two TPG hybrids of a module will sit in a sheet of kapton, functioning both as the wraparound cable and the pigtail cable. The proposed connection between the kapton cable and the hybrids is through bondings, compared to the soldered kapton cables for the BeO hybrids.

Only the layout of the TPG ABCD3 hybrid is presented in figure 4.23. The TPG hybrid does not show the fan-in that actually is included in the layout of the two uppermost layers. Some features of the design are:

- Provision for drilling a hole through the Al/polyimide layers such that a drop of conducting glue can connect the TPG to the analogue ground as a shield between hybrid and detector.
- Metallized area under the chips in the second layer, connected to the chip pads with vias. This improves heat conduction down to the TPG.
- Addition of bond pads on the hybrid edges to facilitate the building of the kapton/epoxy-frame/TPG/Al/polyimide module.
- Removal of ground and power planes under the fan-in to reduce capacitive loading of the chip inputs.
- The thermistor is connected between the two TEMP lines on the hybrid. Earlier versions would connect the top hybrid thermistor between TEMP1 and ground and the bottom side thermistor between TEMP2 and ground. The new scheme provides an average temperature between the two hybrids measured fully differential, such that changes are easy to monitor. In addition is the thermistor moved towards the fourth chip where the anticipated highest temperature is found.

4.11.1 Radiation thickness of the TPG hybrid

The radiation length of the TPG based module will only differ in the value for the hybrid, since the additional components and thermal/mechanical parts are the same. The conducting material is aluminum and the insulation is polyimide resulting in a substantial decrease in the radiation length. The numbers are given in table 4.7. The total contribution of the hybrid is about 0.15%, which reduces the module total to around 1.1%. The reduction here is very important, and comes only from the printing itself, since the TPG substrate is more or less equal to the beryllia substrate.

The conducting/insulating layers are only contributing an amount of material a magnitude below that of the substrate, which means that no electrical sacrifices are necessary in the design. This allows the use of full planes for power and ground. The required adhesion between layers limits 'full' planes to planes hatched at about 92% coverage.

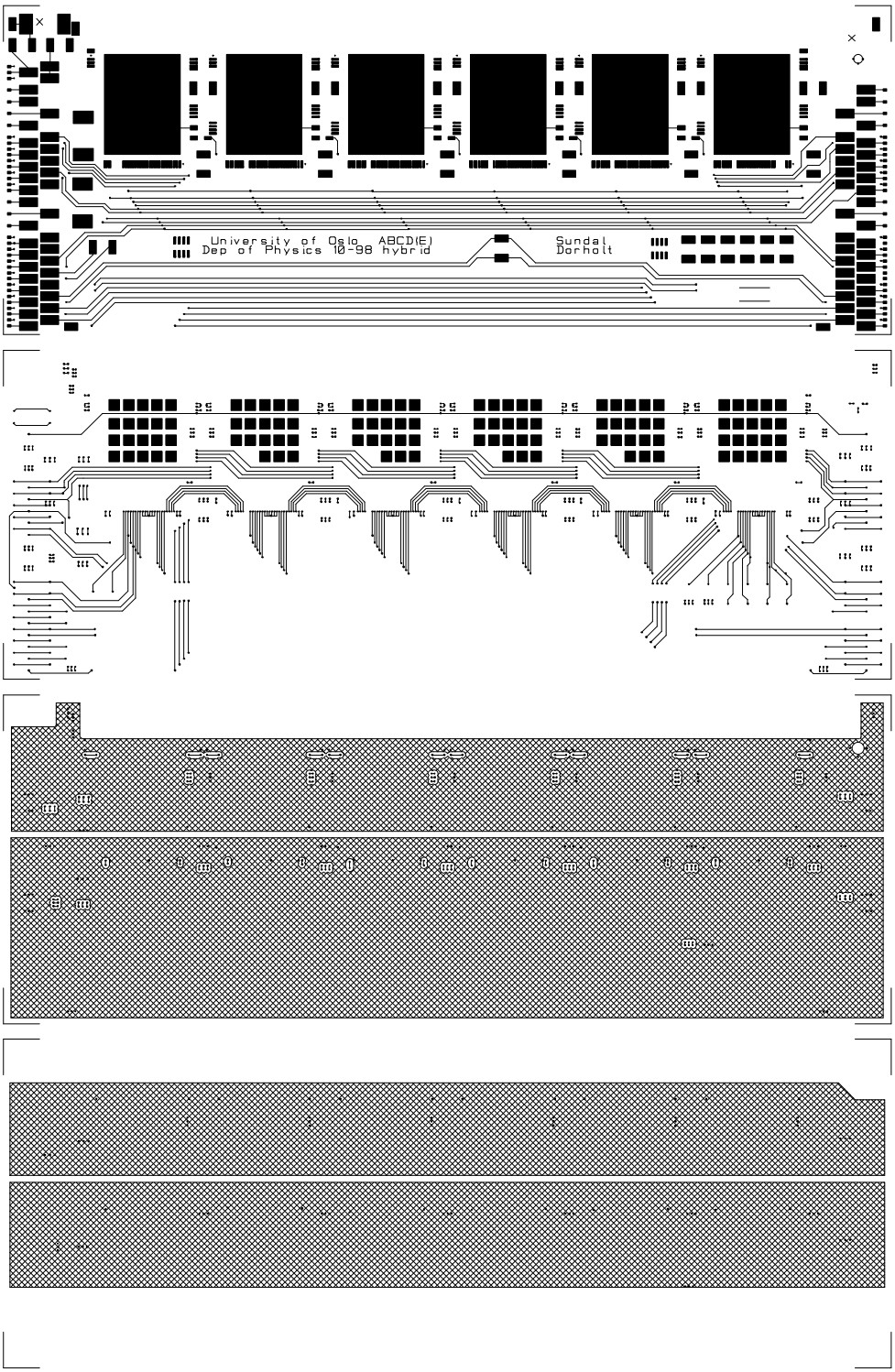


Figure 4.23: The ABCD3 design for the Al/polyimide thin film process. Processed onto an epoxy covered TPG substrate. From top: bond/solder layer, bottom route, ground plane and power plane.

Part	Material	X_0	t	w	l	n	% X_0
TPG+epoxy cover	TPG	190.0	0.5	28.0	74.6	2	0.1350
Substrate total							0.1350
Printing							
insulation layers	poly	287.0	0.015	27.64	74.24	8	0.01054
top layer route	Al	88.9	0.005	0.1	1630.0	2	0.00023
bond pads	Al	88.9	0.005	0.152	0.457	600	0.00003
connector pads	Al	88.9	0.005	0.762	1.524	138	0.00011
0603 pads	Al	88.9	0.005	0.610	1.118	92	0.00004
1206 pads	Al	88.9	0.005	1.067	1.676	12	0.00001
chip pads	A1	88.9	0.005	6.35	8.51	12	0.00045
bottom layer route	Al	88.9	0.005	0.1	1225.0	2	0.00017
bottom cooling pads	Al	88.9	0.005	0.965	0.965	224	0.00014
digital power plane	Al	88.9	0.005	9.0	73.7	1.84	0.00084
digital gnd plane	Al	88.9	0.005	15.5	73.6	1.84	0.00145
analog power plane	Al	88.9	0.005	8.04	73.7	1.84	0.00075
analog gnd plane	Al	88.9	0.005	8.22	73.6	1.84	0.00077
Printing total							0.0155
HYBRIDs total							0.151

Table 4.7: A calculation of the radiation length of an aluminum/polyimide hybrid on a TPG substrate. The result is averaged over a module area of 81.4 cm^2.

4.12 Summary

Readout hybrids based on thick and thin film processing have been made for the ATLAS SCT silicon barrel modules. For the baseline option of gold conductors on beryllia substrate a working single sided module based on the SCT128B chip has been made. Acceptable performance of this module was reported [38] at the 1997 IEEE Nuclear Science Symposium, Albuquerque, New Mexico.

Hybrids have also been designed for several versions of the ABCD readout chip. Some results are presented in [39]. Not all results have been encouraging, but this can be attributed to chip problems such as low phase margins caused by process parameters different from what were expected during the design phase. These problems will hopefull disappear in the latest version of the ABCD soon to be produced. The radiation length of the hybrids produced so far is however not acceptable for the final module. A stripped down module (by minimizing the hybrid material) is therefore described, with a radiation thickness of 1.22%, compared to the design specification of 1.2%.

Due to an interest in finding a module with the best possible heat conduction and the lowest possible radiation thickness, also a hybrid based on a thin film process using TPG as a substrate and aluminum/polyimide was produced. Results with a module based on this hybrid will eventually be published.

Let me draw some personal conclusions at the end. I believe the thick film hybrid will be the best solution for the ATLAS SCT based on the following facts:

- It is the industry standard and has been for many years. It has a verified high long term stability, important in this application where 10 years of operation is required. In addition are there a lot of experience with these solutions in the community.
- The specification with respect to the radiation length can more or less be met.
- It is the only natural choice in the forward section where double sided hybrids on a single substrate are needed. It is an advantage to use the same technology in the forward and barrel section, even though in the barrel section the copper/kapton solution does not need extra soldered kapton cables, since they are an integrated part of the design.
- Results with the SCT128B indicates that the electrical properties of a BeO hybrid are good enough. The problems found with the ABCD today I believe will vanish when the phase margin of the ABCD is improved and the hybrid further optimized.

The TPG solution is an interesting technology for the future. I feel however that it will be risky to use this solution, since there is little time to verify its long term stability. Most of these risks I feel to be related to its mechanical qualities, especially de-lamination problems of the epoxy/TPG substrate and also of its adhesion to the aluminum/polyimide hybrid.

Chapter 5

Conclusion and remarks

Front-end read-out hybrids based on the VA chips by IDE AS in Norway have been sucessfully designed and used in two major B-physics experiments. One for the RICH at the Cleo-III detector at Cornell, US. The other for the SVD at the Belle experiment at KEK, Japan. These are vastly different sub-detectors, which is reflected in the different technologies used for the read-out boards and also in the specific chips used. The succesfull implementation has been reported for the Cleo-III RICH at three major HEP conferences; the 29 th International Conference on HEP [31] in 1998 in Vancouver, Canada, the IEEE Nuclear Science Symposium [35] in 1997 in Albuquerque, US, and the 7 th Pisa meeting on Advanced Detectors [36] (NIM) in 1997 in Elba, Italy. The 1998 paper concludes that excellent results have been achieved with full RICH chambers. The operational Belle SVD has already taken data based on cosmic particles. Preliminary results were reported at the LCPAC99 [37] at KEK, Japan, in February 1999. It concludes that the estimated vertex resolution meets the design goal.

A low cost PC-based test and read-out system was designed for the VA/TA chip sets. This has been used to obtain statistics on VA chip parameters and read-out board parameters for the two experiments mentioned above. Verifying the read-out boards and giving insight to typical spread in parameters for the VA type of chips. The read-out system has shown the ability to measure chip parameters to a high accuracy and noise figures down to the lowest possible values given by noise theory on the input transistors of the chips. In addition has the VA-DAQ read-out system been sold in more than 20 copies worldwide to universities, research institutes and major companies for test and verification of new solid state sensors in silicon, CdTe and CdZnTe, making it a successful product for IDE AS.

These developments show how advanced ASICs containing low noise amplifiers over a period of less than 15 years have developed from the R&D level to almost a commercial off the shelf product. The amplifiers can be quite easily adapted to a variety of applications in experimental physics, medicine and industry.

Readout hybrids based on thick and thin film processing have been made for the ATLAS SCT silicon barrel modules. The baseline thick film hybrid design was used to build a working single sided module based on the SCT128B chip and tested at the H8 test-beam at CERN. Acceptable performance of this module were reported [38] (contributions to

this paper by the author) at the 1997 IEEE Nuclear Science Symposium in Albuquerque in New Mexico. Several hybrid iterations have followed for the ABCD chip versions. A stripped down module for the ABCD chip is proposed, with a radiation thickness of 1.22%, compared to the design specification of 1.2%. A hybrid based on a thin film process using TPG as a substrate and aluminum/polyimide has been produced, promising lower radiation thickness and better thermal performance. Results with a module based on this hybrid will eventually be published.

These implementations define today the most challenging requirements for combined analogue/digital high speed circuits in a radiation hard environment. Again one would expect these circuits and integration methods to be available on a more commercial basis in a time span of 5-10 years.

In the future we will see even more miniaturization and the need for extreme packaging technology. This is already seen in the pixel detectors at LHC where even higher channel counts and power dissipations force the need of unpackaged flip-chip assemblies over larger areas [52].

ASIC/hybrid systems are today a natural part of high energy particle physics, especially together with solid state detectors. The solutions found, driven by the extreme demands of particle physics when it comes to radiation hardness, mechanical stability, material minimization and thermal management, are often state-of-the-art and can be used outside high energy physics.

The most interesting use of the technology outside the HEP community is in nuclear medicine and industrial inspection. The experience of solid-state tracking detectors in barrel shapes can easily be transferred to medical applications. Research is put into replacing the SPECT and PET cameras of today with better and more compact designs offered by the technolygy progress in the HEP community. The major improvement is usually due to improved detection efficiency offered in designs like the Compton camera, where the lead collimator can be removed. The efficiency increase is a very important design goal since it implies a reduction in the radioactive dose injected in the patient. Furthermore one would expect the spatial resolution to improve.

Appendix A

VA-DAQ 1.20 details

This appendix will explain some parts of the VA-DAQ 1.20 system in greater detail. The first section will explain the function of each bit in the write register of the VA-DAQ IO-space. The following section will describe the connectors and jumper settings possible, and the last section will describe the low and mid level software routines.

A.1 Detailed read and write register description

WRITE REGISTER 0: Controls the readout sequence timing.

- Bit 0 - RESBCAL
  RESBCAL is connected to the counter that holds the 8 bit value for the calibration DAC. It is an asynchronous reset that will set the register value to 0 when the RESBCAL=0. This means that in normal operation this bit should be 1.

- Bit 1 - CKCAL
  By clocking CKCAL (first set it to 1 and then to 0) the value of the calibration DAC register will be increased by 1. If the previous value of the register was 255, a clocking will wrap it around to 0. In normal operation this bit should be 0. The register increases its value on the positive edge of CKCAL.

- Bit 2 - INCDEL
  Clocking INCDEL will increase or decrease, depending on the value of the UDDEL bit, the value of the digital pot that controls the coarse hold delay. The internal value of the pot can be clocked to 99 in one end and 0 in the other end. Additional clock pulses after the pot has reached one of the ends have no effect. When the UDDEL bit is high a clocking will increase the internal counter in the pot, and UDDEL low has the opposite effect. The physical hold delay increases when the pot counter decreases, and decreases when the pot counter increases.

- Bit 3 - INCDEL2
  Has the same effect as INCDEL, but controls the fine delay. The fine delay has steps

in the order of 25ns, whereas the coarse delay have time steps of 10 times as much. The same UDDEL bit controls the counter action of this pot, as for the coarse hold delay pot.

- Bit 4 - UDDEL
  Controls the direction of the hold delay when INCDEL or INCDEL2 are clocked. See the description for INCDEL and INCDEL2.

- Bit 5 - ZEROHLD
  An external or internal trigger will set the hold signal after the programmed delay. To set hold inactive (low) one needs to set ZEROHLD low. The signal is an asynchronous active low reset signal for the chip hold signal. This means ZEROHLD is usually 1 and is given a short 0 pulse to clear the VA-chip hold.

- Bit 6 - COMPL
  This bit set means that the value of the external calibration register is inverted (1's complement) by the DAC. If the calibration DAC is forced to end latching while COMPL is high, it will load the inverted value of what is found in the external register. The external register is controlled by RESBCAL and CKCAL, but also by Register 4. Since 'negative' hold delays are allowed for internal triggers, there are only one way to end the continuous latching of the DAC. The DAC will latch on the falling edge of ZEROHLD. To clear an internal trigger can be done as follows, to make sure that TA-triggering works properly. ZEROHLD and CAL is brought low, followed by setting ZEROHLD high again. An accepted TA trigger should always be accompanied by setting CAL. In this way no external triggers can be accepted while INHIBIT is active. If one wants the DAC to latch the inverted value of what is in the external calibration register, COMPL can be asserted before CAL and ZEROHLD go low, and de-asserted at the same time as ZEROHLD goes high. When the next internal trigger starts with CAL going high the DAC will give a calibration pulse that corresponds to a jump from the inverted calibration register value to the calibration register value. If for instance the calibration register is loaded with 14, the DAC will give a calibration signal from DAC-value 241 (255-14) to DAC-value 14, which is a large negative going calibration step-pulse.

- Bit 7 - CAL
  On a positive edge of CAL an internal trigger is initiated. To enable external triggers CAL needs to be kept high permanently. See also the discussion on COMPL. Should also be brought high when an external trigger is accepted.

WRITE REGISTER 1: Controls signal selection and power supplies

- Bit 0-3 - SADR0, SADR1, SADR2 and SADR3
  This is the ADC input AMUX address. Bit 3 is the most significant bit in the four bit address, that gives the signal source for the VA-DAQ ADC. Depending on this address the ADC can sample the signals listed in table 2.4.

- Bit 4 - POWEN
  This bit controls the +2V and -2V supplies for the VA-chips with a relay. With the bit set these two supplies are disabled. When disabled, all digital VA-chip signals are disabled, and for default system set up, all VA bias voltages and currents.

- Bit 5 - LOADB
  This bit controls the loading of a byte to the calibration DAC. This bit should be high in normal operation. If a specific value needs to be set in the calibration DAC, the following sgould be done: Set LOADB low, write the wanted data byte to register 4. Finish off with setting LOADB high again. The two other control signals for the calibration DAC, CKCAL and RESBCAL must be inactive during this sequence.

- Bit 6 - CALGEN
  Setting this bit high will trigger the calibration DAC. It is the logical or of CAL and CALGEN that is the real trigger for the calibration DAC. If the calibration DAC pulses or not depends on how it is setup. It must have been setup with different values in its external and internal register. It takes a negative going pulse on ZEROHLD combined with setting both CAL and CALGEN low to enable the calibration DAC for a new pulse.

- Bit 7 - LATCH
  Setting this bit to 0 will enable external TA triggers, 1 will disable them. Take care not to enable triggers except for the time where they are wanted. Default value is 1.

WRITE REGISTER 2: Controls VA logic signals

- Bit 0 - CONVERT
  There are three ways to force the ADC to do a conversion. An internal/external trigger will after a delay assert the hold, which again starts a conversion. As long as hold is asserted new conversions are easily started by using the automatic read in the driver. This is a routine which reads the ADC and starts the new conversion using the clock pulse for the VA. Both methods involves asserting VA signals (hold or ck). The third method uses the CONVERT bit. This bit is usually low. Setting it high (hold must be inactive, which means external or internal triggers must have been cleared) will force the ADC to convert. After the data is ready and read out, CONVERT must be set low again.

- Bit 1 - VADIG1, CK
  The VA clock signal (ck/ckb). The full VA clock signal is a logic OR of this bit and a clock pulse generated when the ADC is read out in an automatic mode. The following 6 signals are general purpose. They are driven as differential signals at VA logic levels and can easily drive a 100 ohm terminator between the two phases. A default use for them has been defined, this is the use they have with standard ADAPTER boards.

- Bit 2 - VADIG2, DRESET
  Default setting is to put DRESET on bit 2.

- Bit 3 - VADIG3, SHIFTIN
  The VA shift in signal. This is the read-out bit of the chip. A clocking of the chip when this bit is active, will insert a read-out bit into the chip. Consecutive clocks will enable a new channel for outputting its value on the VA chip output. One needs to ensure that shift in is active for both edges of the clock pulse in order to have a correct loading of the VA chip shift register.

- Bit 4 - VADIG4, TESTON
  The VA test on signal. When test on is active, the chip can be tested by using the calibration input.

- Bit 5 - VADIG5, CLKIN
  Default used for the TA CLKIN, which will clock in the disable channel mask and the polarity bit.

- Bit 6 - VADIG6, REGIN
  Default used for the TA REGIN, the shift register data to be clocked in by CLKIN.

- Bit 7 - VADIG7
  A general purpose digital signal at VA logic levels.

WRITE REGISTER 3: Controls bias generation and monitoring

- Bit 0-3 - MADR0, MADR1, MADR2 and MADR3 Address for the monitoring AMUXes. Bit 3 is the most significant bit in a 4-bit number. The number sets the channel selected from the two monitoring AMUXes. If the ADC input AMUX selects either Monitor A or B it can read the signals listed in table 2.5.

- Bit 4 - DACCSB (for bias generation DACs)
  Start loading of a bias to the bias DACs by pulling this signal low. Pull it high again at the end of the down-loading sequence.

- Bit 5 - Bit3.5
  Not used. Reserved for future extensions. Should be kept high as default.

- Bit 6 - DACDAT (for bias generation DACs)
  This is the data for the serial down-loading of the DACs.

- Bit 7 - DACCLK (for bias generation DACs)
  This is the serial clock for the DAC down-loading.

REGISTER 4: Calibration DAC value

- Bit 0-7 - DAC-value
  Writing to this register sets the value of the external calibration DAC register. Manipulations with CKCAL and RESBCAL can change the content of this register. Bit 7 is the most significant bit. The value written to this register is only accepted if the LOADB bit is low.

REGISTER 5: Reserved for future extensions of VA-DAQ

- Bit 0-7 - Not used
  No physical register is connected to the write register 5 strobe on the VA-DAQ 1.20 card.

REGISTER 6 and 7: Available for user made plug-in extensions to CON-D
On CON-D the 8-bit data bus and write strobes for these two registers are brought out, in addition to 4 read strobes, +5V digital and digital ground. The use of CON-D is found under the connector specification sections.

READ REGISTER 0 and 1: Least and most significant ADC bytes
The ADC value is a 14 bit number in two's complement. To make it a signed 16 bit number, just copy the uppermost bit (the fourteenth) to the last two upper bits.

REGISTER 2: Readable TTL-byte newline A byte at TTL-levels can be read from connector CON-A

REGISTER 3: Reserved for future extension to VA-DAQ
No hardware is connected to the read strobe associated with this register. Reading this register should give a value of 255 since the data bus has a weak pull up to +5V digital.

REGISTER 4-7: Available for user made plug-in extensions to CON-D
See the discussion in the connector CON-D specification.

A.2 VA-DAQ jumpers and connectors (cont'd)

This section describes jumpers and connectors of the VA-DAQ system to a detail not found possible to include in chapter 2.

A.2.1 VA-DAQ connectors continued

In addition to the three IDC connectors CON-A, B and C, there are also three LEMO connectors on the front edge of the VA-DAQ system. From the upper left (looking from above and the front edge upwards) these three connectors are named CN1, CN11 and CN42.

CN1: NIM-trigger
This LEMO terminates the incoming signal in 50 Ω. The pot meter P1 right below should be adjusted to a voltage level in between the two logic levels arriving on the LEMO. A positive edge is accepted as a trigger, as long as the NIM-trigger is the selected trigger. This is described in closer detail under the jumper settings. Note that this LEMO is placed

on the VA- DAQ board and not on the ADAPTER board. Another LEMO needs to be placed in the front panel to have access to this signal, or a LEMO cable can be inserted through a hole in the front panel. The same apply to the two other LEMO plugs, CN11 and CN42 mentioned below.

CN11: INHIBIT

This LEMO-output at TTL-levels is at logic high level from the time where a trigger is accepted until the system is finished processing the data from this trigger. Can be used as an inhibit signal for other electronics involved in the read out. The yellow LED is on while INHIBIT is active.

CN42: CAL

This is the calibration step pulse used to induce an input charge in a VA chip, when the chip is run in test mode. This signal is also available on CON-C. The signal should end in 50 ohms, and the signal applied to a typically capacitor of 1.8 pF connected to the CAL pad of a VA chip. On the lower edge of the card three connectors are found. CN64 is for the parallel port cable connection, CON-D is for digital extension cards and CN77 is for the VA-DAQ supplies.

A.2.2 VA-DAQ jumper settings

In the system several 2-pin and 3-pin jumper settings exist. On a 2-pin jumper a jumper does not need to be present, whereas on a 3-pin jumper there needs to be a jumper in one of the two positions. Except for the attenuation of calibration pulse, which is available in the backplate of the VA-DAQ system, no other jumpers are available for the common user.

Jumpers for attenuation of the calibration output

There are five two pin jumpers for attenuation of the calibration step in the right side of the VA-DAQ back plate. These are stacked next to each other. A jumper should be put on one of these five jumpers. The leftmost position gives no attenuation, and each step to the right gives 6 dB attenuation. In the rightmost position the attenuation will be 24 dB.

To the right of these jumpers, two 3-pin jumper settings are found. Each control a 20 dB attenuation. With the jumper in the left position there is no attenuation and in the right position there is 20 dB attenuation.

Jumper for additional attenuation of the calibration output

The jumper, CN43, is located in the upper right corner, close to the LEMO for the CAL signal, CN42. This will terminate the CAL signal in 51 ohms before it leaves the VA-DAQ card. Can be used with VA-hybrids without 50 ohms termination mounted, and will then ensure correct operation of the -20dB attenuator. This jumper is not mounted as default in a VA-DAQ system.

Jumpers for external trigger selection

There are four 2-pin jumpers close to each other on the left edge. A jumper needs to be put on one and only one of these four jumpers. Depending on the position of the jumper, a specific external trigger is chosen:

- Jumper on CN44: Selects the NIM-trigger on LEMO CN1.
- Jumper on CN45: Selects the single-ended TTL-trigger on CON-A.
- Jumper on CN46: Selects the diff. TTL-trigger (or RS422 trigger) on CON-A.
- Jumper on CN47: Selects the TA-trigger on CON-A. This is the default setting.

Jumpers for setting polarity and levels of bias signals

The 3-pin header CN58 selects the maximum voltage levels for positive bias voltages (above ground). If the jumper is in the leftmost position the VA +2 V is selected, in the rightmost position the +2.5 V reference is selected. Similar for CN59 but for the −2 V and the −2.5 V. The default is to select the ±2 V supplies as maximum voltage levels.

The 3-pin headers CN56, CN60, CN57 and CN61 are used to select polarity of the biases BIAS0-1, BIAS2-3, BIAS4-5 and BIAS6-7. With the jumper in the leftmost position, positive voltage is selected. As default, the jumper selections are left, right, right and right for CN56, CN60, CN57 and CN61.

Jumpers for controlling the ±2 V supplies

The 3-pin headers CN54 and CN55 controls the +2 V and −2 V supplies, respectively. If the jumper on CN54 is in its leftmost position, the value of the +2 V supply is controlled by the pot-meter just below the header. The same apply to CN55, but for the −2 V supply. If the jumpers are in the rightmost position, the +2 V supply is controlled by BIAS8 and the −2 V supply by BIAS10.

Two and three-pin headers which are not intended for jumpers

Under the ADC, CN49 is placed, on pin1 analogue ground is found and the digital ground on pin2. From the bottom side of the card a wire should be soldered in to connect analogue and digital supplies. With default supplies, where both analogue +5 V, analogue −5 V and digital +5 V supplies are floating with respect to each other, the VA-DAQ needs the two ground planes to be connected in one point only. Somewhere between the ADCs analogue and digital ground pins is the optimal place for this connection. In a system with all three supplies grounded together at the supply-unit, this connection should not be shorted. Such a solution is not considered optimal.

The CN12 footprint on the upper edge, between the LEMO CN11 and CON-B, can be connected to a yellow LED. The left leg is the cathode. This LED will be on when the

INHIBIT signal is active. The best is to drag a twisted pair to a LED housed in a socket in the front plate. The CN23 and CN24 footprints between CON-B and CON-C can be used for two green LEDS. For CN23 the cathode is the left leg and for CN24 the cathode is the right leg. The CN23 LED will be on when the -2 V supply is enabled, and the CN24 LED when the $+2$ V supply is enabled. The LEDS could be fitted in the front plate.

A.3 Low and mid-level software description

The low- and mid-level software of the VA-DAQ system is listed in the following subsections. The mid-level and the helping routines in the Calculat.llb (calculational help) and Globconv (Global variables and conversion VI's) is the starting point for developing own VI's for measuring other interesting parameters besides those already existing among the menu items.

A.3.1 Low level library; Lowlevel.llb

All low level VI's, defined to be VI's that use the hardware driver, is collected in the LabView library Lowlevel.llb. The hardware driver itself is also found in the library. The low level VI's are grouped into functional units. In addition a few global variables for VI's in the Lowlevel.llb is found in Lowglobs.VI.

VI's for analogue signal selection

Setmux - Selects the signal to read from the 46 analogue channels.

VI's for setting the hold delay

Chgdel - Sets/increments coarse/fine delay.

VI's for setting the calibration signal size

Chgcal - Sets/Increments the value of the external calibration DAC. Will not affect the value of the internal DAC unless it is transparent at the moment.
Chgpulse - Sets/Increases calibration register value, and makes ready for a cal pulse with Settrg. A quiet mode exist where external/internal value is the same.

VI's for controlling VA logic signals

Clock - Gives a single clock pulse to the VA chip.
Reset - Resets the digital part of the VA chip.
Shiftin - Resets and clocks a read-out bit into the VA read-out register.
Gotochan - Shifts in a read-out bit and clocks it to the wanted channel.

Settest - Puts the VA chip in or out of test mode.

VI's for setting the biasing DACs

Setbias - Sets a value of 0-255 in one/all of the twelve biasing DACs.

VI's for trigger conditioning

Settrg - Generates an internal trigger. Also needed to confirm external triggers.
Clrtrg - Clears an external/internal trigger. Can also prepare calibration DAC for new pulse if wanted.
Pulse - Will pulse the calibration DAC. Will not have any effect on the hold or the ADC sampling as Settrg will. **Enexttrg** - Will eanble/disable the possibility of an external TA trigger to VA-DAQ

VI for initializing, cleanup and bus check of the VA-DAQ system

Initdaq - Will put the VA-DAQ system in a well defined startup state.
Clearold - Will reset any set trigger and dump any rubbish ADC data.
Chkbus2 - Will check that all possible bytes can be writtm and re-read from the bus.

VI's for read-out of all channels (pedestal read-out)

Pedinit - Initializes for read-out of all channels.
Pedcorex - Reads a number of channels from a VA-chip. Returns pedestal values in mV. The Pedcorex is implemented by calling other low level VI's. A mid level routine for reading pedestals exist, where all software is inside the driver, making it faster.

VI for enabling/disabling the VA chip supplies, digital signals and biases

Setpow - Turn on or off the +2V/-2V supplies.

VI for down-loading and read back of shift register (TA mask)

Setmask - Downloads and checks a TA mask, using CLKIN, REGIN and REGOUT.

VI's for sampling of the VA output waveform

Waveinit - Initializes for grabbing points on waveforms.
Nwawipul - Reads a point on the waveform at current hold delay and cal-size. Will average over N samples, and also end with the possibility of increasing the cal-DAC value.

Nwaitext - Much like Nwavipul. But will issue a calibrate pulse and let a potential external TA response trigger the ADC readout. Will return how many out of the N runs that gave an external trigger.
Mwaitexi - As Nwaitext but the code inside the driver.

VI's for time delays

Wait1ms - Wait some ms, by performing dummy status reads from VA-DAQ.
Timecore - Is used to find wait time from Settrg to data ready.

VI's for reading analogue values

Nmon - Returns average of several samples with the ADC.

A.3.2 VI's for calculational purpose; Calculat.llb

This is a collection of routines performing various calculations.

VI's for statistics and other calculations

These routines perform various general algorithms.

Addeadar - Merges a list of integer values.
Andarray - Ands together all elements of a boolean array.
Avgstd - Calculates average and standard deviation of an array.
Convjump - Performs Outarray(i)=Inarray(N-i)-Inarray(i).
Interp - Fits a polynomial to a data set and locates the peak.
Mean - Calculates the mean of a data set.
Nantmean - Returns the mean of a data set if some tests are accepted.
O10in255 - Returns a value 10 off the input, but in the range 0-255.
Offrange - Returns the indices of the input elements that didn't pass a cut.
Okarray - Returns an array of elements that do not have the indices mentioned.
Sqsum - Calculates a square sum. Reduces it by square root of the samples.
Trunc255 - Truncates the input to an integer value in 0-255.
Trunc99 - Truncates the input to an integer value in 0-99.
Widecm - Expands an array into a bigger one, with multiple similar elements.

Calculations needed for delays and bias adjustments

The VI's below are not general in the sense that they use global variables specific to VA-DAQ.

Calcdel - Calculates the hardware settings for the wanted hold delay in μs.

Coarseadj - Coarse bias DAC setting to get wanted voltage.
Fineadj - Fine adjust of bias DAC to get wanted voltage.
Truncbia - Truncates a wanted bias voltage into the possible range.

A.3.3 VI's for measuring and setting real values; Midlevel.llb

The VI's in Midlevel.llb rely heavily upon global variables, which values have been calibrated once an for all or at every start up of VA-DAQ. The global variables themselves and the VI's to calibrate them are found in the Globconv.llb

VI's in Midlevel.llb

Calib22 - Measures the two biggest calibration steps after the attenuation.
Calibcl2 - Measures all 256 calibration steps before the attenuation.
Curslope - Measures the current-slope (mV/μA) of a bias.
Getgain2 - Measures the gain of all channels.
Getpeaks - Measures the signal values at two defined peak calibration steps.
Getped2 - Measures the pedestal values of all channels.
Getsout - Checks if the shift out circuitry of the VA chip is working.
Measbias - Measures the voltage and current in the biases.
Measpow - Measures the voltage and current in the ± 2 V supplies.
Npedcs - The core in the pedestal calculations, like in Getped2.
Readbiv - Returns the voltage and current for one of the biases.
Readmon - Reads the value of the 6 general monitoring channels.
Seta8biv - Sets the 8 first biases as close as possible to the wanted voltages.
Setbapv - Tries to set biases and supply to the wanted voltage/current.
Setbiv - Sets a bias voltage as close as possible to the wanted voltage.
Setdel - Sets the hold delay as close as possible to the wanted value.
Thrcore - Measures the threshold input charge for the TA.

A.3.4 VI's for global variables, calibration and conversion; Globconv.llb

The VI's in this library are grouped into three different categories. One category is the global variables, the next contains the routines for calibrating the VA-DAQ system, whereas the last category contains the VI's for converting measured quantities like ADC counts into real quantities like mV or uA.

VI's containing global variables

Globadc - Global variables for the ADC.
Globbia - Global variables for biasing.
Globcal - Global variables for the calibration step.
Globfix - Global variables measured once for the entire system.
Globsof - Global variables for software, contains file paths.
Globaut - Global variables common to automatic testing.
Globautb - Global variables for biasing part of automatic testing.
Globautg - Global variables for the general part of data sheet for automatic testing.
Globautm - Global variables for the misc. part of the automatic testing.
Globautn - Global variables for the noise part of the automatic testing.
Globautp - Global variables for the pedestal part of the automatic teting.
Globauts - Global variables for the gain part of the automatic testing.
Globautt - Global variables for the peak/range part of the automatic testing.

VI's for calibration

Clbadc - Calibrates the ADC.
Clbbias2 - Calibrates the bias voltages.
Clbcal2 - Calibrates the step pulse (the calibration step).
Clbpow - Calibrates the supply voltages.
Clbtim - Calibrates the hold timing.
Biasctr2 - VI used by Clbbias2.
Powctrl - VI used by Clbbias2.
Tunetim2 - Calibrates the Wait1ms VI.

VI's for conversion between different units

Adcmv - Converts ADC counts to mV.
Dadcmv - Converts an ADC count difference to mV.
Madcmv - Converts an array of ADC counts to mV.
Dmadcmv - Converts an array of ADC count differences to mV.
Mvib - Converts a sensed mV difference into current in uA.
Mmvib - Converts an array of mV differences into current in μA.
Mvis - Converts a sensed mV difference into a supply current in mA.

A.4 Automatic testing

VI's for defining setups and launching automatic tests are found in the two libraries; Adeffile.llb and Automeas.llb. The Adeffile.llb contains everything necessary to read and write definition files for setup of VA- DAQ for a certain chip/board. Automeas.llb contains all VI's for setting up the automatic testing and other parameters, the VI's that are performing the actual measurements and the VI's for writing the result to file.

A.4.1 VI's in Automeas.llb

The main VI for setting up a system definition and automatic data sheet generation is the **Automeas.vi**.

Setup of parameters

The setup of parameters, both setting up VA-DAQ, defining tests and cuts and how to write result to files are done by the following VI's. Each item will pop up its own front panel to set up the parameters.

Geneinfo - Define the general parameters for the tested board.
Biasinfo - Set up the biasing part of the definition.
Pedinfo - Set up the pedestal part.
Noiinfo - Set up the noise part.
Gaininfo - Set up the gain part.
Peakinfo - Set up the signal peak part.
Miscinfo - Set up general tests on chip basis. (Like functionality of shiftout).
Biasipar - Helping routine for Biasinfo.
Gainipar - Helping routine for Gaininfo.
Peakipar - Helping routine for Peakinfo.

Doing the automatic test

Most measurements called have their VI's in Midlevel.llb. The measurements are stored in global variables, one global VI for each of the -info (like Biasinfo) VI's in the previous section.

Doauto - The VI launching the wanted measurements. Front panel to show progress.
Biastest - Checks if biasing/supply within specifications. Will return an error string.
Biaschk - The core of the bias/supply checking.

Writing the results of automatic testing to file

Wrtauto - The main VI, a front panel will show the test result.
Genewrt - Will write the general part of the data sheet.
Biaswrt - Will write the biasing part.
Pedwrt - Will write the pedestal part.
Pedwrtfe - Helping routine for pedwrt. (For each chip).
Pedwrtco - Helping routine for pedwrt. (Common for all chips)
Noiwrt - Will write the noise part.
Noiwrtfe - Helping routine for noiwrt. (For each chip)
Noiwrtco - Helping routine for the noiwrt. (Common for all chips)
Gainwrt - Will write the gain part.
Gaiwrtfe - Helping routine for gainwrt. (For each chip)
Gaiwrtco - Helping routine for gainwrt. (Common for all chips)
Gaiwrthe - Helping routine for gainwrt. (Header part)
Gaindev - Helping routine for gainwrt. (Gain deviation).
Sigdev - Helping routine for gainwrt. (Signal deviation).
Peakwrt - Will write the signal peak part.
Peawrtco - Helping routine for peakwrt. (Common for all chips).
Miscwrt - Will write the miscellaneous tests part.
Wrtdead - Helping routine common for these routines.
Wrtallp - Helping routine common to these routines.

A.4.2 VI's in Adeffile.llb

The VI's for writing the definition file

Autwfile - Main VI for writing the definition file, calls the ones below.
Autwhead - Writes the header of the definition file.
Autwgene - Write the general info for data-sheet generation.
Autwbias - Write the biasing part of the data-sheet generation.
Autwped - Write the pedestal part of the data-sheet generation.
Autwnoi - Write the noise part of the data-sheet generation.
Autwgain - Write the gain part of the data-sheet generation.
Autwpeak - Write the peak part of the data-sheet generation.
Autwmisc - Write the miscellaneous part of the data-sheet generation.

The VI's for reading the definition file

Autrfile - Main VI for reading the definition file, calls the ones below.
Autrhead - Reads the header of the definition file.
Autrgene - Read the general info for data-sheet generation.

Autrbias - Read the biasing part of the data-sheet generation.
Autrped - Read the pedestal part of the data-sheet generation.
Autrnoi - Read the noise part of the data-sheet generation.
Autrgain - Read the gain part of the data-sheet generation.
Autrpeak - Read the peak part of the data-sheet generation.
Autrmisc - Read the miscellaneous part of the data-sheet generation.

Appendix B

Noise calculations for a readout system

Noise in read-out front-end electronics can be characterized in terms of common-mode noise and channel noise. For the channel noise one often use the two terms channel noise before and after common mode subtraction. The following calculation will show the relationship between these quantities.

B.1 Definitions

Each physical event, called e, of a total of N_e events, is characterized by N_i numbers, which are the N_i data samples for the event. The samples for the event are read-out in parallel or serial, but usually confined to a 'small' amount of time. The i'th sample in the e'th event is denoted d_i^e.

The common mode for an event is defined as:

$$d^e = \frac{1}{N_i} \sum_{i=1}^{N_i} d_i^e \tag{B.1}$$

The variation in common mode is usually induced on the system by external factors such as capacitive or inductive couplings to other electronics, and are not a part of the inherit noise contributions, which are unavoidable, in the readout system.

The average of common mode for all events is given by:

$$d = \frac{1}{N_e} \sum_{e=1}^{N_e} d^e = \frac{1}{N_e N_i} \sum_{e=1}^{N_e} \sum_{i=1}^{N_i} d_i^e \tag{B.2}$$

The average of the i'th channel over all events (or possibly defined only for the events in this channel not containing a hit) is called the channels pedestal value, and is given by:

$$d_i = \frac{1}{N_e} \sum_{e=1}^{N_e} d_i^e \tag{B.3}$$

The average of pedestals for all channels is also given by d, seen by noting that the expression yields the same double sum as in B.2.

The common mode noise is defined as the standard deviation of d^e over all the events. This is given by

$$\sigma^2(d) = \frac{1}{N_e}\sum_{e=1}^{N_e}(d^e - d)^2 \tag{B.4}$$

The channel noise for channel i (calculated on raw data) is given as the standard deviation of the i'th channel over all the events.

$$\sigma^2(d_i) = \frac{1}{N_e}\sum_{e=1}^{N_e}(d_i^e - d_i)^2 \tag{B.5}$$

Common mode subtracted data differs from raw data in the sense that all raw data for this specific event has the common mode for this event subtracted. If primes denotes common mode subtracted data one then has:

$$d'^e_i = d_i^e - d^e \tag{B.6}$$

The channel noise for common mode subtracted data is of course the same as in B.5 but with primed quantities replacing the unprimed

$$\sigma^2(d'_i) = \frac{1}{N_e}\sum_{e=1}^{N_e}(d'^e_i - d'_i)^2 \tag{B.7}$$

B.2 Relationship between noise contributions

In expression B.7 the right hand side can be expressed in terms of unprimed quantities by using B.6 and the fact that the average of a common mode subtracted channel is given by:

$$d'_i = \frac{1}{N_e}\sum_{e=1}^{N_e} d'^e_i = \frac{1}{N_e}\sum_{e=1}^{N_e}(d_i^e - d^e) = d_i - d \tag{B.8}$$

Writing B.7 using this yields

$$\sigma^2(d'_i) = \frac{1}{N_e}\sum_{e=1}^{N_e}((d_i^e - d_i) - (d^e - d))^2 \tag{B.9}$$

Performing the squaring yields then

$$\sigma^2(d'_i) = \frac{1}{N_e}(\sum_{e=1}^{N_e}(d_i^e - d_i)^2 - 2\sum_{e=1}^{N_e}(d_i^e - d_i)(d^e - d) + \sum_{e=1}^{N_e}(d^e - d)^2) \tag{B.10}$$

Here the first and third term is easily recognized as $\sigma^2(d_i)$ and $\sigma^2(d)$, respectively. The total relationship on a channel basis is then.

$$\sigma^2(d'_i) = \sigma^2(d_i) + \sigma^2(d) - \frac{2}{N_e}\sum_{e=1}^{N_e}(d_i^e - d_i)(d^e - d) \tag{B.11}$$

This equation is neither interesting nor helpful before it is summed over all i channels.

$$\sum_{i=1}^{N_i} \sigma^2(d'_i) = \sum_{i=1}^{N_i} \sigma^2(d_i) + N_i\sigma^2(d) - \frac{2}{N_e} \sum_{e=1}^{N_e} (\sum_{i=1}^{N_i} (d_i^e - d_i))(d^e - d) \tag{B.12}$$

Here the inner sum in i in the last line is recognized as $N_e(d^e - d)$, which results in the fact that this term ends up being $-2N_i\sigma^2(d)$, which yield the result

$$\sum_{i=1}^{N_i} \sigma^2(d'_i) = \sum_{i=1}^{N_i} \sigma^2(d_i) - N_i\sigma^2(d) \tag{B.13}$$

If now a quantity called the average of the square of the noise over all channels are introduced as being

$$\overline{\sigma^2(d_i)} = \frac{1}{N_i} \sum_{i=1}^{N_i} \sigma^2(d_i) \tag{B.14}$$

one finally obtains the compact result

$$\overline{\sigma^2(d_i)} = \overline{\sigma^2(d'_i)} + \sigma^2(d). \tag{B.15}$$

This states that the average of the square of the channel noise for raw data over all channels is equal to the same expression over common mode subtracted data plus the square of the common mode noise.

Index

Bibliography

[1] National Council on Radiation Protection and Measurements. *A Handbook of Radioactivity measurements procedures, 2.edition. NCRP report no. 58.*
Library of Congress Cataloging in Publication Data, 1985.

[2] W.R.Leo. *Techniques for Nuclear and Particle Physics Experiments, 2.edition.*
Springer Verlag, 1994.

[3] C. Grupen. *Particle Detectors.*
Cambridge University Press, 1996.

[4] K. Kleinknecht. *Detectors for particle radiation.*
Cambridge University Press, 1986.

[5] Particle Data Group, M.Aguilar-Benitez et al. *Particle Physics Booklet.*
American Institute of Physics, 1994.

[6] R.Klanner. *Drift and Detection of Charges in Silicon Detectors.*
Lecture at the ICFA School on Instrumentatin in Elementary Particle Physics, Trieste, June 1987.

[7] Bjørn Magne Sundal. *Development of a silicon detector hybrid for the ATLAS experiment at LHC.*
Thesis submitted to the degree cand. scient, University of Oslo, 1995.

[8] E.Nygård. *ASICs and electronic systems for readout of radiation-sensitive semiconductor detectors.*
Dr.scient. thesis, ISBN 82-7368-144-0, Jan. 1997.

[9] E.Nygård et al. *CMOS low noise amplifieer for microstrip readout.*
NIM publication A301 (1991) 506-516.

[10] V.Radeka. *Low-Noise Techniques in Detectors.*
Annual Reviews Nucl.Par.Sci. 1988. 38: 217-277.

[11] J.Kemmer.
Nuclear Instruments and Methods 226 (1984) 89.

[12] A.Peisert. *Silicon microstrip detectors.*
Article written by the author Jan. 1992, INFN, Italy.

[13] C.J.S.Damerell. *Vertex Detectors: The State of the Art and Future Prospects.*
Council for the Central Laboratory of the Reasearch Councils, Preprint RAL-P-95-008. Lectures at the 23. Annual Summer Institute on Particle Physics, SLAC, Stanford, 1995.

[14] P.Holl et al.
IEEE Transactions on Nuclear Science, NS-36 (1988) 251.

[15] P.Allport et al.
Nuclear Instruments and Methods, A342 (1994) 22.

[16] H.Dijkstra et al.
IEEE Transactions on Nuclear Science Vol. 36 (1989) 591.

[17] N.Bachetta et al.
Nuclear Instruments and Methods, A342 (1994) 39.

[18] T.I.Westgaard et al.
Paper contributed to the 7th European Symposium on Semiconductor Detectors (1995).

[19] J.Kemmer, G.Lutz.
Nuclear Instruments and Methods A273 (1988) 588.

[20] G.Bagliesi et al. *A Double Sided Readout Silicon Strip Detector. A New Device for Vertex Detection in High Energy Physics.*
Preprint INFN PI/AE 86/10.

[21] Integrated Detector & Electronics, situated at Høvik, Norway. *Data sheets for readout chips.*
Contact IDE for data sheets.

[22] V.A.J. van Lint. *The Physics of radiation damage in Particle detectors.*
NIM A253 (1987) 453.

[23] H.Spieler, LBL, Berkeley, California, USA. *Introduction to Radiation-Resistant Semiconductor Devices and Circuits.*
Tutorial written with support from the US department of Enrgy, Office of High Energy and Nuclear Physics.

[24] R.K.Bock, A.Vasilescu. *The Particle Detector BriefBook.*
Springer Verlag (1998).

[25] L.Andricek, G.Lutz et al. *Single sided p-on-n and double sided silicon strip detectors exposed to fluences up to* $2 \cdot 10^{14}/\mathrm{cm}^2$ *24GeV protons.*
Paper presented at the VII Pisa Meeting on Advanced Detectors, La Biodola, Isola d'Elba, May 1997.

[26] CERN Courier. *Twenty-five years of neutral currents.*
CERN Courier, volume 38, no 8, 1988.

[27] G.Mæhlum. *A Measurement of Lifetimes of b-hadrons Using a Silicon Microstrip Detector at LEP.*
Thesis for the degree Dr.scient, University of Oslo, 1993.

[28] The Belle Collaboration. *Technical Design Report.*
KEK-Report 95-1, April 1995.

[29] K.Berkelman. *Upgrading CESR*
Note distributed at Cornell.

[30] M.Artuso. *R&D towards the CLEO-III detector.*
Presentation given at XXIX International Conference on HEP, Vancouver, Canada 1998.

[31] M.Artuso. *Progress towards CLEO-III: The Silicon Tracker and the LiF-TEA Ring Imaging Cerenkov Detector.*
Paper presented at XXIX International Conference on HEP, Vancouver, Canada 1998.

[32] M.S.Yokoyama, H.Tajima. *Measurements of radiation effect on VA1 chip.* Note by the authors, University of Tokyo, Dec. 1997.

[33] Belle SVD group. *Technical Design Report of Belle SVD.*
Belle SVD group, March 1998.

[34] C.Bopp, D.Marlow, both Princeton. *Heat flow measurements for G10-based Hybrids for the BELLE SVD.*
KEK Belle Note 213.

[35] M.Artuso et al. *Status of Construction and First Tests of the CLEO-III RICH.*
IEEE Trans.Nucl.Sci. 45:643-647, 1998.

[36] M.Artuso et al. *The CLEO-III Ring Imaging Cherenkov Detector.*
Nucl.Instrum.Meth. A409-375-378,1998.

[37] H.Tajima, Tokyo University. *Vertexing Software Development.*
Presentation at LCPAC99 at KEK, Japan.

[38] W.Dabrowski, B.Sundal et al. *Performance of the Binary Readout of Silicon Strip Detectors Using the Radiation Hard SCT128B Chip.*
Paper at the 1997 IEEE Nuclear Science Symposiumn, Albuquerque, New Mexico.

[39] D.Ferrere, D.Macina et al. *Test on ABCD chips.*
Atlas Internal Note ATL-INDET-98-217, Nov.1998.

[40] J.E.Moyal. *Theory of ionization fluctuations.*
Phil.Mag. 46 (1955) 263.

[41] CERN. *The LHC Conceptual Design Report - The Yellow Book.*
CERN/AC/95-05(LHC).

[42] S.Stapnes. *Physics at LHC.*
Talk held at the Institute of Experimental Physics, SAS, Košice, Slovakia, 1998.

[43] ATLAS collaboration. *ATLAS Technical Proposal.*
Printed at CERN December 1994 ISBN 92-9083-067-0.

[44] ATLAS collaboration. *ATLAS Inner Detector Technical Design Report. Volume 1.*
ATLAS TDR 4, CERN/LHCC/97-16, ISBN 92-9083-102-2 30 April 1997.

[45] ATLAS SCT collaboration. *Technical Specifications for ATLAS Silicon Microstrip Detectors.*
Note by the ATLAS SCT community.

[46] F.Anghinolfi, W.Dabrowski et al. *Development of front-end electronics for silicon strip detectors using the DMILL BiCMOS rad-hard process.*
In Balatonfuered 1996, Electronics for LHC experiments 483-487.

[47] W.Dabrowski et al. *A single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS silicon tracker.*
In London 1997, Electronics for LHC experiments 153-157.

[48] L-Halbo. *Electronic components , packaging and production.*
Stranberg og Nilsen Grafisk AS, Oslo, 1993, ISBN 82-992193-1-0.

[49] C.Haber. *Summary on Hybrid Technology for the SCT.*
Note for the SCT Steering Group for the SCT Hybrid review.

[50] R.Oliveira, Gandis Workshop, CERN.
Private coummunication.

[51] Geneva SCT group. *Geneva University's activities in the ATLAS SCT group.*
http://schp5.unige.ch/atlas/atlaspage/module/home.html

[52] ATLAS Pixel Detector group. Front www page.
http://atlasinfo.cern.ch/Atlas/GROUPS/INNER_DETECTOR/PIXELS/pixel.html