Development of a silicon detector hybrid for the ATLAS experiment at LHC

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Contents

Preface

To be involved in a project as big as the Large Hadron Collider, LHC, as a part of ones thesis is both challenging and frustrating. I had to get a solid grip on something that has been going on for years before I started and will continue for years to come. The part one can play is to lay a little piece in an enormous puzzle. The main problem was to precisely define the thesis project and also where to end it. As a consequence it took quite a long time to define what there was to do and to put it into a firm framework. When this was done the thesis was so clearly defined as one can expect working in such a large project.

The definition I ended up with, was that I wanted to do schematic for a prototype hybrid and follow it through layout and production. This was interesting in itself, since no one had any experience in doing thick film hybrids at the University of Oslo. In addition I would make all the electronics that was needed around the hybrid to get it operational, which meant building a full test setup around a VME-crate. This test setup I would like to get working by myself, but the actual collection of physical measurement and interpretation of these I had to leave for other students. I would merely point out some of the interesting measurement which could be done.

The experience I gained from the making of the prototype hybrid, I would use to make schematic and guidelines for the layout for a single sided Z-module hybrid for the test beam in 1995. My responsibilities could have ended here, but I was lucky to be the one who first got this hybrid working in a lab setup, using a support PCB made by a new student, and a VME-crate. I also had the opportunity to be in the test beam testing the FElix chip, but then using a PCB made at CERN.

The last part I wanted to do, was to show that our Z-module hybrid concept could fulfill ATLAS technical specifications in terms of radiation length of the silicon barrels. By including some general physics considerations in my thesis I wanted to show that all electronic specifications evolve from the ATLAS physics specifications.

A master thesis is never done alone and this one in no exception. I should thank many people for help, information and support the last one and a half year. I will however only mention a few here.

I would in particular thank Ole Dorholt at the University Electronics Workshop for doing all layouts mentioned in this thesis, except for the level shifter which I did myself in an inspired moment. I would also like to thank my supervisor Steinar Stapnes for valuable comments and corrections to my thesis and support throughout the project.

Chapter 1

Introduction

1.1 CERN and LHC history

At the UNESCO-meeting in Florence in 1950 it was recommended that a European laboratory for physics was formed. In less than three years CERN, The European Laboratory for Particle Physics, was formed.

The headquarter is in Geneva, and today the number of member states count 19 countries[1], and four countries have status as observers.

In March 1984 The European Committee for Future Accelerators, ECFA, found that the TeV region was the right next step to explore in particle physics.

The first step towards the Large Hadron Collider, LHC, came in 1985 when a planning committee proposed a proton collider ring in the already existing LEP tunnel. They found this to be the most cost-effective way to reach the TeV region.

Around Christmas 1994 the project was finally approved. Today one foresee the completion of LHC around 2004, but then with missing magnets. First in 2008 it will run at highest possible energy, which is 14 TeV in the center of mass system, if money can be provided from non-member countries like Japan and USA.

More information about the LHC can be found on the home pages of CERN on the WWW [1].

1.2 Physics for the LHC

The hope is that this leap in center of mass energy will give us a glimpse of new physics. The biggest unsolved problem of particle physics today is mass. How is it that some particles have mass and others do not?

The explanation the physicists have today in their Standard Model is the so called Higgs mechanism. Particles achieve mass by interacting with a scalar field, called the Higgs field.

[1] Most West European countries and some former East Block countries

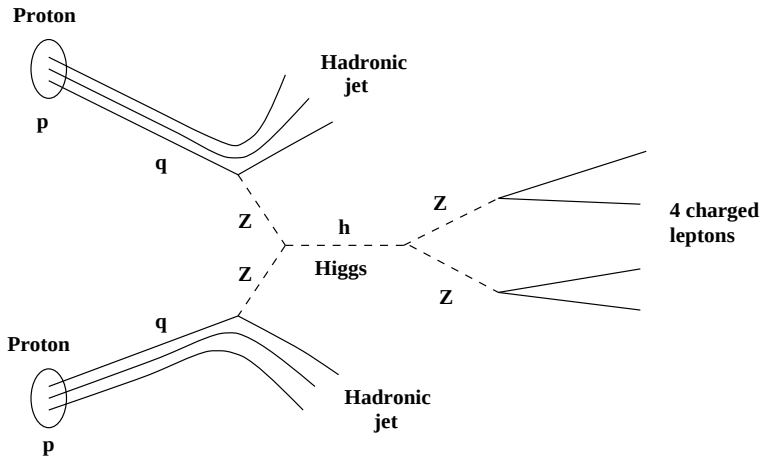

Figure 1.1: A typical Standard Model Higgs event.

The search for the field particle mediating the Higgs field, the Higgs particle, is one of the main motivations for building LHC.

Calculations based on the Standard Model indicate that the Higgs boson should have an energy between 80 GeV and 1 TeV. A typical Higgs event for the LHC is shown in figure 1.1.

Other interesting experiments are the search for the top quark, investigation of charge parity (CP) violation in B-decays and not to forget heavy ion physics.

A search for very heavy W- and Z-like particles, could reveal physics beyond the Standard Model. These models are called super symmetric models, or SUSYs. The Minimal Super-symmetric Extension to the Standard Model, MSSM, will for instance give five Higgs particles.

1.3 Detectors for the LHC

Three detectors are proposed for the LHC project, these are:

- ATLAS, A Toroidal LHC Apparatus.
- CMS, The Compact Muon Solenoid.
- ALICE, A Large Ion Collider Experiment.

The Particle Physics Group at the University of Oslo is involved in the ATLAS project. The next chapter is an attempt to give an overview of the ATLAS detectors and sub-detectors, but only those concerning this thesis are described in any detail. Most of this information can be found in the ATLAS Technical Proposal [3, chapter 3 and 5], and in the Technical Proposal for the SCT [2].

Chapter 2

The ATLAS detector

This detector is designed to be a multi-purpose detector for the LHC project. It consists of several sub-detectors, and the most important ones are:

- Calorimeters.
    1. Hadronic Calorimeter.
    2. Electromagnetic Calorimeter.
- Muon Spectrometer.
- Inner Detector.

An overview of the ATLAS detector is shown in figure 2.1.

2.1 The Inner Detector

The inner detectors sole task is to track and pattern recognize the particles from the collisions. A drawing of the inner detector is shown in figure 2.2. It has an outer radius of 115 cm and a length of 690 cm, and the mass is approximately 1500 kg. It sits in a cavity with an axial magnetic field of 2 T set up by a super-conducting solenoid. There are three major parts, two forward regions and a barrel structure. The inner detector is again divided into sub-detectors, these are:

- The Semi-Conductor Tracker, SCT.
    1. Pixel detector, in the barrel region.
    2. Strip detector, in the barrel region.
    3. GaAs detector, at the end-cap of the barrels.
- Micro Strip Gas Counters, MSGC[1].

[1]Since this report was written, ATLAS has decided to replace the MSGC in the forward direction with silicon strip detectors.

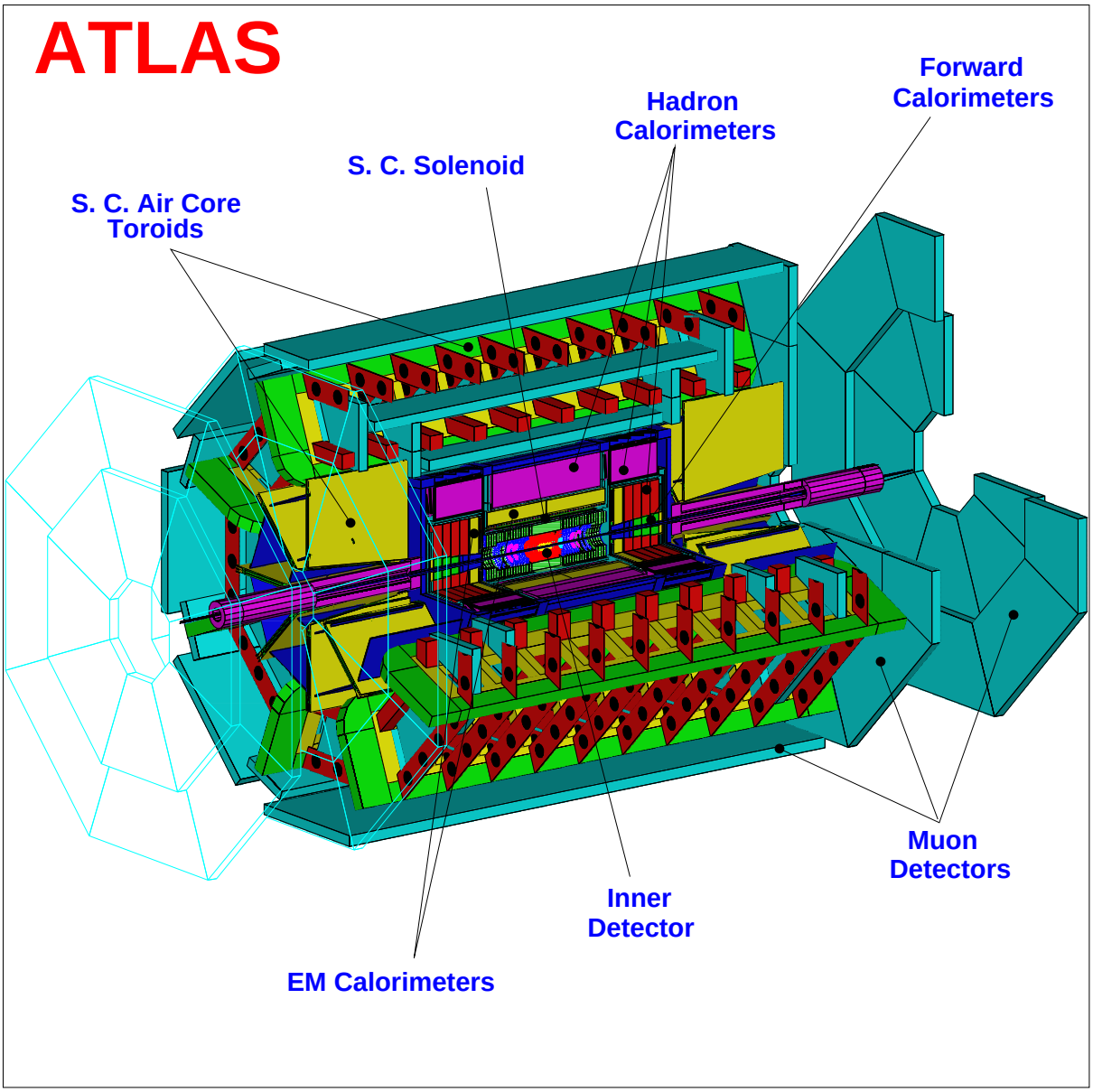

Figure 2.1: The ATLAS detector for the LHC.

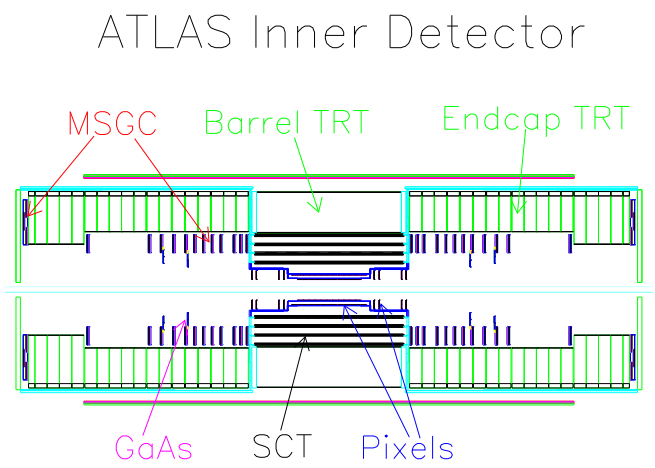

Figure 2.2: An axial cut of the ATLAS inner detector.

- Transition Radiation Tracker, TRT.

2.2 The Semi-Conductor Tracker, SCT

The SCT has to track and pattern-recognize the particles from the collisions. The sagittal resolution of the pixel and silicon detectors is better than 20 μm. The pixel and strip detectors sit in the barrel region, and each barrel has a thickness of only about 1.6% of a radiation length. The GaAs detectors are mounted on structures called wheels in the forward directions.

GaAs detectors tolerate more radiation than silicon, and are therefore chosen over silicon detectors in the end-caps where the level of radiation is much higher.

The SCT pixel and strip detectors are mounted in small modules. Thousands of these modules are mounted on cylindrical supporting shells concentric around the beam.

Pixel detectors are more expensive than strip detectors, but the advantage is better spatial resolution and higher radiation tolerance.

The most cost-effective is therefore to have pixels closest to the beam where the total area is small. Further from the beam where the demands to radiation hardness and spatial resolution[2] decreases, strip detectors are used.

The Silicon Pixel detectors are placed in the two innermost cylindrical shells, at radii 11.5 cm and 16.5 cm, and they are 66 cm and 78 cm long, respectively.

The barrels for the silicon strip detectors are placed at radii 30 cm, 40 cm, 50 cm and 60 cm. The length of the barrels is 160 cm. These four barrels contain 2856 modules

[2]It does not imply a lower angular resolution. If two identical pixel detectors, the first placed twice as far from the beam as the second, they both have the same spatial resolution. But the angular resolution of the detector furthest away is twice as good.

of 144 cm^2 silicon detector area each, for a total of 41 m^2. A detector of this dimension represents a major step forward compared to todays silicon systems. The largest silicon detector today is the micro vertex detector at the DELPHI experiment at the LEP accelerator, which has a silicon detector area of only 0.8 m^2.

A removable vertex layer is planned around the beam pipe. This layer will either be a silicon pixel layer at 4 cm or a silicon strip layer at 6 cm radius, outside to the beryllium beam pipe of 2.5 cm radius. This layer will mainly be used for vertex finding for B-physics during the first few years of operation.

There are two conflicting requirements to a good silicon detector and its support system.

- **Low mass:** This will reduce the radiation length. Lower mass means thinner materials.
- **Solid support structure:** The support structure has to carry the weight of hundreds of silicon modules, cabling and cooling pipes. The requirement to mechanical stability is around 10 μm.

On top of the mechanical problems, there are numerous problems to overcome in electronics.

- **Cooling:** All the silicon detectors and front-end electronics use a lot of electrical power, somewhere between 6 and 12 kW, which makes cooling an important issue. For the cooling, one solution is to force binary ice, which is a liquid solution with ice crystals, through beryllium cooling channels. Along the channel the temperature should be between 0°C to 10°C.
- **Radiation:** To keep the radiation damages of the silicon detectors and the front end electronics at a minimum level, the modules should be kept at 0°C for their entire lifetime, which is approximately 10 years. After this period, surface and bulk radiation damage will put the silicon detectors out of function. The innermost silicon detectors are at distances as close as possible to the beam for a lifetime of minimum 10 years.

If the modules could be kept at 0°C during assembly, operation and repair, it would relax the demands to finding materials with matching coefficients of thermal expansion.

The thesis only concerns hybrid design for the silicon strip detector modules, and the silicon strip sub-system of the SCT will now be covered in more detail.

2.3 The silicon strip sub-system of the SCT

The two major parts of a barrel are the support structure and the detector module. There are two proposed detector modules for the silicon strip detectors, the Z-module and the r/ϕ-module. Both modules consist of two silicon strip detectors with the size of 6 cm by

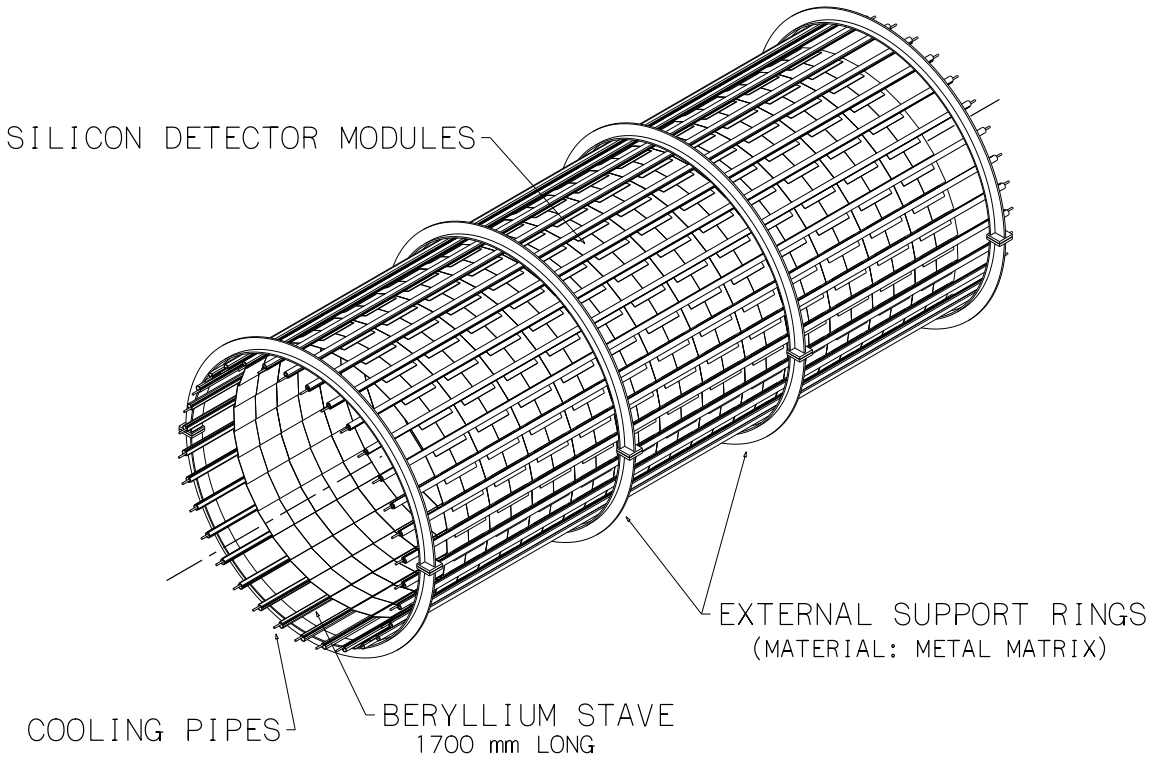

Figure 2.3: Z-module support structure for the barrel at 30 cm.

6 cm each, bonded together to give total strip lengths of 12 cm. The front-end electronics to read-out the strips are proposed made in two different hybrid technologies.

In the next subsections the support structures and the two types of modules will be described.

In the following sections the detector and the electronics will be described, being the most important parts from a functional point of view.

2.3.1 Support Structure

The two detector module solutions use a different support structure. In the Z-module support structure the barrels are made of beryllium staves along the z-axis with four intermediate support rings. The rings are made of a metal matrix, which makes them very rigid. The beryllium staves also contain the cooling channels. The cooling channels along the z-axis of the barrels give us the name Z-module. Mechanical simulations of the barrels show that the total compression under an approximately 500 kg load is in the order of only 10 μm. Beryllium has the lowest radiation length of all materials that are suitable for building a support structure. Low mass and a low coefficient of thermal expansion are other favorable properties. The support structure for a Z-module is found in figure 2.3.

For the r/ϕ-module a carbon fiber composite is considered for the barrel. The modules sit on top of this cylinder, and the cooling channels are placed on top of the modules.

2.3.2 The r/ϕ-module

The r/ϕ-solution uses a hybrid consisting of an adhesive-less copper/kapton laminate on top of a beryllium shield. The shield is then placed on top of one of the two silicon detectors that build a module. The front-end chips read-out the strips at the midpoint where the two detectors are bonded together. The concept is seen in figure 2.4.

The solution is potentially better than the Z-module solution, at least when it comes to radiation length and the input capacitance seen by the front-end amplifiers, contributed by the thin hybrid laminate and the short fan-in, respectively.

Some drawbacks are introduced as well. The biggest one is the fact that the cooling channels cannot be straight, as in the Z-module solution. Instead they twist like a snake to cover the heat producing hybrids, which is not optimal if binary ice has to be forced through these channels.

2.3.3 The Z-module

The Z-solution proposes to use a multi-layer thick film process on a ceramic substrate, known as a thick film hybrid. In order to read-out both detector sides, both ceramic sides need to be processed. Standard ceramics, like radiation thin beryllia, have a thickness of 635 μm and the thick film layers should add only a few hundred μ-meters to the thickness.

The hybrid sits on the side of the two detectors, glued to them with some millimeters of overlap, as seen in figure 2.5.

A fan-in structure is needed to route the detector strips in to the front-end chips. The fan-in can be made of a beryllia substrate, but thinner than the hybrid substrate since it does not play a role in the support.

The extra distance from the strips to the front-end chips, introduced by the fan-in, creates a higher input capacitance for the chips. Higher capacitance requires more current in the front-end amplifiers to maintain a good signal-to-nose ratio, which again increases the demands to cooling.

One good property of the fan-in structure is to transport heat from the detector to the cooling channel. The cooling channel passes over the front-end chips on the hybrid, and is in thermal contact with the fan-in fingers that go between the chips. The self-heating of the detectors can therefore be controlled very well. Thermal runaway studies [4] has shown that the Z-module is better than the r/ϕ-module in this respect.

2.4 Silicon Detectors

A silicon detector is made by etching diodes by a photo-litographic technique on a silicon wafer. The size of a ATLAS detector is 6 by 6 cm^2 and it has a thickness of 300 μm. For analog read-out a read-out pitch of 112.5 μm is chosen, which gives approximately 2.9 million silicon strip channels to read-out.

When a voltage of more than 40 V is present over the diodes in the backward direction, they are fully depleted, and function as a detector. A charged particle with a relativistic

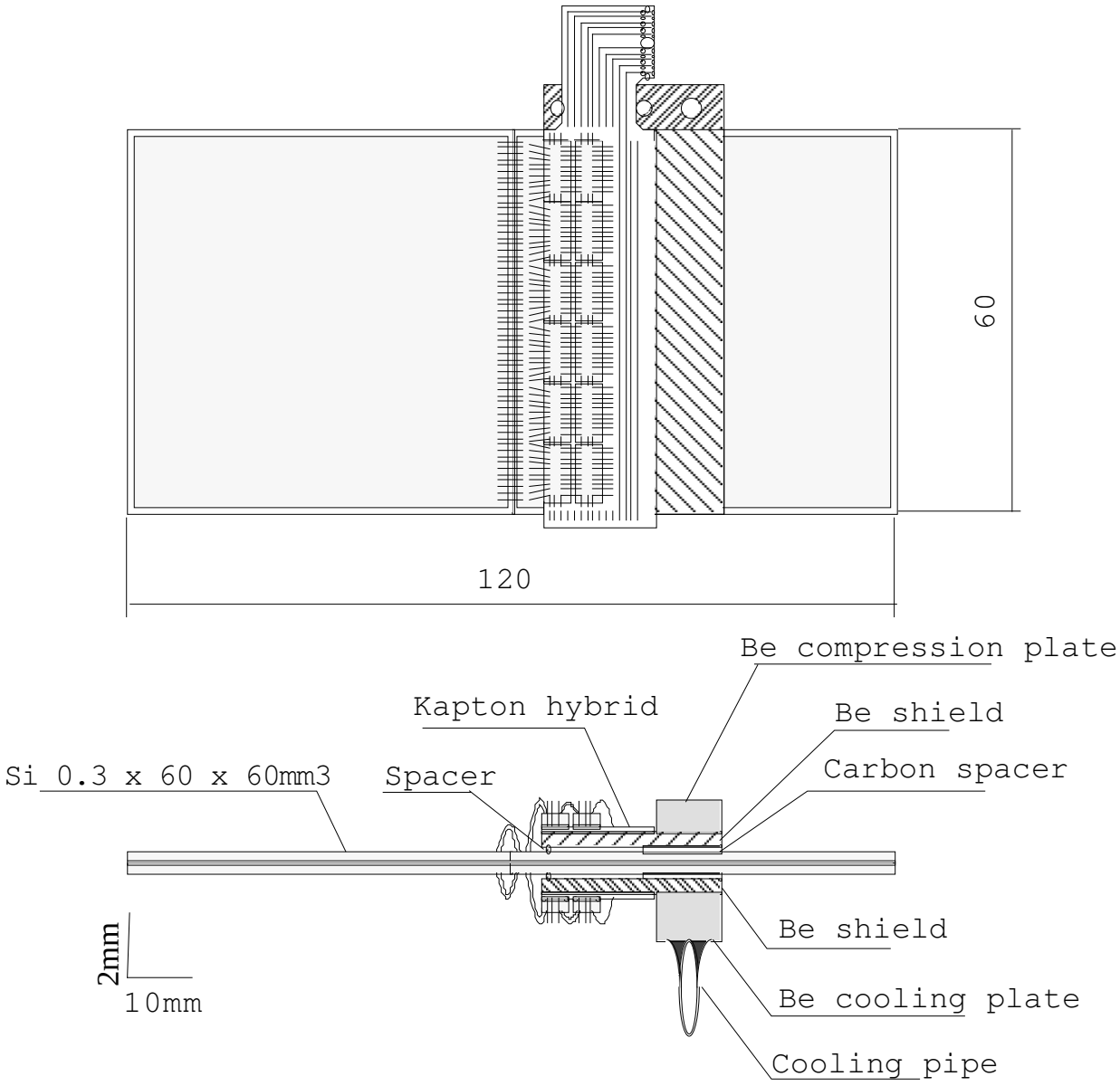

Figure 2.4: The r/ϕ-module concept for the silicon detector barrels.

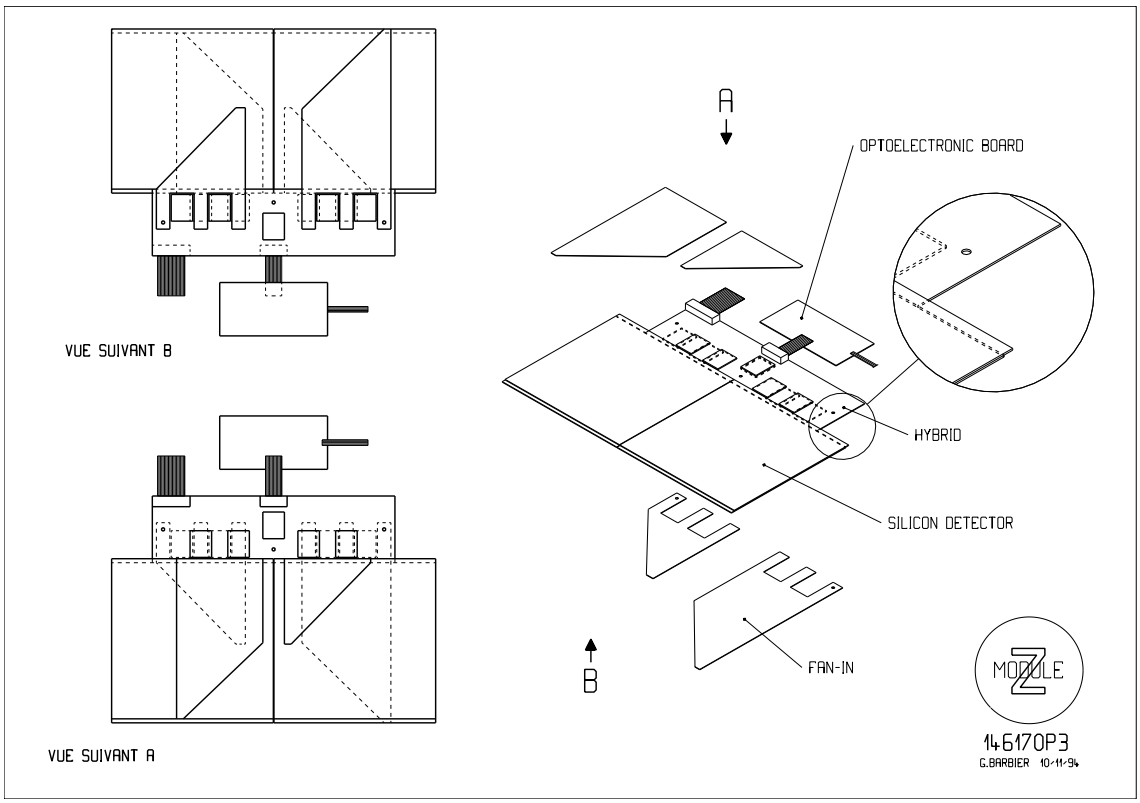

Figure 2.5: The Z-module concept for the silicon detector barrels.

velocity, which crosses the detector, releases around 22000 electrons by ionization over just a few nanoseconds. The current spike, with the approximate shape of a δ-pulse, is divided by neighboring strips and picked up by the front-end amplifiers. By the charge distribution between the strips the position of the crossing can be found with a resolution of approximately 20 μm, which is sufficient for the reconstruction of the particle tracks. The pitch is chosen so that one minimizes the number of channels and cost to the point where the 20 μm resolution is first achieved.

The main discussion is whether to choose double-sided detectors or single-sided detectors glued back to back. The first alternative has of course lower radiation length and less heat generation as good arguments. The single-sided design is less demanding when it comes to design and how to supply the power for the detector. For the single sided version both p+ and n+ read-out-implants and n or p bulk are evaluated. All these types are under prototyping.

The resolution of 20 μm is in the r/ϕ-direction in a cylindrical coordinate system with the z-axis along the barrel axis. The demands to resolution in the z-direction is only in the order of 0.5 mm. This is achieved by having the strips on the back side of the detector rotated a small angle of 40 mrad. This makes the construction of read-out electronics much simpler, because all strips are almost parallel and the read-out electronics can be almost symmetric on both sides of the detector.

Radiation damages are categorized into surface and bulk damages. Surface damages are controlled by production techniques and contribute much less to the problems than the bulk damages. Bulk damages of various sorts exist. An example is damage to the silicon lattice, which creates new energy levels in the middle of the energy gap for the semiconductor. This leads to higher leakage currents, which again leads to more noise and higher power consumption. A general discussion of detectors for the ATLAS project can be found in [2, chapter 4].

2.5 Silicon Strip Electronics

Three main architectures are described for the read-out of the detectors. These are:

- **Analog.** A pre-amplifier implemented in bipolar or CMOS followed by an analog pipeline and a fast analog MUX. All pulse heights are read-out optically.
- **Digital.** The AMUX is replaced by a sparsification unit using an ADC. One reads out optically the digitized values which are above threshold.
- **Binary.** A fast bipolar pre-amplifier, shaper and comparator is followed by a digital pipeline. One reads out optically the bit patterns corresponding to the discriminated value.

Optical read-out means either Multi Quantum Well, MQW, or Light Emitting Diode, LED. The MQWs has the advantage of dissipating very little power, but even LEDS

dissipate only about $5\,\mu$W/channel for digital and 200μW/channel for analog read-out. The production technologies are radiation hard. LEDs are an older and more evaluated technique and may be a safer approach.

Bipolar technologies are inherently radiation hard. The minor damages are almost eliminated by minimizing the thickness of the base of the bipolar transistors. This does not hurt the performance since thinner bases give faster transistors.

For CMOS one has to choose certain radiation hard production techniques. Two different approaches exist. They are called bulk and silicon-on-insulator, SOI. The effect of production techniques on radiation hardness for CMOS devices are well enough understood to make chips that will survive for the expected 10 years of operation, without a significantly increase in noise levels.

The noise limit is set at approximately 1500 equivalent noise charges, ENC, after 10 years of operation. The equivalent signal-to-noise ratio is 15 for a minimum ionizing particle, MIP, which releases about 22000 electrons. Another key consideration is minimizing the power consumption, here a maximum of 4.8 mW per channel is chosen.

The front-end chips FElix from Sintef/SI and APV5 from RAL, which will be discussed in the following, fit into the first two read-out schemes.

The APV5 from RAL is produced by the UK branch of the US company Harris and is radiation hard. The FElix has so far been produced by the Austrian AMS in a non-radiation hard technology. Radiation hard versions in Harris or DMill processes are being considered.

Chapter 3

The Test Hybrid

Two hybrid iterations were made.

- A first two chip test hybrid for the 32 channel FElix was made together with an accompanying printed circuit board, PCB. Familiarity with design, layout and production of thick film hybrids was gained.
- A second four chip single sided hybrid for the 128 channel FElix, also with a PCB, was made for the test beam in the autumn of 1995.

This chapter describes the test hybrid design and production, and the extra electronics needed in order to make it work in a lab setup.

As for the second iteration, only the hybrid and the support PCB were made at the University of Oslo. While for the beam test one would need to put on the detectors and the fan-ins. In addition a box to shield it from light is needed. All this has to be placed on a beam telescope. Since groups in the UK[1] were making full Z modules, including hybrids, for the APV5 front-end chip, the full FElix128 hybrid was made compatible with the mechanical support delivered by the UK groups.

3.1 Why a hybrid?

Why is a hybrid in a thick film technology needed? Some important answers are:

- Space requirements. Each layer add very little to the total thickness, as compared to the laminate of a PCB.
- It has a low radiation length, when a beryllia substrate is used.
- It has superior high frequency characteristics compared to a PCB.

[1]Birmingham, Cambridge, Liverpool, Oxford and London Universities, Queen Mary Westfield College and Rutherford Appleton Laboratory.

- Mechanical stability of a ceramic substrate is much better than that of a glass/epoxy based PCB.
- The thermal conductivity of beryllia is much higher than for a PCB.

All specifications for the ATLAS electronics derive from the physics the detector need to be sensitive to. The hybrid and electronic specifications are summarized:

- 112.5 μm detector read-out pitch for analog and digital read-out and 75 μm for binary read-out. The spatial resolution then achieved is better than 20 μm in the ϕ-direction. The z-direction demand is in the order of 0.5 mm, achieved by rotating the strips on the detector back side by 40 mrad.
- Two and two detectors are bonded together to give total strip length of 12 cm. The length is limited both by occupancy and the input capacitance the strips give the front-end electronics.
- To reduce radiation length thin materials need to be used in detectors and front end electronics. Since beryllia substrate has a low radiation length, thick film hybrid technology is a possible solution.
- The high luminosity leads to the need of radiation hard technologies both for detectors and front-end electronics.
- The low cross section of the interesting physics like Higgs events leads to the enormous collision rate of 40 MHz to boost the luminosity. Full read-out of millions of strips at a rate of 40 MHz, would be an impossible task. Therefore the data is pipelined in analog or digital arrays until a first level trigger can discard most of them.
- Signal-to-noise ratio of 15 of the front-end electronics after 10 years of operation. In this way one can maintain an efficiency above 99% with an occupancy below 10^{-3} and the spatial resolution better than 20 μm.

3.2 Schematic, components, layout and production

3.2.1 The hybrid schematic

For the drawing of the schematic Viewdraw is used. Viewdraw is a schematic design tool from Viewlogic. A full Viewlogic package consists of a multitude of tools. Digital, analog and mixed circuits or for instance Field programmable gate arrays, FPGAs, or other highly specialized circuits can be drawn. The circuits can then be simulated in several ways. Analog circuits typically by different SPICE versions, and digital circuits by a tool called ViewSim.

The schematic for the test hybrid is drawn on a single sheet, as shown in figure 3.1. The only active components are the FElix chips and the analog multiplexers, AMUXes.

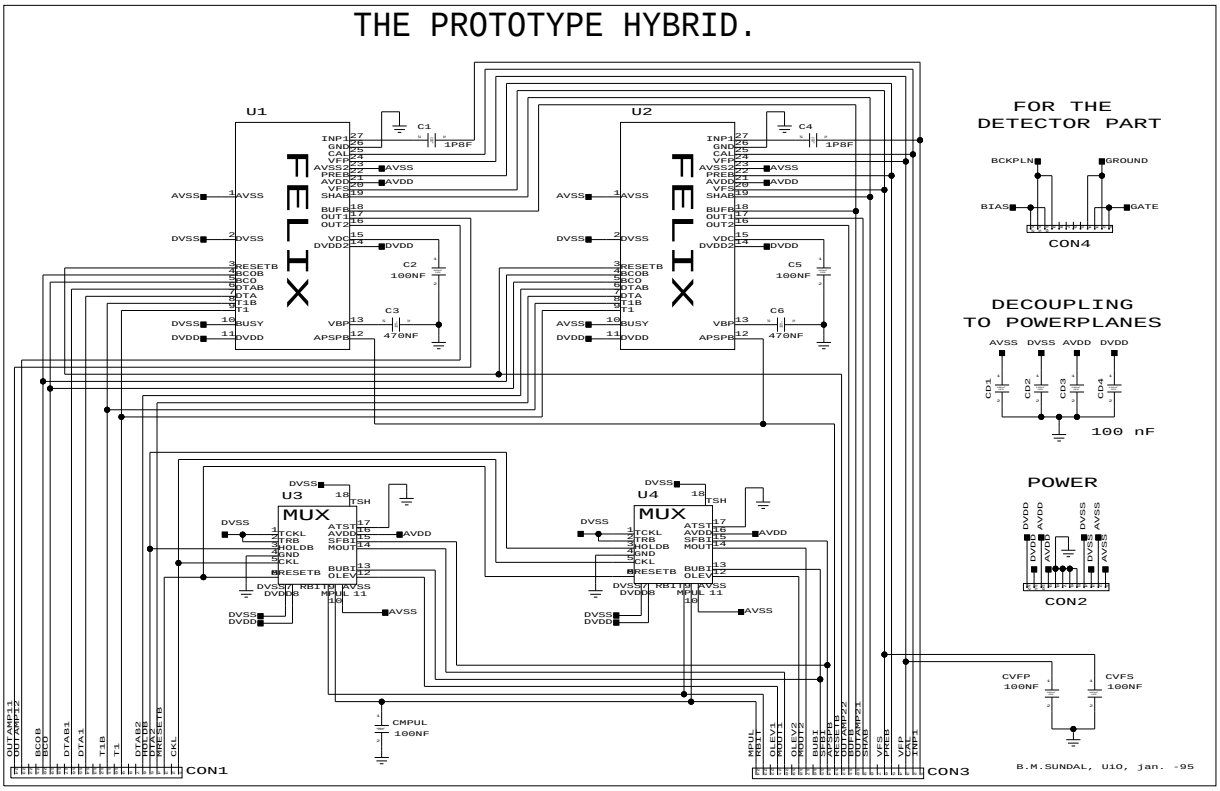

Figure 3.1: The schematic for the test hybrid.

The rest of the components are connectors and capacitors for decoupling. The purpose of the hybrid is mainly to house the active chips and to provide an interface (through the connectors) to a PCB, which can provide input signals (biasing and digital signals) and take care of the analog and digital outputs.

One of the biggest problem in making the schematic was to collect all the about the FElix and AMUX, in order to provide the chips with all necessary signals. The symbols for the chips in the schematic contain only pin information, and not any simulation information. The hybrid can therefore not be simulated electrically. The symbols do not contain any information of the analog input pads from a detector, or the output pads bonded across to the AMUX. This is because these bondings have no connection with the hybrid, and are as such of no interest to the schematic and layout of the hybrid. The symbols do not contain any information about pads that are not used, even though they exist. All signals of the chips are shown in figure 3.9.

The hybrid cannot be fully simulated. Therefore, to reduce noise, the following basic rules have been used.

- Keep analog and digital signals well separated.
- Separate power for the analog and digital parts.
- All biasing and power voltages must be decoupled.
- Make power and ground separate planes. Critical signals can be shielded from one another by means of these planes.
- Short tracks are better, because one reduces the capacitance of the track and its ability to pick up nearby signals.
- A signal with very fast rise or fall time should have its inverted signal very close to its own track in order to reduce pickup.

The FElix signals BCOB and T1B are examples of this type of signals. They are dummy signals, and only have bonding pads on the FElix, but are not connected to anything else internally. It was decided to keep these signal tracks on the hybrid. When the tracks for a pair like T1 and T1B are close to each other, they give less pickup noise on other signals then if one of them were alone. This is because that whenever one has an abrupt change in one signal, one has an equal but opposite voltage change in the B-signal, which tend to nullify the effect of pickup on other signals by parasitic capacitances and induced power fluctuations.

Since all other tests of the FElix had been of one single chip on a single PCB, it was decided to make a hybrid with two FElix chips.

After a discussion with the chip designers the two FElixes were decided to have common analog biasing from the PCB. The two only exceptions are the biasing voltages VDC and VBP, which were separately decoupled to ground. No opportunity of putting them on a

fixed voltage were provided, in order to reduce the number of signals brought out over the connectors. Also for the AMUXes, the biasing is common for the two chips.

The explanation of how the hybrid works, and the motivation of what signals to bring out is discussed in the test setup section. This is because the hybrid is just a carrier for the chips. To understand the read-out one really needs to look at the system of hybrid and support PCB.

The active part of the hybrid, the CMOS chips, will now be described.

3.2.2 FElix, a Front-End Amplifier

Sintef/SI in Oslo has developed a front-end amplifier called the FElix. The chip follows the original silicon detector read-out concept proposed by the RD20 collaboration. The first full chip was produced early in 1994, in 1.2μ non-radiation hard CMOS process of Austrian AMS. It could read-out 32 channels of a silicon strip detector. A simple figure of the read-out concept can be found in figure 3.2.

Earlier read-out chips for silicon detectors, like the VIKING, have a signal-to-noise ratio in the range 40-80 [5]. The problem at LHC, as mentioned in the previous section, is that the physics going to be studied in ATLAS has very small cross section. In order to get a reaction rate high enough to observe a reasonable amount of interesting events, one has to increase the luminosity by boosting the beam crossing rate to 40 MHz. This means that slow charge collection in the order of μs is not an option. The increased luminosity also requires radiation hard technologies.

The level one trigger occurs at a rate of maximum 100 kHz, which means that only one of 400 events on the average is sent on to the stages following the pipeline. Since the time bin for an event is 25 ns, the pre-amplifier should be able to sample and process a read-out value from a strip in this time interval. Such a fast amplifier has a bad signal-to-noise ratio, and it uses a lot of power compared to slower amplifiers. Neither is acceptable. The solution is to use a slower pre-amplifier and shaper, and later use a de-convolution scheme to recover the timing information and the signal. Deconvolution reduces the parallel noise with 40% and increases the series noise with only 6% compared to simple fast CR-RC shaping [6].

Each channel does the signal processing described below. A more thorough description of the deconvolution architecture can be found [6, pages 217-227].

The small current spike from the detector is first put through a fast charge-sensitive pre-amplifier, which has a gain of 1 mV/fC. The signal is then shaped by a slower CR-RC shaping amplifier network to give a pulse with a peaking time of 75 ns, which is 3 beam crossing intervals, BCOs. The gain of this stage is approximately 20.

The analog delay and buffering unit, ADB, samples the signal at 40 MHz (the BCO-rate) and keeps it $2\,\mu$s in its pipeline in order to let the first trigger decision arrive. The trigger decision is made on the basis of either muon or calorimeter data. If a trigger pulse (T1) arrives, four samples concerning the interesting event are pulled out at the end of the pipeline. The continuous read-out frequency of the FElix is 250 kHz. That is, if several triggers occur within a short time interval the FElix will put them out one at a time at a

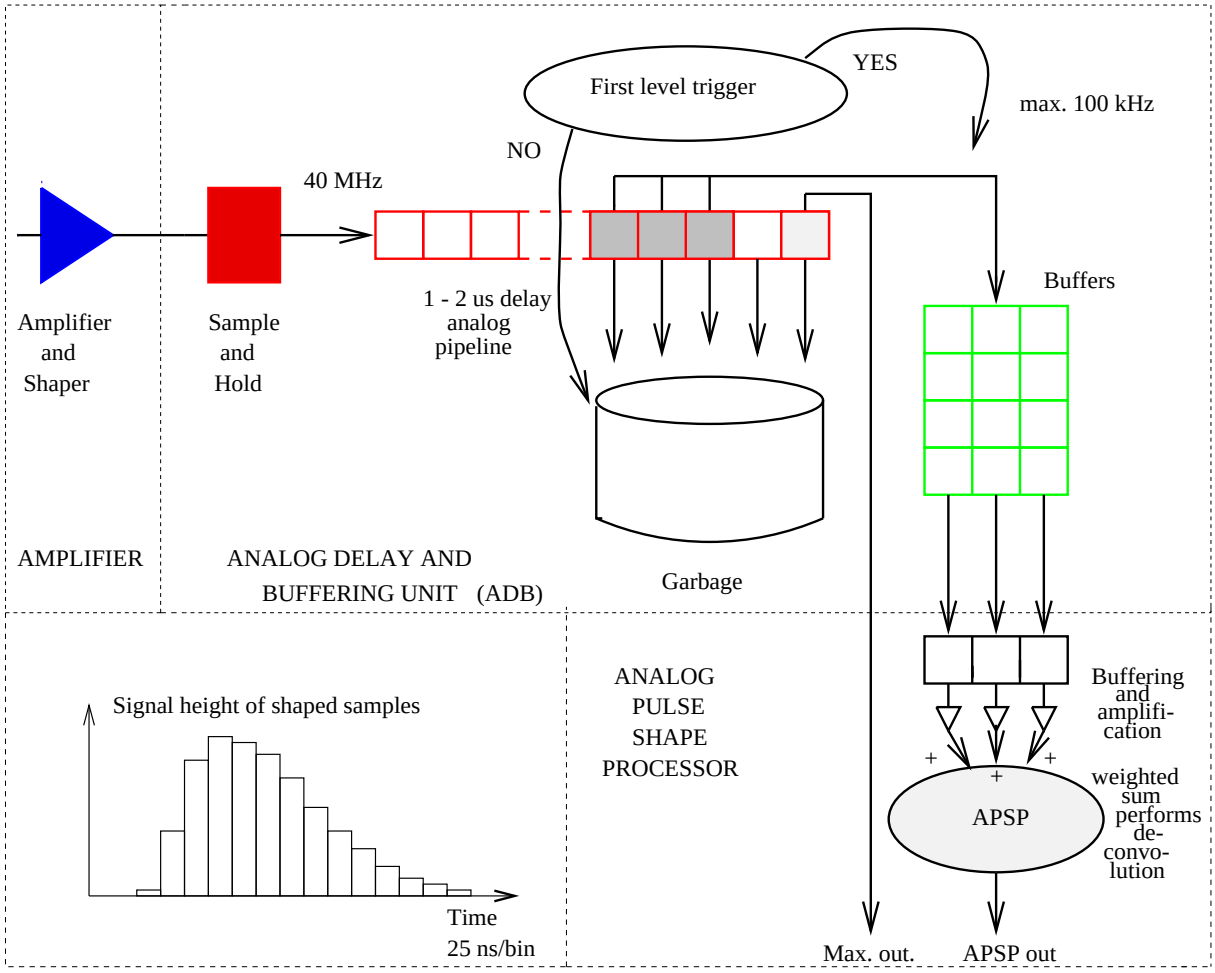

Figure 3.2: Functional description of the FElix chip.

rate of 4 μs per event. The processing of a single event takes 4.775 μs. The maximum T1 rate is 100 kHz, which corresponds to a mean T1 arrival of 10 μs.

Three of the four samples are put through the analog signal processor, APSP, which de-convolutes the shaping done by the CR-RC shaper, and gives an output proportional to the height of the shaped signal out of the ADB. This is not the total height of the ADB signal, but only the part associated with this trigger. Because of pile-up from earlier triggers due to the long shaping time, the total height of the pulse can be higher than the contribution from a specified trigger. The fourth sample associated with the total pulse height out of the ADB is also put on the FElix output. This is put out first, for a period of 550 ns. Then after 250 ns, which is the signal reset time of the output, the de-convoluted signal is put out for 550 ns. To indicate that there are valid signals on the 32 analog outputs (from the APSPs) the DTA signal is high for the same periods.

The BUSY signal can be used by electronics following the FElix in the read-out chain, to slow down the FElix read-out. BUSY can be asserted anywhere in the time slot from one BCOs after the first DTA to 13 BCOs after the second DTA. The FElix will then finish the read-out of the event associated with these two DTA-pulses, but will not start to read-out any more events before BUSY is brought low again. Events associated with triggers in the interval BUSY was high, will be read-out as soon as BUSY goes low. If the following electronics is fast enough the BUSY signal can be hardwired low.

After testing during 1994 ATLAS H8 test beam run some minor analog problems were spotted, but the overall performance of the first FElix was good. In the next 32 channel version of this chip, finished in January 1995, the analog problems were fixed. That is the pre-amplifier current was raised from 300 μA to 700 μA, which should give a better signal-to-noise ratio. The input amplifier to the APSP from the ADB was redesigned so it looked more like the pre-amplifier, which resulted in less pickup from the clock than earlier. The chip was also less sensitive to changes in the biasing, and the signal outputs of the broken channels were stronger. The shaping time were shortened a bit, but this proved to be unnecessary.

There are two versions of the latest 32 channel FElix, both incorporating these analog changes. The difference is in the digital logic, which is made much more robust with respect to timing variations. One of them uses the old digital logic with the APSP starting its read-out clock a fixed time after the trigger, and the the other with a continuous 1.25 MHz APSP clock. This means that the FElix with the new digital logic does not give an APSP output on a fixed time after the trigger. The problem that one had to make a full reset of the FElix for each event read-out was also fixed.

Table 3.1 describes briefly the signals on the latter 32 channel versions used on the test hybrid. The input and output pads (32 of each) are not listed. The signals not used are marked with a star.

Figure 3.9 shows how the FElix and AMUX are bonded up on the test hybrid, and can serve as a reference of how the chips look. The figure shows all pads, also those not in use. The size of this FElix is 9677 μm by 4642 μm, and the size of the AMUX is 2434 μm by 2206 μm.

Pad/Signal	Description
AVDD	+2V analog power.
AVSS	-2V analog power.
DVDD	+2V digital power.
DVSS	-2V digital power.
GND	Ground.
VFP	-0.4V for pre-amplifier feedback resistor.
VFS	0.3V for shaper feedback resistor.
VDC	Grounded through 100nF capacitor, Backplane ADB storage capacitors.
VBP	Grounded through 100nF capacitor. APSP backplane capacitors.
PREB	700μA for pre-amplifier bias current.
SHAB	120μA for shaper bias current.
BUFB	80μA for pre-amp/shaper output buffer.
APSPB	20μA for APSP bias current.
BCO	40MHz clock. At least 0.5V swing around +0.2V. 0.5V amplitude around ground should always be OK.
BCOB	Dummy bond pad for inverted of BCO-clock.
T1	FElix trigger, over 0.5V to trigger, less than -0.5V is OK low level.
T1B	Dummy version of T1, implemented to reduce pick up.
RESETB	Low to reset FElix chip, that is lower than -0.5V.
BUSY	Digital control input. FElix outputs data when ready if BUSY is pulled low by external logic.
DTAB	Open drain inverted output.
DTA	Open drain output, data available from FElix.
CAL	0.07V step excite all channels with 1 MIP.
INP1	Analog input to inject a charge in the first broken channel. 1 MIP for 2mV step, if ext. capacitor is 1.8pF.
INP2*	Analog input for the pre-amplifier in the second broken channel.
OUT1	Analog output from pre-amp. in first broken channel.
OUT2	Output from pre-amp. in second broken channel.
OADB1*	Output of ADB in first broken channel.
OADB2*	Output of ADB in second broken channel.
IAPSP1*	Input to APSP in first broken channel.
IAPSP2*	Input to APSP in second broken channel.
OAPSP1*	Output of APSP in first broken channel.
OAPSP2*	Output of APSP in second broken channel.

Table 3.1: Description of FElix32 signals for the test hybrid.

3.2.3 Analog MUX for FElix read-out

For the read-out of the FElix an analog multiplexer, AMUX is used. The AMUX is constructed at CERN [7] [14] and produced in the same AMS technology as the FElix.

The AMUX was constructed for the read-out of the first FElix for the beam-test in 1994. A single FElix and a single 32 channel AMUX was then put on a PCB, containing all the electronics needed for the biasing and line driving of the analog signals.

The bonding pads for the input signals from the FElix were ordered in one row with a pitch of 42.4 μm.

The read-out clock can be operated at maximum 20 MHz, and the AMUX has to be provided with this clock or a slower one through the BUFCKL-pin. In the -94 beam test this clock was not continuous, but rather a sequence of 32 cycles of a 5 MHz clock applied at the right moment. This sequence along with the other control signals are generated from the sequencer module, called SEQSI, in the VME-crate.

A 32 channel FElix was read-out in $\frac{32}{5\,\mathrm{MHz}} = 6.4\,\mu$s, using this sequence. One observes that the time it takes to read-out the AMUX is more than the minimum time between outputs from the FElix, which is 4 μs as mentioned in the previous section. In order to read-out the FElix without use of BUSY, an AMUX that can run at 40 MHz is needed, and will be constructed in the future This 40 MHz AMUX128 will be implemented in a single chip together with the first FElix128 (128 channels), to make the second generation FElix128.

The functionality of the AMUX is shown in figure 3.3 A more thorough description exists from the chip designer [7].

Each channel has an input switch and a storage capacitor followed by a input buffer, which together build a sample and hold unit. The input buffer is a source follower based on NMOS transistors, which give a voltage gain of 0.75. This leads to the total voltage gain of 0.75 of the whole AMUX. The input switches are controlled by the BUFHOLD signal. The BUFHOLD signal is asserted low.

The multiplexing is achieved by a row of 32 switches, one for each channel, that feed the same analog bus line with their output. This line is connected to a pull-up resistor to increase the current in the read channel, which improves the falling edge of the signal. To ensure that one and one channel outputs at a time, the switches are controlled by a shift-register (a row of D flip-flops). Sending a logic one down through this shift-register enables a new channel switch for each clock-cycle. To introduce this read-out bit to the first D flip-flop, the chip is provided with the pin RBITIN. The bit is clocked in on the negative edge of the CKL.

The fourth and last digital control signal of the AMUX is the RESETB, which is asserted low. This signal resets the shift register. An example of the timing relations between the four digital control signals is shown in figure 3.4.

Since the FElix also has a signal called RESETB, the AMUX signal is renamed MRESETB in the schematics. In schematics the other digital signals are given shorter names. The BUFHOLD, BUFCKL and RBITIN are simply called HOLDB, CKL[2] and RBIT. The

[2] The erroneous CKL is kept. A short form for CLocK ought to be CLK.

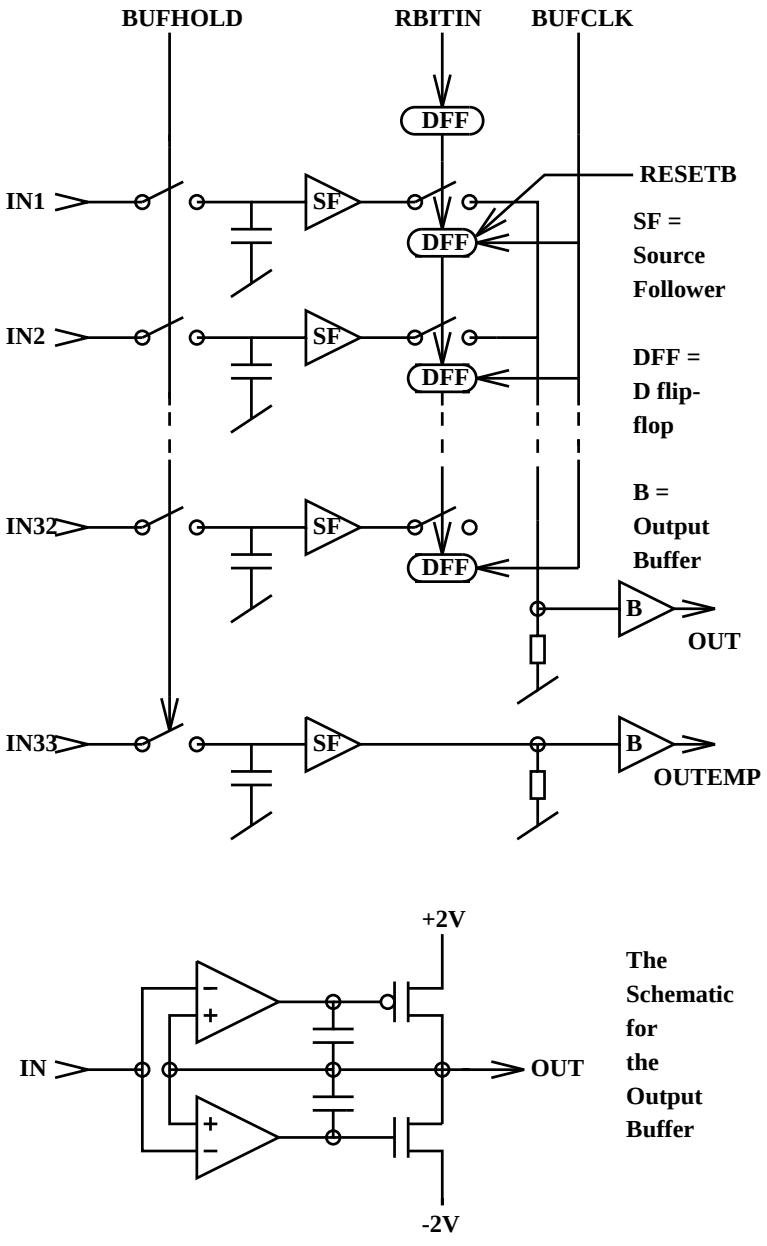

Figure 3.3: Functional description of the analog MUX.

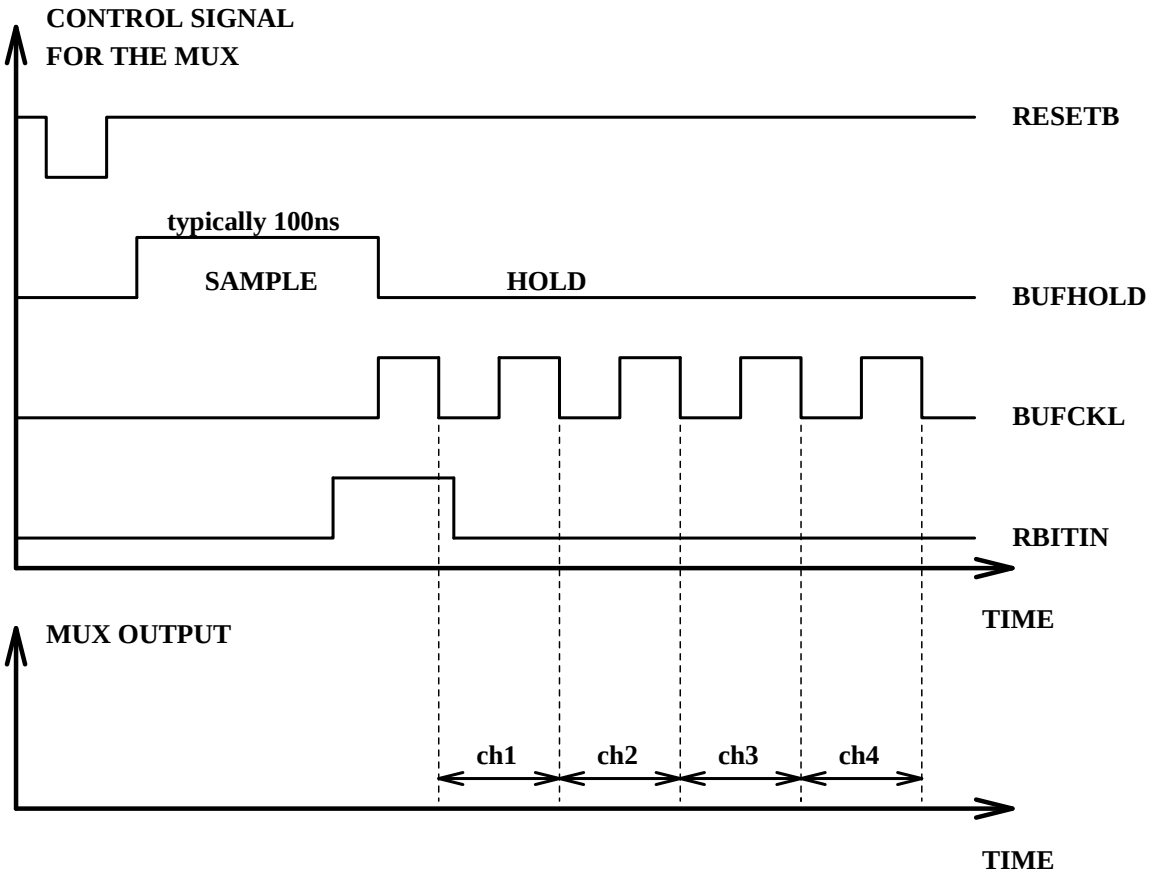

Figure 3.4: Digital control timing for the AMUX.

B in the end of the HOLDB and MRESETB indicates that these two signals are active low, in contrast to RBIT and CKL, which are active high. But mark that the AMUX clocks the read-out bit in the end (falling edge) of the CKL.

The chip also contains an additional multiplexer for test purposes. The inputs to this AMUX is called BUFTCKL, TRESETB, TSHIFTIN and ANTESTINP. During normal operation the three first ones are connected to digital $-2\,\mathrm{V}$ and the last one is grounded. These signals are named TCKL, TRB, TSH and ATST in the schematics.

To limit cross-talk and offset from the digital part, an extra single channel is implemented to be used as a reference. The output of the AMUX is therefore differential. The output buffer is a quasi-complementary configuration. It has a low output impedance and a high signal swing.

The performance of the AMUX is good. Just make sure to notice the limitation of 30 pF in the capacitive load specification. This means that it can not drive more than short lines. The supply voltage is $+2\,\mathrm{V}$ and $-2\,\mathrm{V}$, both for the analog and digital part. The power dissipation is less than 50 mW. The maximum nonlinearity is less than 1 percent, which is insignificant since it drowns in the expected noise introduced by the front-end chip, anyway.

Pad/Signal	Description
AVDD	+2V analog power.
AVSS	-2V analog power.
DVDD	+2V digital power.
DVSS	-2V digital power.
GND	Ground.
MPUL	1 V, for bias voltage for pull-up resistor.
BUBI	150 μA bias current for the output buffer.
SFBI	20 μA bias current for sample and hold buffer.
MRESETB	Resets the shift register. Active low.
CKL	The shift register clock, max. 20 MHz.
HOLDB	Selects sample or hold, HOLDs when low.
RBIT	Input of shift register, active high.
MOUT	The analog MUX output.
OLEV	The reference part of the analog MUX output.
TCKL	Test clock, to -2 V digital in normal operation.
TRB	Test read bit, to -2 V digital in normal operation.
TSH	Test sample/hold, also to -2 V in normal operation.
ATST	Analog test input, grounded in normal operation.

Table 3.2: Description of AMUX32 signals for the test hybrid.

The signals of the AMUX32 are summarized in table 3.2 and in figure 3.9.

3.2.4 The hybrid layout

The layout for the hybrid is made at the electronics workshop at the Physics Institute at the University of Oslo [19]. The layout is made using CADSTAR, which is a PCB layout tool from Zuken-Redac.

A meeting with AME, the Norwegian company situated in Horten, which produced our test hybrid, early in the autumn of 1994, revealed that there are not any major differences between the layout of a PCB and a hybrid. The biggest difference is probably in the fact that one needs to specify how the insulating layers will look, since they are printed in the same way as the conducting layers.

For the capacitors, which are the only passive components, it was decided to use surface mounted components. Mostly in the series 0805, but two of them in the series 1206. The space used by a 0805 component is 2 mm by 1.25 mm, and for a 1206 3.2 mm by 1.6 mm.

For the connectors Flex Connectors from DuPont are used. The connectors have 0.5 mm pin spacing, sufficiently low to bring out the amount of signals wanted from the hybrid. The Flex connectors need kapton (polyetylen) cables. The cable is a plastic film with

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Figure 3.5: Layout of the kapton cables for the test hybrid.

a thickness in the range 150 μm to 250 μm. The tracks are printed on this film using a standard photo-litographic PCB production process. Figure 3.5 shows the layout of the kapton cables in scale one-to-one for the test hybrid. The upper cables are for CON4, the middle ones for CON2 and the lower type for CON1 and CON3. Here the connector numbers refer to the schematic in figure 3.1. From the finished film, one can then cut out the cables as one like. The tracks are of copper, with a layer of gold on top. The cables do not tolerate very much bending before the brittle copper/gold tracks suffer very thin cuts, which are almost impossible to see. They are first noticed when ohming the cable, and no connection between the two ends are found.

The decision was to make a hybrid with four conducting layers. The bottom layer is a power plane, which is a conducting plane divided into four parts. Each part for one of the supply voltages, AVSS, AVDD, DVSS or DVDD. The next conducting layer is the bottom signal routing. Above this is the ground plane, and on the top is another signal routing layer. The four conducting layers, as well as the insulation layers, bond pad layer and solder stop layer, are shown in figures 3.6 and 3.7 in scale one-to-one, whereas the top layer with component placement and names is shown in figure 3.8 in scale 3-to-1.

The figures have text naming the layers. The comment in parenthesis in these figures refers to the column named '**Screen name**' in table 3.4 describing the individually screens printed.

There are three insulation prints between each pair of conducting layers. The insulation should go all over the hybrid except from where the vias (electrical connection between two conducting layers) should go. In the topmost of these three printed insulation layers the vias are a bit bigger than in the bottom one. Only the topmost insulation printing screen, of the three building a full insulation layer, are shown in figure 3.6.

The finished layout in CADSTAR was imported to a Gerber-program, where one makes a file for each layer. It is the output from the Gerber-viewer that is shown in figure 3.6 and figure 3.7. When defining the layers, AME, wanted the conducting layers to be specified as positives, the black in the figure representing the actual conducting track. The black indicates the holes in the printing screen, so that conducting paste is printed through these holes in the printing process.

The films for the insulating layers, AME wanted to be given in inverted form. Here black means where there should be no holes in the printing mask for the insulation. The viafill goes where the black is in these layers. From the files we provided AME with for the insulation layers, they made printing masks for both the insulation and for the viafill.

The bond pad layer is given as a positive (black where the bond pads should be), whereas the solder stop layer is given as a negative (black where there should be no solder stop).

3.2.5 Production and mounting of the test hybrid

Ten hybrids were produced by AME. They are printed on an alumina substrate, with the size 0.635 mm $\times$ 34.7 mm $\times$ 60.7 mm.

Bottom layer, power plane.
(**Layer 1**).

First 'insulation' layer.
(Via-fill 1.2).

Second layer, bottom route.
(**Layer 2**).

Second 'insulation' layer.
(**Via-fill 2.2**).

Third layer, ground plane.
(**Layer 3**).

Third 'insulation' layer.
(**Via-fill 3.2**).

Figure 3.6: Layout (Gerber files) for six layers of the test hybrid.

Fourth layer, top route.
(**Layer 4**).

Solder stop layer.
(**Solder-stop-layer**).

Bond pads in gold.
(Negative of **Bond-pad-layer**).

Figure 3.7: Layout for three more layers of the test hybrid.

Figure 3.8: Component names and placement for the test hybrid.

Specification	Value
Min. conductor width	200 μm
Min. conductor distance	200μm
Min. via dimension	300μm x 300μm
Min. via insulation distance	300μm
Bonding pad size	300μm x 500μm
Min. conductor to chip distance	250μm

Table 3.3: A list of some design rules from AME.

There are four conducting layers, called power plane, bottom route, ground plane and top route. The conducting material is a silver-palladium alloy. Approximate thickness of a conductor is 10 μm. It is easy to solder onto silver-palladium, but it is not possible to bond onto it. For the bonding pads there are printed an extra layer on top with bonding pads in gold. The bonding pads are printed in the size 800 μm $\times$ 300 μm. 300 μm is overlap with the track in the top layer, so that the usable bond pad size is 500 μm $\times$ 300 μm. The part of the bonding pad that overlaps the silver/palladium track is unusable for bonding because of the migration of silver/palladium into the gold. The possibility of making a battery effect between a bond pad and the ground plane underneath, which might cause small pieces of the bond pad to peel of, forced us to have holes in the ground plane right underneath the bond pads.

There are three insulation layers between each pair of conducting layers, each with a thickness of approximately 15 μm. The major ingredient in the insulation is aluminum oxide, Al_2O_3. When printing the insulation layers, one gets holes where the vias are going to be. To fill these holes with conducting material one has separate screen printings of viafill. In order to reduce the possibility of these vias not being properly filled, the size of the vias are stepped up in the topmost of the three layers making a full insulation layer. This is seen in table 3.4

Table 3.3 shows a list of specifications for the thick film process at AME. Table 3.4 lists the different layers that are screen printed. The layers in this table which are marked with a star, Gerber files were provided for. The rest of the layers AME made files for themselves by inverting appropriate layers from the files they received. The double star on the solder stop layer indicates that this layer was provided inverted. AME had to invert it before making the printing screen for this layer. From all these files AME made the printing screens, a total of 18 screens. The printing then consists of 21 prints, since the screens Insulation 1.1, Insulation 2.1 and Insulation 3.1 are all printed twice.

The mounting of the connectors and the capacitors was done by re-flow soldering at the University of Oslo, whereas FElixes and AMUXes were glued with conducting glue and bonded on to 4 hybrids at CERN. The bond map for this is shown in figure 3.9.

Print no.	Screen name	Via dimension
1	Layer 1* (power plane)	
2	Insulation 1.1	300μm x 300μm
3	Insulation 1.1	300μm x 300μm
4	Viafill 1.1*	300μm x 300μm
5	Insulation 1.2	400μm x 400μm
6	Viafill 1.2*	400μm x 400μm
7	Layer 2* (bottom route)	400μm x 400μm
8	Insulation 2.1	300μm x 300μm
9	Insulation 2.1	300μm x 300μm
10	viafill 2.1*	300μm x 300μm
11	Insulation 2.2	400μm x 400μm
12	Viafill 2.2*	400μm x 400μm
13	Layer 3* (ground plane)	400μm x 400μm
14	Insulation 3.1	300μm x 300μm
15	Insulation 3.1	300μm x 300μm
16	Viafill 3.1*	300μm x 300μm
17	Insulation 3.2	400μm x 400μm
18	Viafill 3.2*	400μm x 400μm
19	Layer 4* (top route)	400μm x 400μm
20	Bond-pad-layer*	
21	Solder-stop-layer**	

Table 3.4: The different layers printed for the test hybrid.

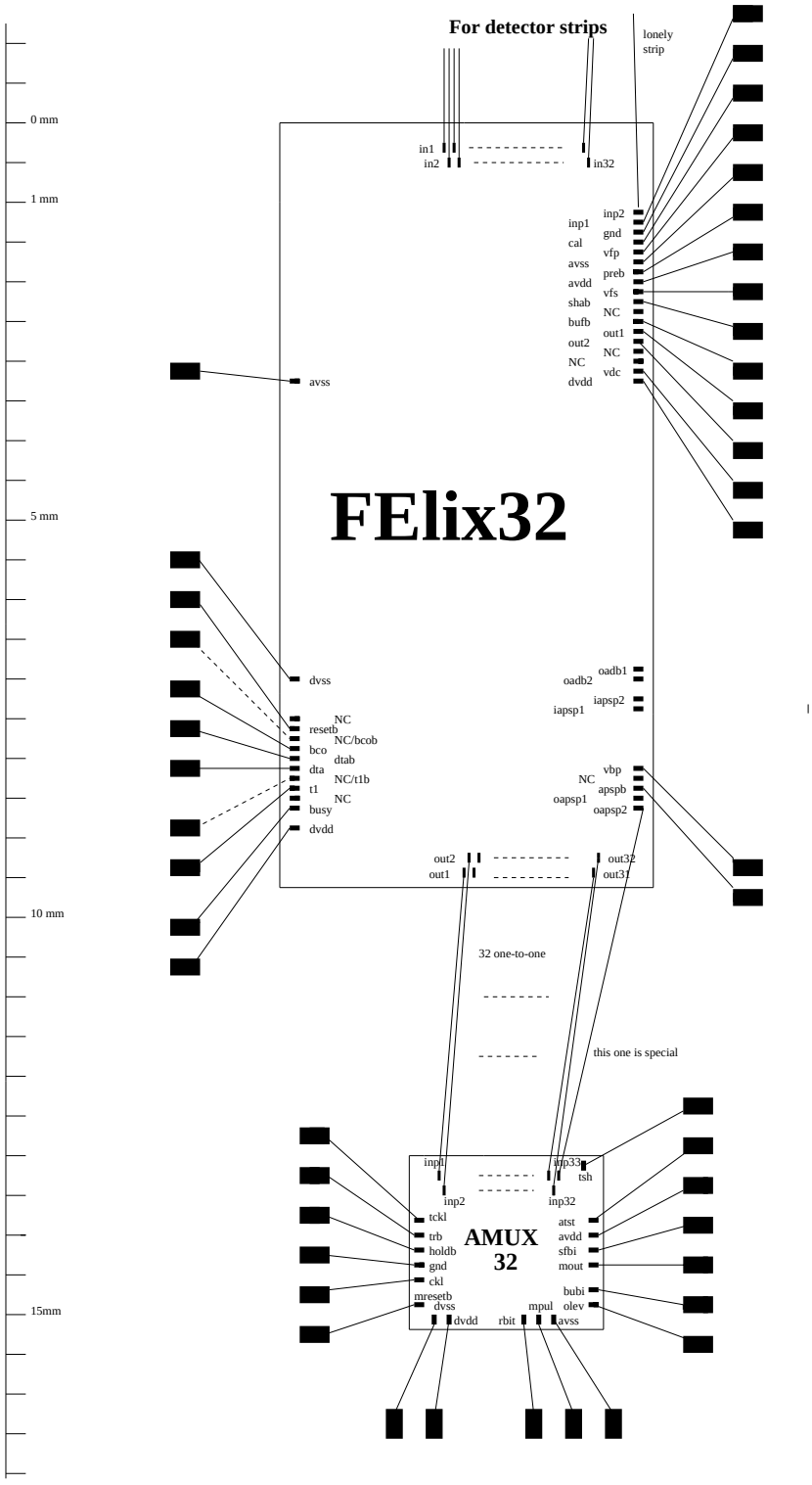

Figure 3.9: The bond map for the test hybrid.

3.3 Description of the test setup for the test hybrid

Two of the hybrids with the FElixes with the new digital logic were bonded directly to detectors. This is CSEM detectors. The strip pitch is 25 μm, whereas a 50 μm read-out pitch (every other strip) is used. The detector size is 3 cm $\times$ 6 cm, where the strip length is 6 cm. The thickness of this detector is 350 μm.

Two other hybrids with FElixes with the old digital logic, were glued to a small 2 cm $\times$ 2 cm PCB. One channel on each FElix was bonded to this board. Via this board a charge equivalent to that of a minimum ionizing particle, MIP, could be injected. This is achieved by sending a 2 mV step through a 1.8 pF capacitor. This gives a charge injection of $\Delta q = C\Delta V = 1.8\,\mathrm{pF} \cdot 2\,\mathrm{mV} = 3.6\,\mathrm{fC} = 22000\,\mathrm{e}^-$, which is the same as the charge released by a MIP passing through a 300 μm thick silicon detector.

A large printed circuit board (PCB) was connected to the hybrid by short kapton cables, about 2 cm long. This support PCB sets up the hybrid biasing (for the FElixes and the AMUXes) and delivers all the control signals like the trigger and the BCO-clock. The output signals of the hybrid are to weak to drive a long line, so they are amplified on the PCB, before they are put on a cable, which in the test setup is terminated in an oscilloscope. For a real test beam setup the analog output is sent to a SIROCCO module in a VME-crate. The SIROCCO module is a fast ADC, which can run with a frequency of up to approximately 18 MHz.

The digital signals are provided by a sequencer, a VME module called SEQSI [15], constructed at RAL. This sequencer is loaded with a bit pattern corresponding to the desired digital signals. The bit-patterns are output as ECL-levels when the module receives a trigger. It is in reality an advanced programmable pulse generator.

Since the 32 channel versions of the FElix and AMUX can not use ECL-levels for the digital signals, a level shifter has been made. ECL-levels are translated to logic levels close to +2 V (logic one) and -2 V (logic zero), proper levels for a CMOS chip powered at ± 2 V. The FElix can tolerate less swing than ± 2 V, probably down to ± 0.5 V, but then the noise requirements are difficult. A ± 2 V is therefore used to ensure good noise margins on the logic levels.

The major parts of the test setup are:

- The box, which is made at the mechanical workshop at the Physics Institute, and contains:
  - The test hybrid with FElixes and AMUXes and small PCB for charge injection.
  - Support PCB for providing digital control, analog input and read-out of the hybrid.
- Level shifter board for digital signals.
- The SEQSI-module and the rest of the VME-system.

The different items of this list will now be described. The hybrid and the PCB sitting in the same box, will be discussed together.

3.3.1 Hybrid and PCB in the test setup

The schematics of both the hybrid and the PCB are shown in figure 3.10. Layout plots showing just the component names and their placement are given in figure 3.8 and figure 3.11 for the hybrid and PCB, respectively. The PCB was laid out as a simple two layer PCB. The top and bottom layers are shown in figure 3.12 and figure 3.13. The figures, in scale one-to-one, were sent to a photo-plotter and the PCB was etched, drilled and mounted with components.

The little PCB for charge injection into one channel of each of the two FElixes on the hybrid, is glued to the hybrid. The signal arriving over the lemo cable is terminated to ground and led through a 1.8 pF capacitor before it is bonded over to a FElix. A lemo cable is a coaxial cable with a characteristic impedance of 50 Ω. One need separate cables for the two FElixes. The circuit on the PCB is just a copy of how the INP1 is implemented. In both cases a charge is injected into the pre-amplifier. But for the little PCB it is into a full channel, ending up in the AMUX, while for the INP1 it is only to a broken channel.

In the test setup the hybrid and the PCB is placed within the same box, as shown in figure 3.14. The hybrid which lies on top of the PCB, can be protected by a light proof metal cover put on top. There are rubber packings around this cover where the kapton cables can come out. The cover encloses the hybrid into a light proof inner box. The roof of this cover is a thin metal foil, which particles can pass through in case of a radioactive source setup with detectors mounted to the hybrid.

The hybrid is in reality consisting of two separate sets, each consisting of a FElix and an analog MUX to read it out. Since these two sets have biasing, digital control and analog inputs hooked up to the same lines, it is impossible to provide one set with signals that the other will not have.

The connectors on the hybrid, named CON1 to CON4 in the schematic, are the Dupont connectors leading to the PCB via the kapton cables. On the PCB schematic these connectors have the same names, so it is easy to compare the schematics.

The 12 pin connector CON2 provides the hybrid with the supply voltages and ground. The supply voltages DVSS and DVDD are −2 V and +2 V respectively. These two powers the digital parts of the FElixes and AMUXes. AVSS and AVDD have the same function for the analog part. On the PCB the supply voltages AVDD and DVDD are both made from a single +2 V entering the PCB on connector CON6 (placed in the lower left corner of both the schematic and the layout). The +2 V is split and each branch is filtered by RF-drossels (LD1 and LD2) and decoupled to ground. The AVSS and DVSS is generated in the same way. The −2 V is also split into a third branch, filtered in the same way. This voltage is used to terminate the digital control signals entering the PCB on connector CN7 from the level shifter.

The CON4 is for the detector part. This part is completely separate on the hybrid. The tracks for the detector powering ends up in the 3 big bonding pads and the long strip on the upper edge of the hybrid. This is seen from Layer 4 in figure 3.7. The strip is for the detector backplane, which makes it possible to glue the detector with conducting glue to it. The three pads are to bond over the BIAS, GATE and GROUND (guard) for

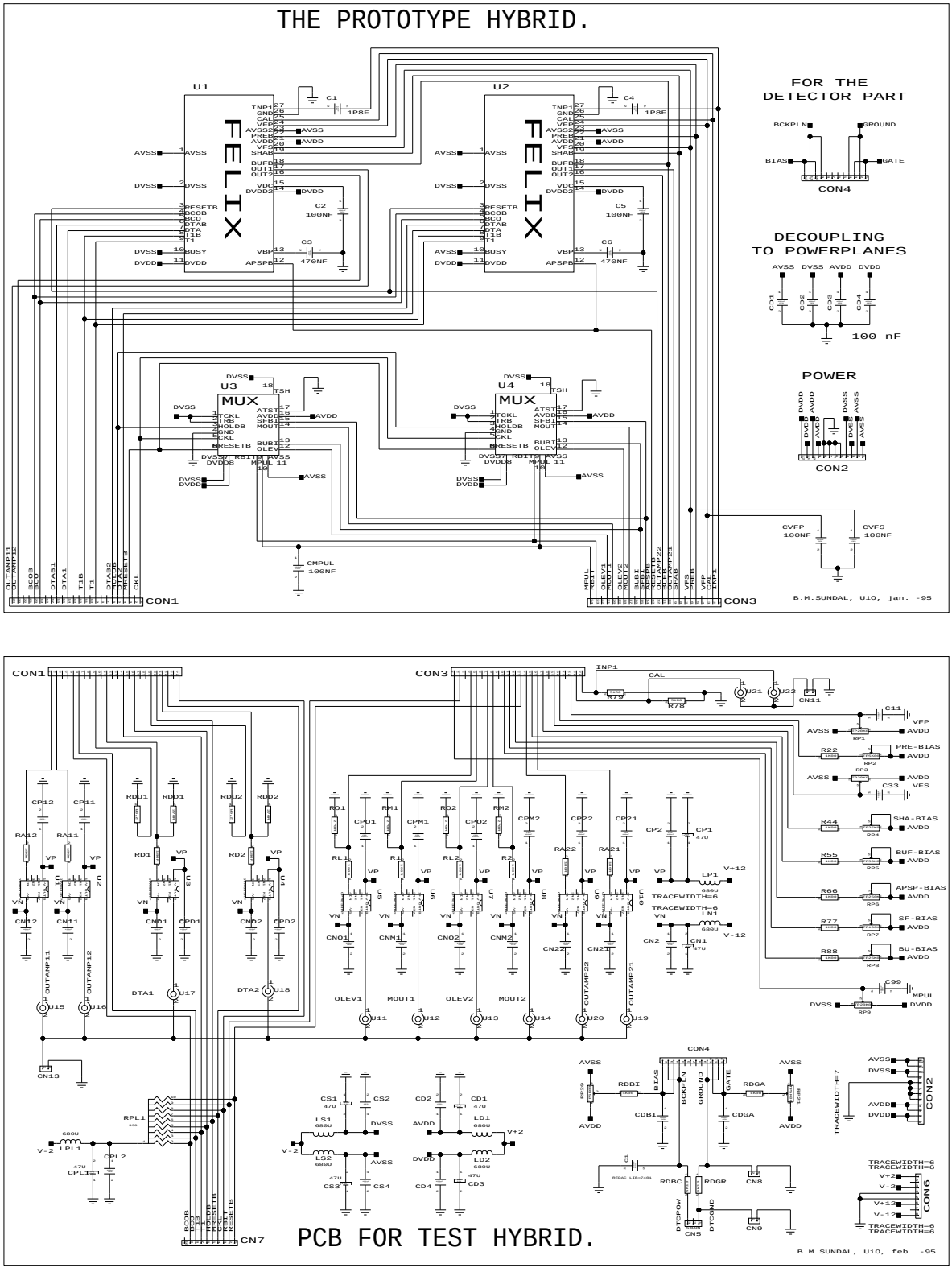

Figure 3.10: Schematic for the test hybrid and the support PCB.

Figure 3.11: Component names and placement for the support PCB.

Figure 3.12: Layout of the top layer of the support PCB.

Figure 3.13: Layout of the bottom layer of the support PCB.

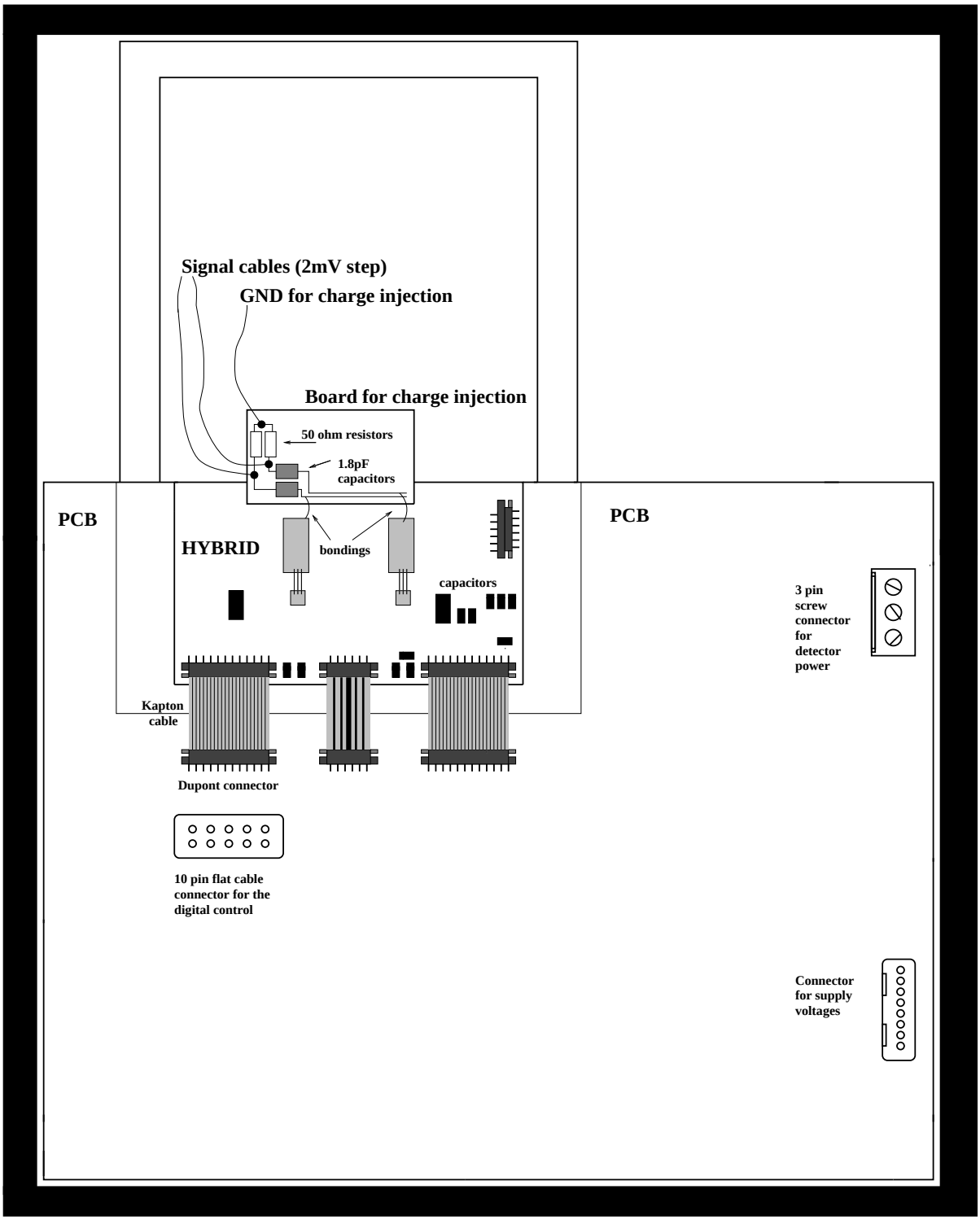

Figure 3.14: The box for the hybrid and PCB test setup.

the detector. On the PCB the GATE and BIAS are set up by potentiometers to voltages between AVSS and AVDD. The backplane voltage, BCKPLN, and the GROUND (guard) for the detector need to be provided to the PCB via the three pin screw connector CN5.

On the CON1 most of the digital controls for the FElixes and AMUXes enter the hybrid, on the PCB they are pulled to $-2\,\mathrm{V}$ as a means of terminating the signals from the flat cable they arrive at. This procedure reduces distortion of the signals.

All the biasing for the FElixes and AMUXes are provided over CON3. The voltages are set up on the PCB by tapping a potentiometer on the mid-tap. The voltages, VFS and VFP, but not MPUL, are generated in this way by putting the ends of the potentiometer at AVSS and AVDD. For MPUL the potentiometer ends are at DVSS and DVDD. By turning the pot-meter a voltage in the range $-2\,\mathrm{V}$ to $+2\,\mathrm{V}$ can be set up. The analog supply voltages are used to generate VFS and VFP, because internally in the chips these voltages are provided to the analog parts. VFS is internally in the FElix applied to the gate of a MOSFET-transistor coupled like a resistor. The two legs of the resistor are the source and drain of the MOSFET, and by varying the voltage VFS on the gate, one can alter the resistor value. The VFS controls a resistor, which is the feedback resistor in the shaper. The VFP controls the feedback resistor in the pre-amplifier. The MPUL controls resistors, too, these are the pull-up resistors for the digital control signals entering the AMUX. This voltage was therefore generated from DVSS and DVDD.

The currents, all of them supposed to flow into the FElixes and AMUXes are generated by connecting the chip pad to AVDD via a variable resistor. By altering the resistance one can control the amount of current flowing into the chip. Internally to the chip the current is used in the reference branch of a multiple current mirror, which mirror the current to all channels. The mirror image currents flow from AVDD and GND to AVSS.

For testing of the broken channels, one can use the INP1. One needs to provide the PCB with a voltage step of $2\,\mathrm{mV}$ to lemo connector U21. Since this signal arrives over a lemo cable it is terminated on the PCB in a $50\,\Omega$ resistor. On the hybrid this voltage step ends in two $1.8\,\mathrm{pF}$ capacitors, one for each FElix. On the other end of the capacitor there will be a very fast current pulse, very much like the current pulse from a detector. Only broken channel 1 on each FElix is bonded to this signal, as seen from the schematic and figure 3.9. To see the response this signal gives in the pre-amp/shaper on the two FElixes one needs to look at the output of the pre-amp/shaper. The output is the pin called OUT1 on the FElix symbol in the schematic. The output for FElix U1 (schematic) is on the track OUTAMP11, and for FElix U2 it is the track OUTAMP21. The first digit in the signal names indicate the FElix number, and the second, which of the two broken channels on that specific FElix.

From the PCB it is seen that the outputs of the broken channels are sent through line drivers and out on lemo connectors named U15 and U19 for OUTAMP11 and OUTAMP21 respectively. The line drivers are of the type OPA633 from Burr-Brown. These are typical coaxial cable drivers. With the jumper CN13 one can choose to ground the lemo housings to ground on the PCB or not. If not, there need to be some kind of other ground connection between the PCB and the oscilloscope.

Another test input is the CAL. The signal is provided much like INP1 to the PCB on

the lemo connector, named U21 in the PCB schematic. It is a voltage step of 0.064 V for 1 MIP. Internally in the FElix it goes to separate capacitors (56 fF) for each channel of the FElix. In this way one can inject a charge in every channel of the FElix. The principle is the same as for INP1, but the capacitors are internal to the FElix instead of external. The voltage step needs to be bigger since the capacitor value is smaller.

For both FElixes the DTA and DTAB are brought out. These signals tell us if the digital logic is functioning when the sequence is running. These signals were described in the FElix subsection. The DTABs are brought out close to the DTA tracks, as a means of reducing the pickup noise on other signals of the fast edges of the DTA signal. On the outside both DTAs and DTABs are pulled up to ground by 270 Ω resistors, since these signals are of the open drain (collector) type. Only the DTA version are then sent through line drivers (OPA633).

The real analog outputs from the AMUX are differential. The reference channel (OLEV) and the real output (MOUT) are very much the same, as seen in figure 3.3. When the AMUX clock (CKL) runs, the analog AMUX outputs sequentially the values it has sampled from the 32 FElix outputs. The reference channel input of the AMUX is in our case bonded to the output of the APSP-stage of broken channel 2 on the FElix.

From both AMUXes the MOUT and OLEV are terminated to ground with 270 Ω resistors on the PCB, and the voltage on top of this resistor are driven out of the PCB by OPA633 line drivers.

3.3.2 Level shifting

The outputs of the sequencer are standard differential ECL signals, logic high and low are -0.9 V and -1.74 V.

Since the test hybrid has CMOS-chips powered at 2 V and -2 V, the voltages representing logic high and low should be near 2 V and -2 V to assure that the chips will work properly.

A level shifter from ECL to CMOS has been made, by using 26C32 differential line receivers and 26C31 differential line drivers. The schematic specifies 26LS32 instead of 26C32, since the component library only had the LS-versions. Pin layout for these two versions are of course the same. The reason for going back to differential signals, is that the trigger signal is wanted differential. And for the reason of having the same time delay on all digital signals, all are converted to differential, though only one is used. The idea of using these chips as level shifters was developed at CERN [14].

The receivers can handle an input signal with a common mode of ± 7 V and a differential voltage in the area of ± 0.2 V with a hysteresis of around 0.1 V. These CMOS drivers and receivers have data-sheets specifying their operation when the supply is in the range 4.5 V to 5.5 V. They have been tested with a supply voltage of 4 V without any degradation of chip performance.

The ECL-input has a common mode of $(-0.9 - 1.74)\,\mathrm{V}/2 = -1.32\mathrm{V}$ and a differential voltage of $(-0.9 - (-1.74))\mathrm{V}/2 = 0.42$, which is well within the receiver specifications.

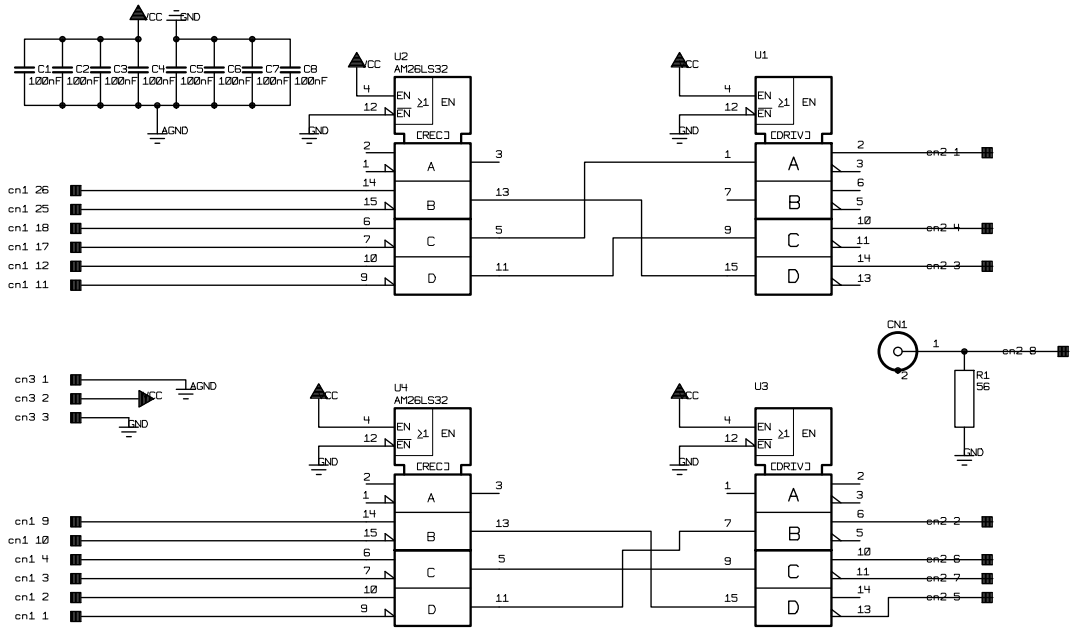

Figure 3.15: The schematic for the level shifter.

When the output is sent over a flat cable to the support PCB and terminated with 330 Ω resistors, the logic levels are about +1.2 V for logic one and close to −2.0 V for logic zero.

The schematic for the level shifter is shown in figure 3.15, and the PCB layout in figure 3.16. The latter figure is in scale one-to-one. The schematic and layout are both made in VISULA, a PCB schematic and layout tool from former Recal-Redac. The layout was sent to a photo plotter, and the PCB was then produced at the University of Oslo.

The BCO-clock is the only digital signal not sent through the 26C31 and 26C32, mainly because this 40 MHz clock is too fast to be handled by these receivers and drivers. The ad hoc solution is to provide the BCO on a lemo cable to the level shifter board. Here it is terminated in 50 Ω before sent on to the PCB and hybrid. In the NIM-crate a bipolar amplifier module is used to amplify the NIM-level BCO-clock and move it to a DC-level around ground level. This is not optimal since both on the PCB and the hybrid parallel tracks are used such that both BCO and BCOB can be provided.

Figure 3.17 shows the placement of the different signals on the input and output connectors for the test setup. The component list is found in table 3.5, and for the placement of the components, see figure 3.18.

3.3.3 SEQSI, the sequencer VME-module

As already mentioned, the sequencer is designed at the Rutherford-Appleton Laboratories [15] in the UK. The acronym stands for the SEQuencer for use in Silicon read-out Investigation.

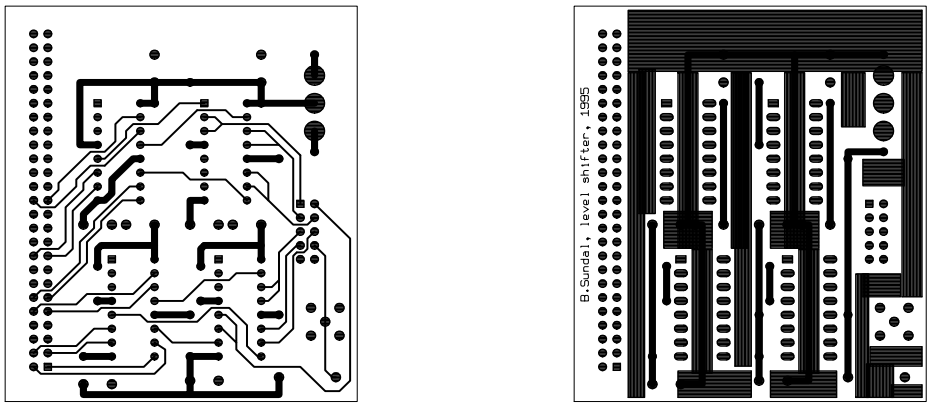

Figure 3.16: The PCB layout for the level shifter.

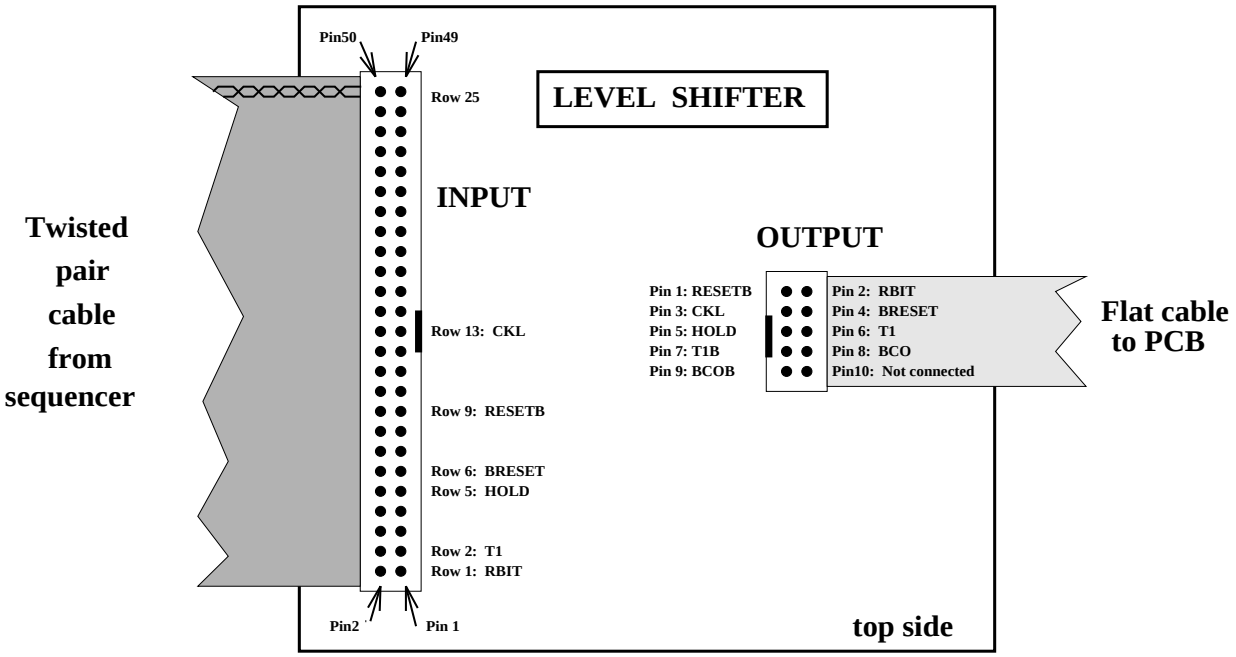

Figure 3.17: Placement of signals on the connectors of the level shifter.

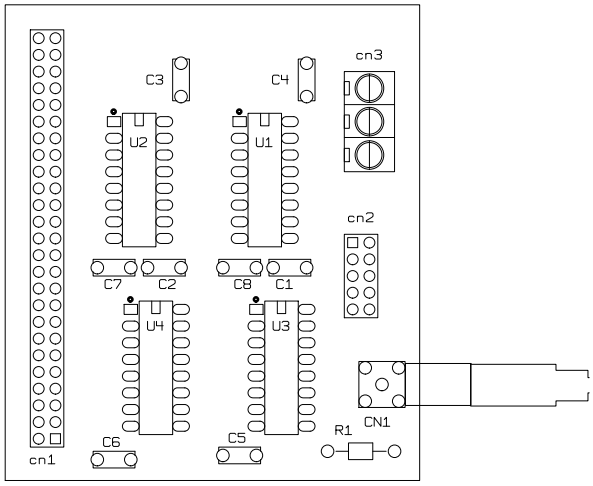

Figure 3.18: Placement of components on the level shifter.

Comp.	Part type	Description
C1	100nF	100V X7R Mlayer Ceramic 10%
C2	100nF	100V X7R Mlayer Ceramic 10%
C3	100nF	100V X7R Mlayer Ceramic 10%
C4	100nF	100V X7R Mlayer Ceramic 10%
C5	100nF	100V X7R Mlayer Ceramic 10%
C6	100nF	100V X7R Mlayer Ceramic 10%
C7	100nF	100V X7R Mlayer Ceramic 10%
C8	100nF	100V X7R Mlayer Ceramic 10%
CN1	LEMO-00	LEMO size 00 pcb mounted socket
R1	56	56R TR5 Metal Oxide Film 2%
U1	DS26C31	Quad diff. line drivers
U2	DS26C32	Quad diff. line receivers
U3	DS26C31	Quad diff. line drivers
U4	DS26C32	Quad diff. line receivers
cn1	DILH50	50 pin DIL header
cn2	DILH10	10 pin DIL header
cn3	TBLOCK3	3 way screw connecter block

Table 3.5: Component list for the level shifter.

The sequencer has a 64 kilobit deep and 32 bit wide memory. The bit pattern one would like to send out is loaded sequentially into the memory. Twenty of these 32 bits are easily programmed. Four of these have small programmable delays (maximum seven times 2 ns).

The sequencer front panel is shown in figure 3.19. The important connectors are the 50 pin flat-cable connector on the bottom, and the four lemo connectors B29, B30, TRIG and BCO on the top.

The 20 easily programmed signals are on the lower part of the 50 pin output connector. Each signal is output as differential ECL, numbered from the bottom. Be aware that the numbering of bits in the sequencer (like B29) corresponds to a numbering from 0 to 31. On the output connector (rows counted from bottom) or in the defining file (columns counted from left), numbering is started at 1.

The next uppermost row is the BCO-clock (always 40 MHz in our case) in ECL-levels. This clock can have a programmable delay of maximum seven steps of 2 ns each. The three rows underneath are also BCO-clocks. These three can be delayed together, with a different delay from the BCO in the next uppermost row.

The four lemo connectors on the top of the panel is as follows. The BCO, is the BCO clock output as NIM-levels. The TRIG is a NIM input. When the sequencer receives a TRIG it starts to output the sequence in memory at a rate of the BCO-clock. When it has finished the sequence, it runs an idle sequence until it receives the next trigger. The B29 and B30 are two more easily programmed outputs, in addition to the other 20. But these are only output as NIM-levels and not as ECL on the bottom connector at all.

A C-program called `start_seq` is made, which will read a file defining the sequence one wants to output and download it to the sequencer module. The file format is the only part kept from earlier times [16]. The program is found in Appendix A. An example of a file is shown in figure 3.20. As mentioned is the 20 first columns the signals output on the bottom 20 rows of the output connector on the sequence. In addition are the columns 30 and 31 (bits 29 and 30) defining the outputs on the lemo connectors B29 and B30.

One could imagine a file with only lines of zeros and ones, but in order to reduce the file size, one has extra lines of control text. The first line defines how many distinct blocks the sequence consists of. On the next line the first block is defined. The offset is how many lines one has so far. The length divided by the width says how many times one want to repeat the block underneath. The width says how many lines that are in the block. In figure 3.20 the second line says that the first data line (11000000000000000000000000000000) is to be repeated 20 times. Further down in the file one has a big block with a width of 20 and a length of 640. That means that the 20 lines below (the block) are going to be repeated $640/20 = 32$ times. This is in fact the block where the AMUX runs 32 cycles at 2 MHz in this sequence.

Since files like this are easy to understand, but not very easily made or visualized without a great deal of work, two more C-programs have been made to help this. The programs are listed in appendix A.

In the program `seq_tools`, made specific for testing of the test hybrid, one can do the following.

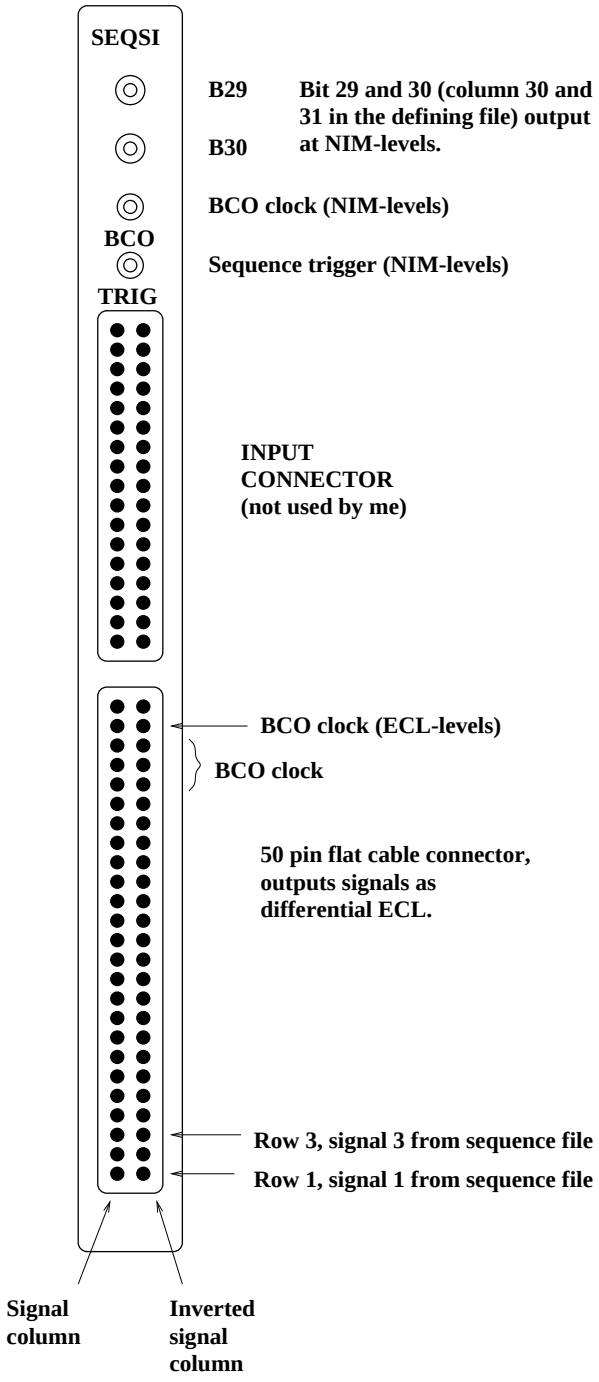

Figure 3.19: Front view of the SEQSI VME-module.

```
blocks= 14
offset= 0 length= 20 width= 1
11000000000000000000000000000000
offset= 20 length= 12 width= 1
11100000000000000000000000000000
offset= 32 length= 160 width= 1
11000000000000000000000000000000
offset= 192 length= 12 width= 1
10000000000000000000000000000000
offset= 204 length= 150 width= 1
11000000000000000000000000000000
offset= 354 length= 10 width= 1
11000000000100000000000000000000
offset= 364 length= 640 width=20
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000010000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
11000000000100000000000000000000
offset= 1004 length= 20 width= 1
11000000000100000000000000000000
offset= 1024 length= 20 width= 1
11000000000000000000000000000000
offset= 1044 length= 16 width= 1
11000100000000000000000000000000
offset= 1060 length= 40 width= 1
11000000000000000000000000000000
offset= 1100 length= 20 width= 1
01000000000000000000000000000000
offset= 1120 length= 20 width= 1
01000010000000000000000000000000
offset= 1140 length= 100 width= 1
11000000000000000000000000000000
```

Figure 3.20: An example of a sequence file.

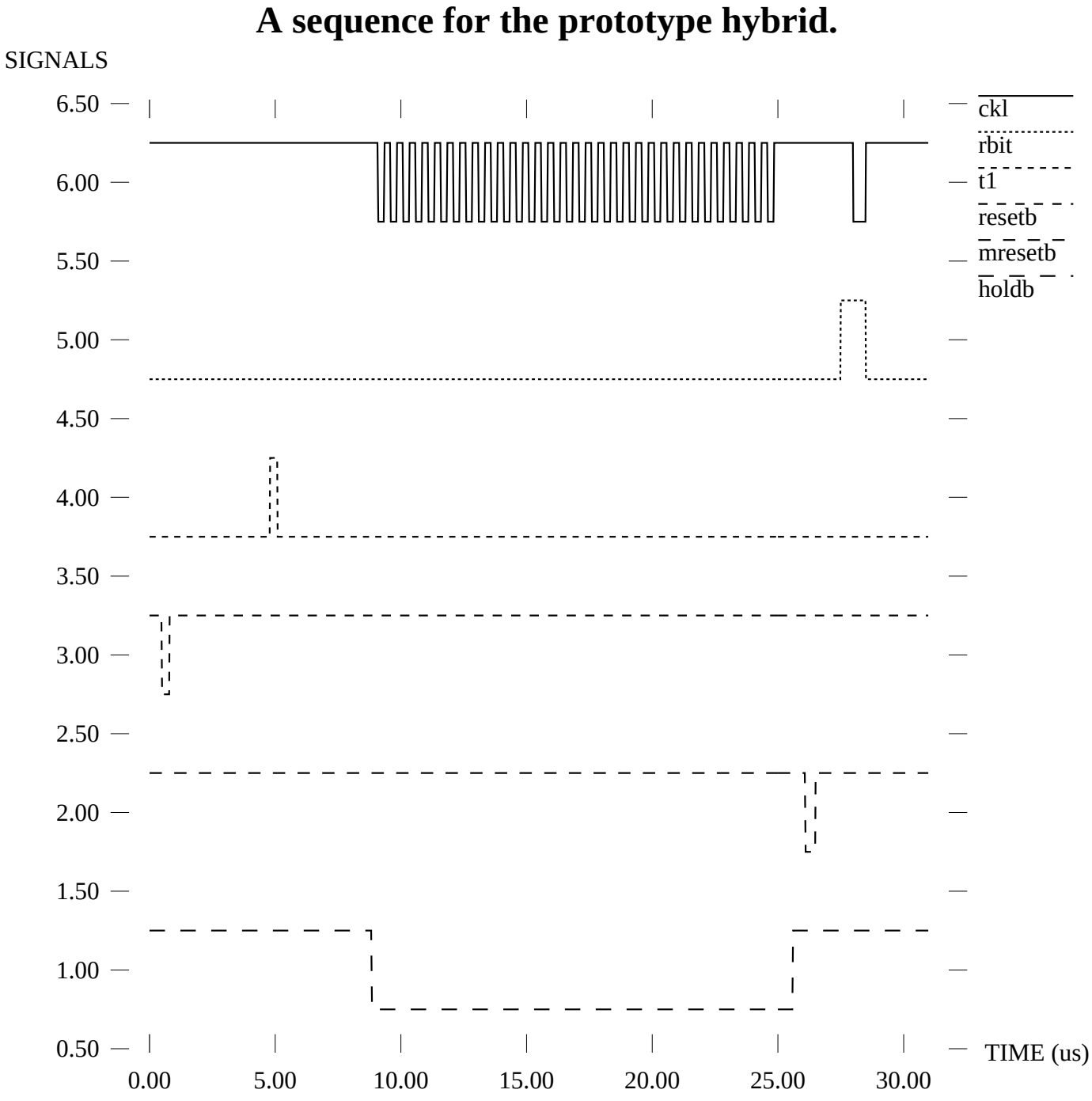

Figure 3.21: A sequence for the test hybrid, as presented by xgraph.

- Make a sequence for the read-out of the test hybrid, by answering a set of easy questions about the sequence. The program will then make a sequence file in the format discussed above. Upon running start_seq and specify this file, it will be downloaded to the sequencer. The program dumps the sequence in another file, too, which it calls xgraph.dat. This file can be read by the program xgraph, which is a program for drawing graphs. This program is not implemented in the VME-system, and the xgraph.dat file must be moved to an Unix system to get a drawing of the sequence.

- Read a sequence of the format above, and make a xgraph.dat file that can be understood by xgraph. As above, this can be done on the VME-system, but since xgraph does not exist there, one anyway needs to take the data file over to a Unix system to view the drawing of the sequence.

A drawing of the sequence made by xgraph of the sequence in figure 3.20 is shown in figure 3.21. This is a perfectly good sequence to read-out the test hybrid.

To alter where the different signals end up on the output connector of the sequencer, one needs only to alter the six `define` statements in the beginning of the seq_tools.c program, and the character array `name` just below defining the signal names. Then one needs to recompile the program. The program shown in appendix A does not have the signals placed where the description of the level shifter in the earlier subsection should indicate. This is because another version of the level shifter has been made, which will be discussed later.

The program, `seq_visual`, is a more general program for visualizing sequences. This program will run on a UNIX-system. See appendix A for information.

Since the output on the 50 pin connector is differential one needs to specify where the signal comes out, and where the inverted signal comes out. In each row on the connector, the signal seen from the drawing made by xgraph is on the left. The pin on the right is the inverted signal. The sequence file shows just the opposite.

3.4 Setup for initial testing of the test hybrid

A drawing of the test setup is found in figure 3.22. It shows how all the parts are interconnected. This setup reads out 32 channels of the FElix by means of the AMUX. Since the little PCB for charge injection is only bonded to one channel on each AMUX, the read-out will give a AMUX output which is relatively flat (some pedestals), except for the channel were the charge is injected. This, of course, if everything works as it should.

To make some initial testing, the full setup is not needed. A good start is to check the two broken channels connected to the INP1. One can inject a 2 mV step and see if the output of the pre-amp/shaper (OUTAMP11 and OUTAMP21) has the right shape, which is of the form $\frac{t}{\tau}e^{-t/\tau}$. When performing this test, the level shifter (digital signals) can be de-connected from the PCB to reduce noise.

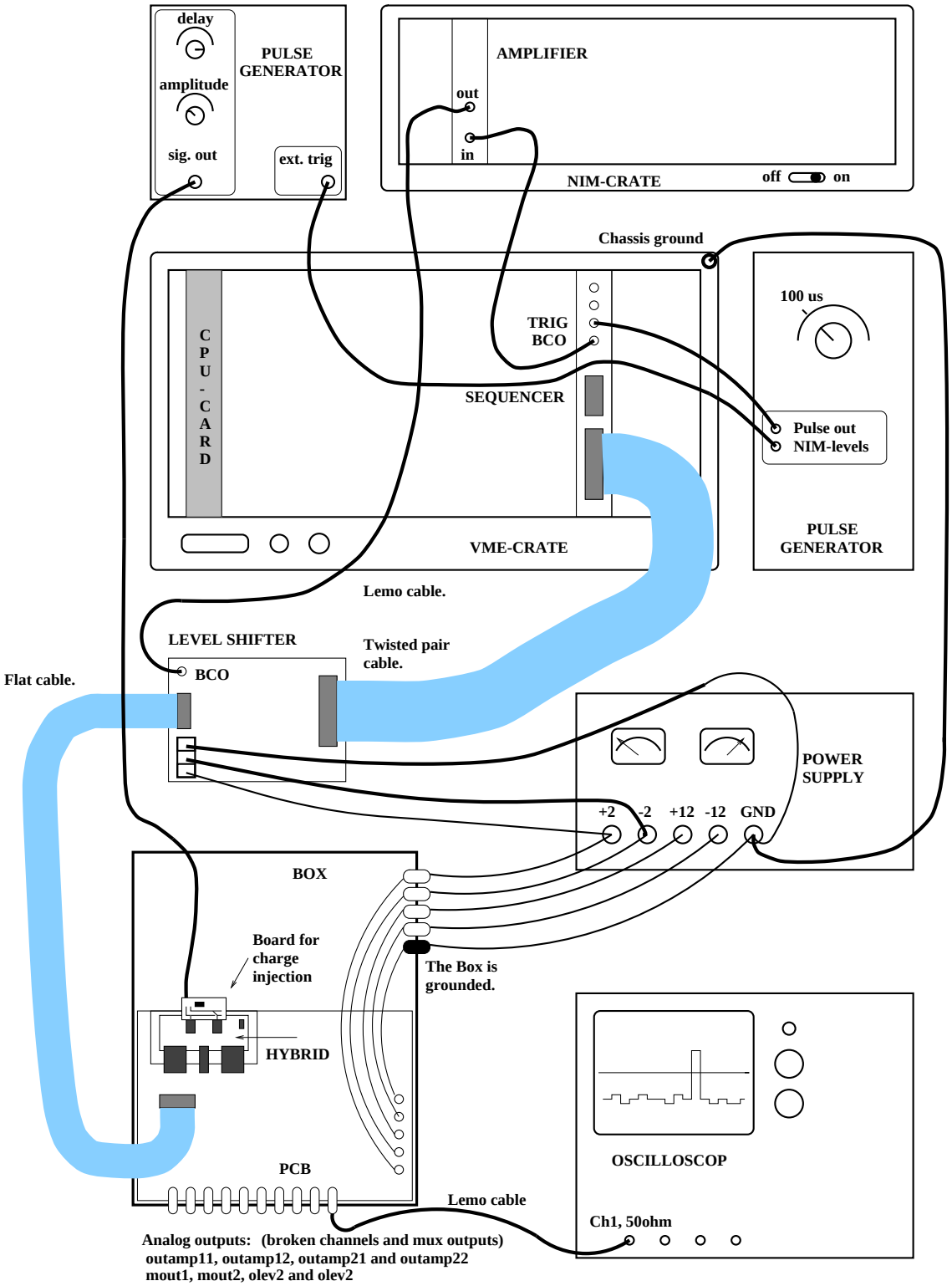

Figure 3.22: The test setup for the test hybrid.

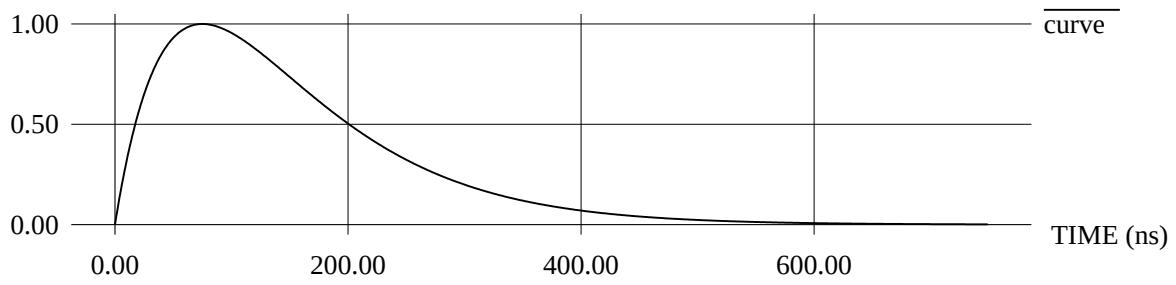

Figure 3.23: The ideal pulse shape from the pre-amp/shaper in the FElix.

This ideal pulse shape is plotted in figure 3.23, with a time constant of 75 ns and the y-axis normalized to 1.

The shape of the pulse is determined by the biases VFS, VFP, PREB, SHAB and BUFB, where VFS and PREB/SHAB in particular are important. All these biases are connected to the pre-amp/shaper, with BUFB being the current for the output buffer of the pre-amp/shaper that feeds the input of the ADB. The amplifiers both in the pre-amplifier and the shaper are actually of the same type. The pre-amplifier (integrator) is controlled by VFP and PREB and the shaper by VFS and SHAB. The nominal values found by simulations and then later adjusted by measurements at CERN, are found in table 3.1 and table 3.2 in the previous subsections.

When using only the pre-amp (the broken channel), the signal does not necessarily looks like the real thing going into the ADB. This is of course because our long hybrid tracks give a much higher capacitive and resistive load to the pre-amp/shaper output than the ADB-inputs give the full channels. One should therefore not put too much work in getting a perfect waveform out of the broken channel.

The two next subsections describe the pre-amp/shaper and how the APSP processes the signal from the pre-amp/shaper.

3.4.1 The perfect output waveform from the pre-amp/shaper.

The δ-like current pulse from a detector (in the time domain) will have the form

$$I_{in}(s) = Q_0 \tag{3.1}$$

in the frequency domain. Here Q_0 is the charge released in the detector, typically 3.6 fC for a MIP. It might seem strange that the current I has the unit of charge (C) in the frequency domain, and not the unit of current (A). This is because the process of going from the time domain to the frequency domain involves a Laplace integral. This integral is over time, so the Laplace integral of $I(t)$ will give the $I(s)$ in unit of current multiplied by unit of time,

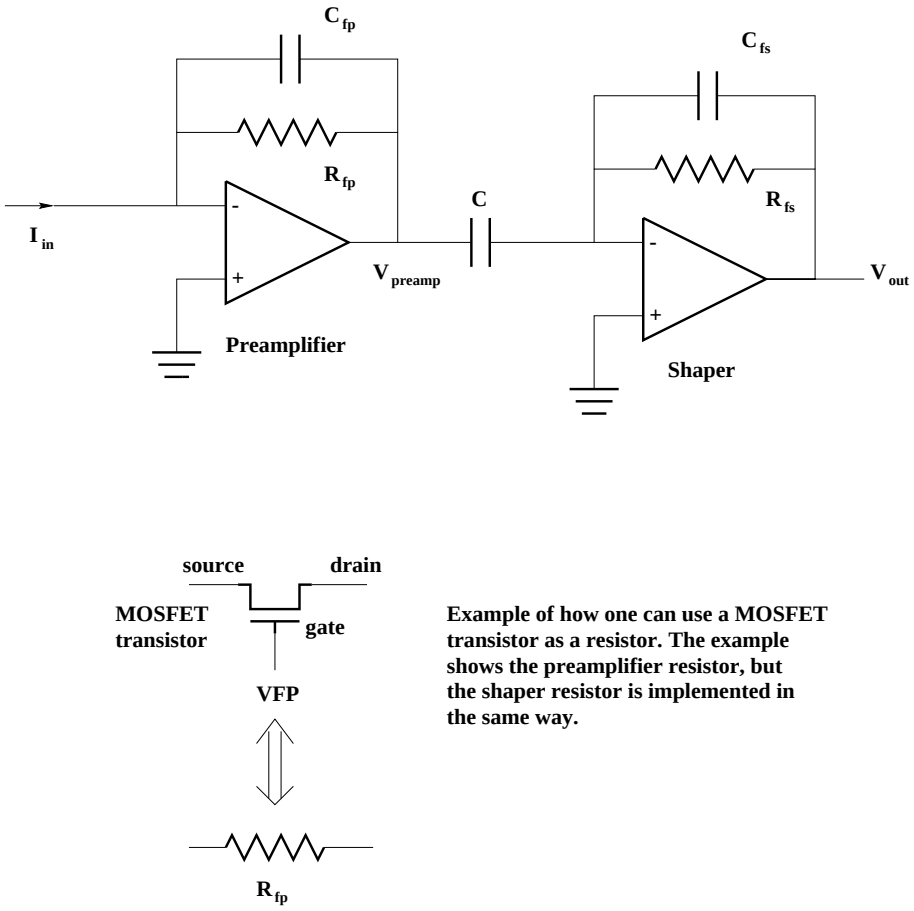

Figure 3.24: A schematic for the pre-amp/shaper using ideal amplifiers.

which is charge. An introductory text to network analysis by use of Laplace transforms can be found in [13].

The pre-amplifier is in fact an integrator, as shown in figure 3.24. In the frequency domain it has the (system) response

$$\frac{V_{preamp}(s)}{I_{in}(s)} = -\frac{R_{fp}}{1 + sR_{fp}C_{fp}} \tag{3.2}$$

The resistor R_{fp} is the one controlled by the voltage VFP, and C_{fp} is the integrating capacitor in the feedback loop. The variable s is the complex frequency variable. The resistor R_{fp} is very big, and only has the function of stabilizing the pre-amplifier by having a DC component in its feedback loop. At the frequencies the pre-amplifier is operating, we have that $sR_{fp}C_{fp} \gg 1$, and one can safely assume

$$\frac{V_{preamp}(s)}{I_{in}(s)} \approx -\frac{1}{sC_{fp}}, \tag{3.3}$$

which is the response of an ideal integrator. Our integrator or pre-amplifier will integrate

the current spike from the detector, to give the total charge, since the time integrate of a $\delta(t)$-function is a step function.

The shaper together with its input capacitance C, shown in figure 3.24, has a response

$$\frac{V_{out}(s)}{V_{preamp}(s)} = -\frac{R_{fs}Cs}{1+s\tau_{shaper}}, \tag{3.4}$$

where $\tau_{shaper} = R_{fs}C_{fs}$.

The multiplication of equation 3.3 with equation 3.4 gives the total system function for the pre-amp/shaper, which is

$$\frac{V_{out}(s)}{I_{in}(s)} \approx \frac{R_{fs}C}{C_{fp}} \cdot \frac{1}{1+s\tau_{shaper}}. \tag{3.5}$$

The amplifiers are not perfect, however. The gain is not infinite, and the amplifiers can not provide infinite currents. For example, the pre-amplifier output will rise exponentially towards the step value. By altering the currents PREB and SHAB in the pre-amplifier and shaper one can alter the effective upper limit bandwidth of the amplifiers. All amplifiers have a upper frequency where the gain starts to drop. If one calls the time constant attributed to this low-pass effect τ_{limit}, it adds a modifying factor $1/(1+s\tau_{limit})$ to the pre-amplifier/shaper response, which now will read

$$\frac{V_{out}(s)}{I_{in}(s)} \approx \frac{R_{fs}C}{C_{fp}} \cdot \frac{1}{(1+s\tau_{shaper})(1+s\tau_{limit})}. \tag{3.6}$$

One can now alter PREB, SHAB and VFS so that both τ_{preamp} and τ_{shaper} are 75 ns, that is $\tau = \tau_{limit} = \tau_{shaper} = 75$ ns. If we insert τ and eliminates R_{fs} by using $R_{fs} = \tau/C_{fs}$ the pre-amplifier/shaper response in equation 3.6 will read

$$\frac{V_{out}(s)}{I_{in}(s)} \approx \frac{C}{C_{fp}C_{fs}} \cdot \frac{\tau}{(1+s\tau)^2}. \tag{3.7}$$

If equation 3.1 is inserted for $I_{in}(s)$, the response of the pre-amplifier/shaper to a detector pulse will be given by

$$V_{out}(s) \approx \frac{Q_0 C}{C_{fp}C_{fs}} \cdot \frac{\tau}{(1+s\tau)^2}, \tag{3.8}$$

which by using the inverse Laplace transformation

$$\mathcal{L}^{-1}\left[\frac{\tau}{(1+\tau s)^2}\right] = \frac{t}{\tau}e^{-t/\tau} \tag{3.9}$$

gives the time domain response of

$$V_{out}(t) \approx \frac{Q_0 C}{C_{fp}C_{fs}} \cdot \frac{t}{\tau}e^{-t/\tau}, \tag{3.10}$$

which is the wanted response of the pre-amp shaper to a detector pulse.

There is another way to understand the waveform out of the pre-amp/shaper, in addition to using the broken channel output. The broken channel output could have some distortion problems as mentioned at the end of the previous section. The solution is to pick it up after the APSP for the full channels.

This can be done by putting the test setup in peak mode. Then the test input is moved in time and the amplitude of the interesting channel in the AMUX output is observed. By altering the delay of the test pulse one scans through the waveform from the pre-amp/shaper. If the test pulse is too early the APSP will pick the peak sample too late and one will get a value on the exponential decreasing part of the pre-amp/shaper waveform. If the test pulse is too late, the APSP logic when outputting the peak sample, will take a sample corresponding to the fast rising edge of the pre-amp/shaper waveform. If the test pulse is far too late the APSP logic will already have output its so called peak value already before its arrived and the amplitude will be zero. Since the exponentially falling edge of the pre-amp/shaper output is at an observable amplitude for around 15 BCO periods after the peak, there is a total window in time of $(15 \cdot 25 + 75)\,\mathrm{ns} = 450\,\mathrm{ns}$ where one can place the test pulse and still see something on the corresponding channel at the AMUX output.

There exists a package of Labview programs [17] for testing of the FElix chips. The timing scan mentioned above is made with a Labview program called **'Find pulse shape'**. This program controls both the oscilloscope and the pulse generator, which has a programmable delay, over a GPIB bus. The result of running this program is shown in figure 3.25. Since the delay is used along the time axis and the amplitude in peak mode in fact is negative, one need to turn the figure upside down to recognize the pulse shape out of the pre-amp/shaper. This pulse shape is not really ideal. One sees there is an undershoot (figure viewed upside down) on the end. This figure was made for a PCB with one FElix and one AMUX, and equipped with a detector. This particular PCB was installed in the test beam the day after this figure was made.

3.4.2 De-convolution using the APSP

The function $\frac{t}{\tau}e^{-t/\tau}$ rise fast, has its maximum at $t = \tau$, and then falls off exponentially. This shape has the feature that it can be de-convoluted using only three consecutive time samples, as it is done in the APSP. For our pre-amplifier/shaper the rise time is $\tau = 75\,\mathrm{ns}$, corresponding to three BCO periods.

If one normalizes this function to 1 at its maximum one gets,

$$h(t) = \begin{cases} \frac{t}{\tau}e^{-t/\tau+1} & \text{if } t \geq 0 \\ 0 & \text{if } t < 0 \end{cases} \tag{3.11}$$

The waveform is sampled at times $t = n\Delta t$, here $n \in \mathcal{Z}$, with sampling interval Δt.

Ideally one would like that a simple weighted sum of three consecutive samples is zero for all n, except for $n = 0$, where the weighted sum should be 1. This can be formulated

Figure 3.25: Pulse shape from pre-amp/shaper as measured by using the peak mode sample out of the APSP.

mathematically as,

$$\begin{array}{rcrcrcl} w_3h(t-\Delta t) & + & w_2h(t) & + & w_1h(t+\Delta t) & = & 0 \quad \text{if } t \neq 0 \\ w_3h(-\Delta t) & + & w_2h(0) & + & w_1h(\Delta t) & = & 1 \quad \text{if } t = 0. \end{array} \tag{3.12}$$

Since $h(t) = 0$ for $t \leq 0$ the last line gives $w_1h(\Delta t) = 1$. If one solves this equation for w_1 and introduces the variable $x = \Delta t/\tau$ one finds that

$$w_1 = e^{x-1}/x. \tag{3.13}$$

The first line of 3.12 can be rewritten in terms of n to read

$$w_3h(n\Delta t - \Delta t) + w_2h(n\Delta t) + w_1h(n\Delta t + \Delta t) = 0 \text{ for n} > 0. \tag{3.14}$$

Only $n > 0$ is considered in the following since the result is trivial for $n < 0$. By inserting the function $h(t)$ and using $x = \Delta t/\tau$, one gets

$$w_3(n-1)exe^{-(n-1)x} + w_2nexe^{-nx} + w_1(n+1)exe^{-(n+1)x} = 0, \tag{3.15}$$

which reduces to

$$w_3(n-1)e^x + w_2n + w_1(n+1)e^{-x} = 0, \tag{3.16}$$

by removal of the factor exe^{-nx}. This expression can be written as

$$n(w_1 + w_2 + w_3) + (w_1e^{-x} - w_3e^x) = 0, \tag{3.17}$$

which is a linear combination in n on the form $a \cdot n + b = 0$, where a and b are constants. The only way a linear combination in n can be zero for all $n > 0$ is if both a and b are zero, that is $w_1 + w_2 + w_3 = 0$ and $w_1e^{-x} - w_3e^x = 0$.

There are now three equations for the solution of the three weights. The system of equations is,

$$\begin{array}{rcrcrcl} w_1 & & & & & = & e^{x-1}/x \\ w_1 & + & w_2 & + & w_3 & = & 0 \\ e^{-x}w_1 & & & - & e^xw_3 & = & 0. \end{array} \tag{3.18}$$

The result is

$$w_1 = e^{x-1}/x \tag{3.19}$$

$$w_2 = -2e^{-1}/x \tag{3.20}$$

$$w_3 = e^{-x-1}/x \tag{3.21}$$

For $x = \Delta t/\tau = 25\,\text{ns}/75\,\text{ns} = 1/3$, which are the values used in the FElix, one has $w_1 \approx 1.540$, $w_2 \approx -2.207$ and $w_3 \approx 0.791$.

If the sampling of the pre-amp/shaper response misses a bit, for instance because the relative phase between the physical input signal and the BCO is wrong, the output from the APSP will not have the full amplitude (1 for $t = 0$, 0 for $t \neq 0$ for the expression of $h(t)$ used above).

The effect of sampling at the wrong time can be written with a new expression for the sampling time, which is $t = n\Delta t + f\Delta t$. Here f is the error in the position of the sampling measured as a fraction of one sampling interval Δt. How will now the de-convoluted sum,

$$w_3 h(t - \Delta t) + w_2 h(t) + w_3 h(t + \Delta t), \tag{3.22}$$

look for $n = 0$, which earlier gave the result 1?

If one samples the pre-amp/shaper waveform far too late or early, corresponding to missing by more than a sampling interval, $|f| \geq 1$, one finds that the expression 3.22 is zero. This is interesting, because in peak mode there is an observable output in a time window of about 450 ns around the perfect timing. But in de-convoluted mode a response from the APSP is found in a time window of 50 ns width ($|f| < 1 \Rightarrow \Delta t|f| < 25\,\text{ns}$) around the perfect timing.

If one samples a little too late, $1 > f > 0$ and $n = 0$, one will have that $h(t - \Delta t) = 0$ and the de-convoluted sum reduces to

$$w_2 h(f\Delta t) + w_3 h(f\Delta t + \Delta t) = (1 - f)e^{-fx}. \tag{3.23}$$

If one samples a little too early, $-1 < f < 0$ and $n = 0$, one has both that $h(t-\Delta t) = 0$ and $h(t) = 0$ and the sum reduces to

$$w_1 h(f\Delta t) = (1 + f)e^{-fx}. \tag{3.24}$$

The two equations 3.23 and 3.24 can be written as one equation, for the APSP-response amplitude as a function of f. This is a relative amplitude,

$$A(f) = (1 - |f|)e^{-fx}, \ -1 < f < 1. \tag{3.25}$$

This function is plotted in figure 3.27, for three values of x. In the FElix $x = 1/3$. The shape is near triangular, the amplitude of the APSP-response drops nearly linearly with the error in the sampling position.

It is now interesting to compare this figure to figure 3.26, which is a printing of the Labview program **'Find pulse shape'** [17], but this time for the FElix in de-convoluted mode. The time scale is too compressed, and since the time axis uses the delay of the physical pulse instead of the sampling time error, one really needs to see this figure in a mirror to compare it to figure 3.27 ($x = 1/3$). Nevertheless the agreement is good. One sees that the width of the time window where one can observe an APSP-response is close to 50 ns, and that the waveform is near triangular with one positive curvature slope and one negative curvature slope.

3.5 Setup for full testing of the test hybrid

The full test setup is shown in figure 3.22.

Figure 3.26: Amplitude of APSP-response for different timing.

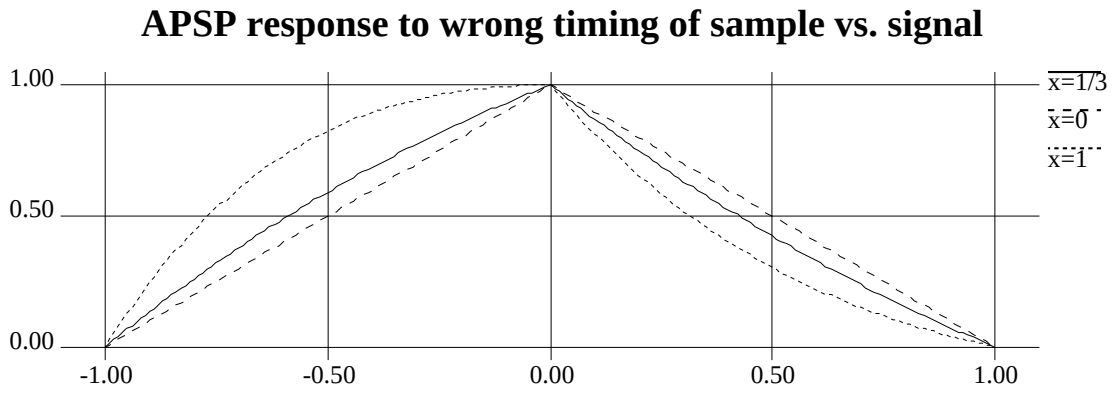

Figure 3.27: APSP response to wrong timing of the sampling relative to the input pulse

The setup works as follows. The pulse generator on the right makes a pulse every $100\,\mu$s, or at another suitable period. The pulse generator starts the sequencer, and it also triggers the pulse generator in the upper left corner of the figure.

The pulse generator in the upper left corner gives an output on a lemo cable after an adjustable delay. This output is scaled down to give either something around 2 mV for the charge injection board, or something around 0.1 V for the CAL.

The sequencer is started by the pulse from the first pulse generator. The sequencer outputs all the digital control signals, except the BCO, on a twisted pair flat cable, to the level shifter. The BCO is output from the sequencer as NIM levels. The BCO is sent to a bipolar amplifier, in a NIM module in the NIM-crate. This to give the possibility of changing the amplitude and DC-level of the BCO to around 0.6 V peak-to-peak around 0V DC-level. The BCO is then sent on over a new lemo cable and terminated in $50\,\Omega$ on the level shifter. Both BCO and the rest of the signals, which are shifted, are sent over a short flat cable to the PCB, where all lines are pulled to -2 V by $330\,\Omega$ resistors.

The critical part of making everything functioning is the timing. Two things need to be right:

- The T1 must appear a time after the test pulse, which is the same as the delay of the ADB. The ADB consists of 67 cells used for delay, and the BCO clocks the samples from one cell to the other. This gives a delay of $67 \cdot 25\,\text{ns} = 1.675\,\mu$s. Make sure to put RESETB for the FElix before the test pulse.

- The HOLDB (see for instance figure 3.21) must go low either in the middle (or late part) of the first or the second DTA. If it goes low in the first DTA, the AMUX is holding the peak value from the FElix, and if it goes low in the second DTA, the AMUX will hold the de-convoluted value.

If there is no BUSY (as in the test hybrid), there is a time of $4.775\,\mu$s between the rising edge of T1 until the falling edge of the last DTA. If one want to start holding at a time of $0.1\,\mu$s before the end of the DTA, one needs a delay of $(4.775 - 0.1)\,\mu\text{s} = 4.675\,\mu$s

from the start of the T1 until the HOLDB goes low to read-out the de-convoluted, and a time of $(4.775 - 0.1 - 0.55 - 0.2)\,\mu s = 3.925\,\mu s$ to read-out the peak value.

3.6 Problems and changes to the test setup

When turning on the test setup and checking the signals and voltage supplies, one major problem was observed. The 40 MHz BCO was present almost everywhere. If one measured on the connector pins on the hybrid, one could find the BCO signal with almost the same amplitude on both the BCO-pin and the ground pin. Most of the problem lay in the fact that the screen of the BCO lemo cable was not connected to ground on the level shifter, as can be seen in figure 3.15 of the level shifter schematic. Fixing this did not remove the problem fully. Two improvements were implemented:

- Reduce pickup and asymmetric drawing of current, which create spikes on the supply voltages, and provide BCO differential. A new level shifter was made with all signals kept differential as long as possible, including the BCO.
- A better strategy for how supply voltages are provided and decoupled. This requires changes to the PCB, by cutting tracks with a scalpel and soldering on extra components and wires. More pull-down resistors were used because all control signals now arrive at the PCB differential. BCO is special and requires pull up resistors.

These changes are described in the two following sub sections.

One could of course have totally redesigned the PCB but the mechanical setup would then have had to be changed. This was found to be too time consuming.

3.6.1 The new level shifter

As explained the problem with the level shifter is the fact that differential signals are generated but not sent over the flat cable to the PCB. The inverted signals should at least be terminated on the level shifter to a resistance similar to the one that the signals are terminated to on the PCB. Not having this termination lead to a lot of asymmetric drawing of currents, which gives spikes on the supplies. On the new level shifter all signals are sent differential to the PCB. In addition the terminating resistors on the PCB were too big. This distorted the edges of the digital signals. This time the signals will be terminated in 110Ω on the PCB, which is close to the characteristic impedance of a twisted pair cable.

Furthermore pickup was observed between the digital signals, probably caused both by the tightly routed level shifter and the flat cable leading to the PCB. This is easily solved by making the new level shifter a bit bigger, and by using a twisted pair flat cable instead of a flat cable.

As for the input side of the level shifters there are some changes. The signals are terminated to $-2\,V$ with a $110\,\Omega$ resistors. On the previous level shifter there were no resistors, but instead a ground connection between the level shifter and the sequencer, which now is superfluous.

The new level shifter will be put in a grounded aluminum box to reduce the noise.

For all other signals than the BCO the 26C32 and 26C31 receivers and drivers are used. Differential ECL versions of the BCO are output on the same 50 pin connector as the rest of the digital control signals, and not only as a NIM-signal on the lemo connector higher up on the front panel of the sequencer. The differential ECL-versions have a peak-to-peak range of about $-0.9-(-1.74))\,\mathrm{V} = 0.84\,\mathrm{V}$, which is sufficient if the DC-level is shifted up about 1.4 V. This is easy to do with two transistors each for BCO and BCOB, since 1.4 V is two base-emitter voltage drops.

A schematic drawn in Viewdraw made for simulation purposes of this BCO-shifter is shown in figure 3.28. One sees the circuitry for BCO (the BCOB circuitry is the same). The transistors are used as emitter followers. The transistors are always in their forward active region, which ensures fast reaction to input voltage changes. The circuit is powered at $\pm 2\,\mathrm{V}$ and a signal generator provides a 40 MHz clock at ECL-levels for the simulation. The circuit contains terminating resistors to place both on the level shifter and on the PCB. If the finished level shifter works only with the $110\,\Omega$ resistor on the PCB, the one on the level shifter can be removed, to reduce the current the circuit uses. The new level shifter shown later only has the terminating resistors on the PCB.

Figure 3.29 shows the transient simulation presented by Viewtrace after simulations done by Viewspice. One sees that the output (VO) is at suitable voltage levels around 0 V. Figure 3.30 shows the Bode plot of the same circuit. One see that the drop in amplification is insignificant up to 100 MHz, implying that the 2N3906 transistors used for the shifting easily can handle 40 MHz. Of course the output of this circuit will not necessarily have this ideal shape due to stray capacitance.

The schematic for the new level shifter is shown in figure 3.31. The components were mounted on a wiring board.

3.6.2 New supply and decoupling strategy

The new strategy for providing supply voltages is shown in figure 3.32. One declared **cold** ground point is used. This is the chassis of the PCB/hybrid box. From there a fat wire connects to the chassis of the level shifter box. Each box is connected to its inside circuitry with one ground wire.

From the power supply there goes a twisted pair from each floating voltage, to the banana plug holes on the PCB/hybrid box chassis. One of the wires goes into the corresponding voltage banana plug hole, whereas the other wire is grounded in the cold point.

What happens on most of the different supply and GND-branches on the PCB is shown in figure 3.33. The main filtering and decoupling of the different supply branches are done by a RF-drossel, an electrolytic capacitor of some μ-Farads and an ceramic capacitor of 100 nF. These are put close to the branching point whenever possible. When active components (OPAs) are put on the same branch, they have decoupling locally as seen from the figure. The branches for the terminating resistors are filtered and decoupled in the same way. The BCO and BCOB are terminated to the $+2\,\mathrm{V}$ branch and the rest of the digital control signals are terminated to the $-2\,\mathrm{V}$ branch.

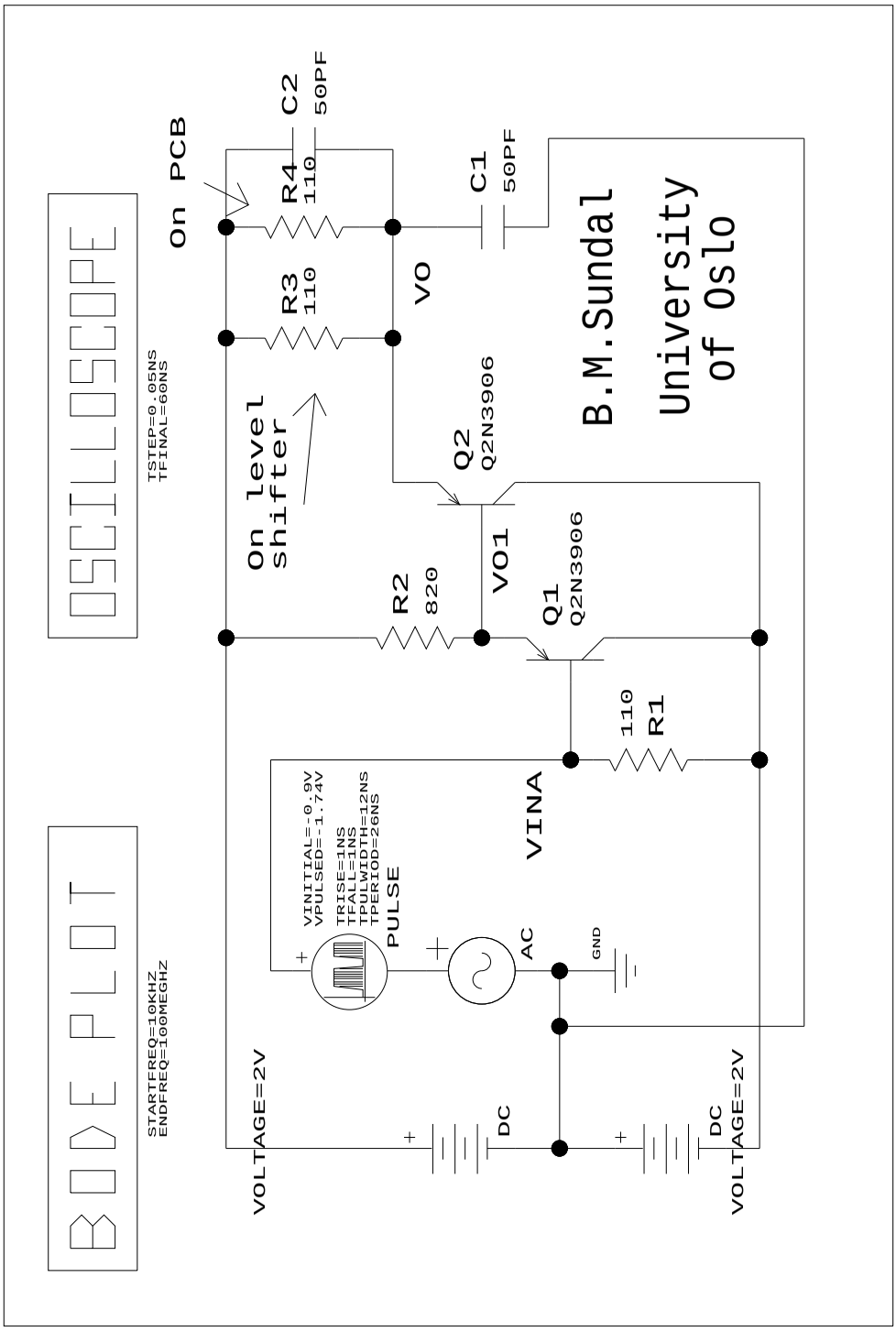

Figure 3.28: Schematic for simulation of BCO level shifter.

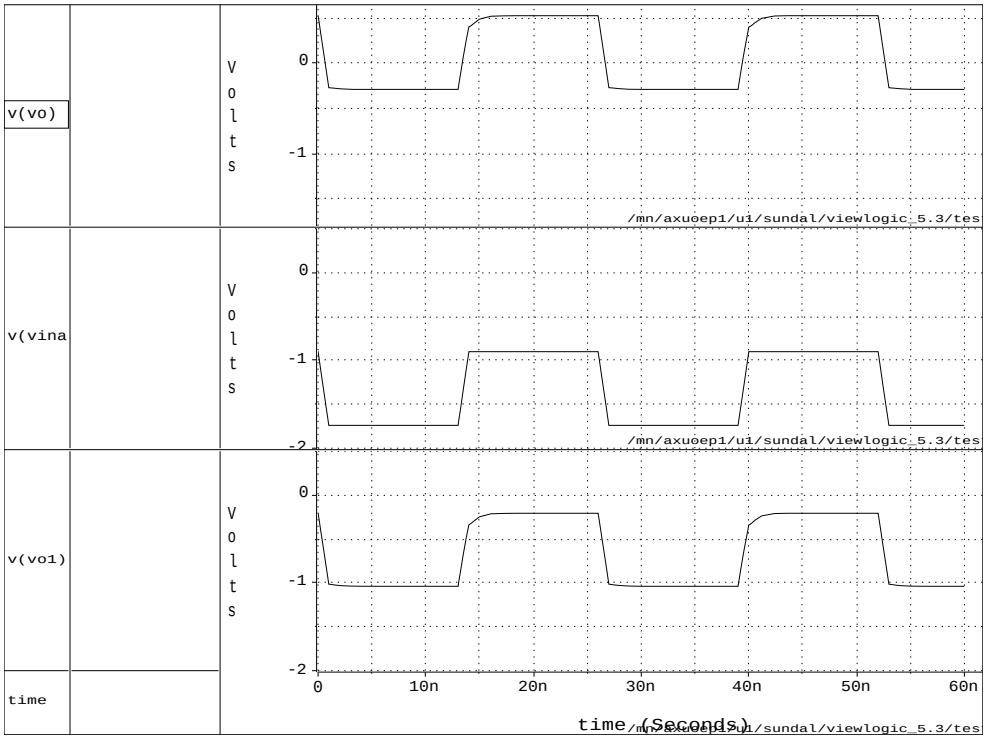

Figure 3.29: Result of transient solution for BCO-shifter.

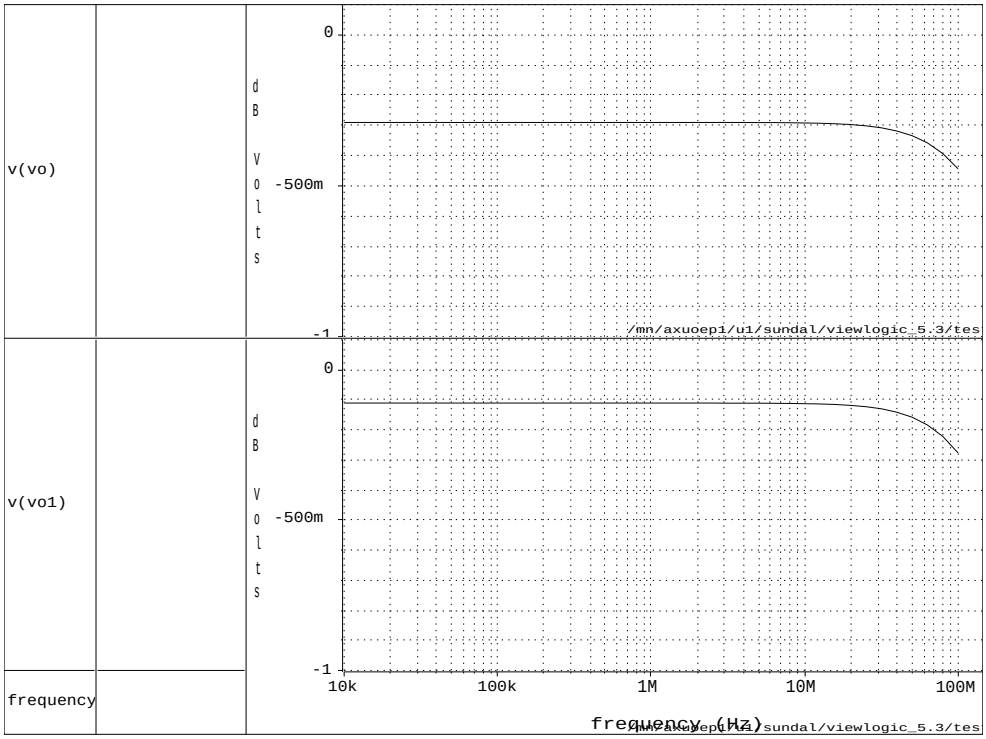

Figure 3.30: The Bode plot for the BCO-shifter.

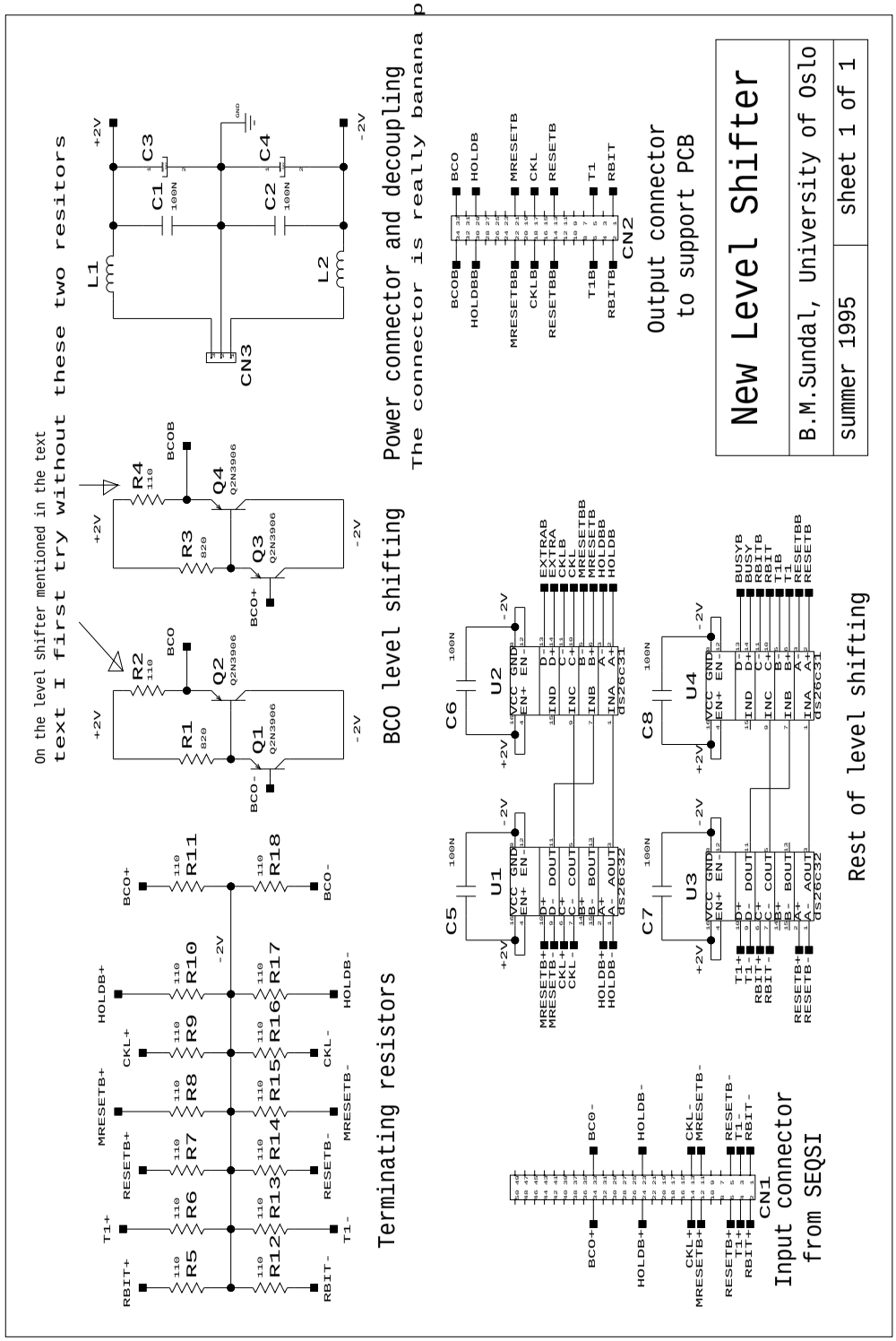

Figure 3.31: Schematic for the new level shifter.

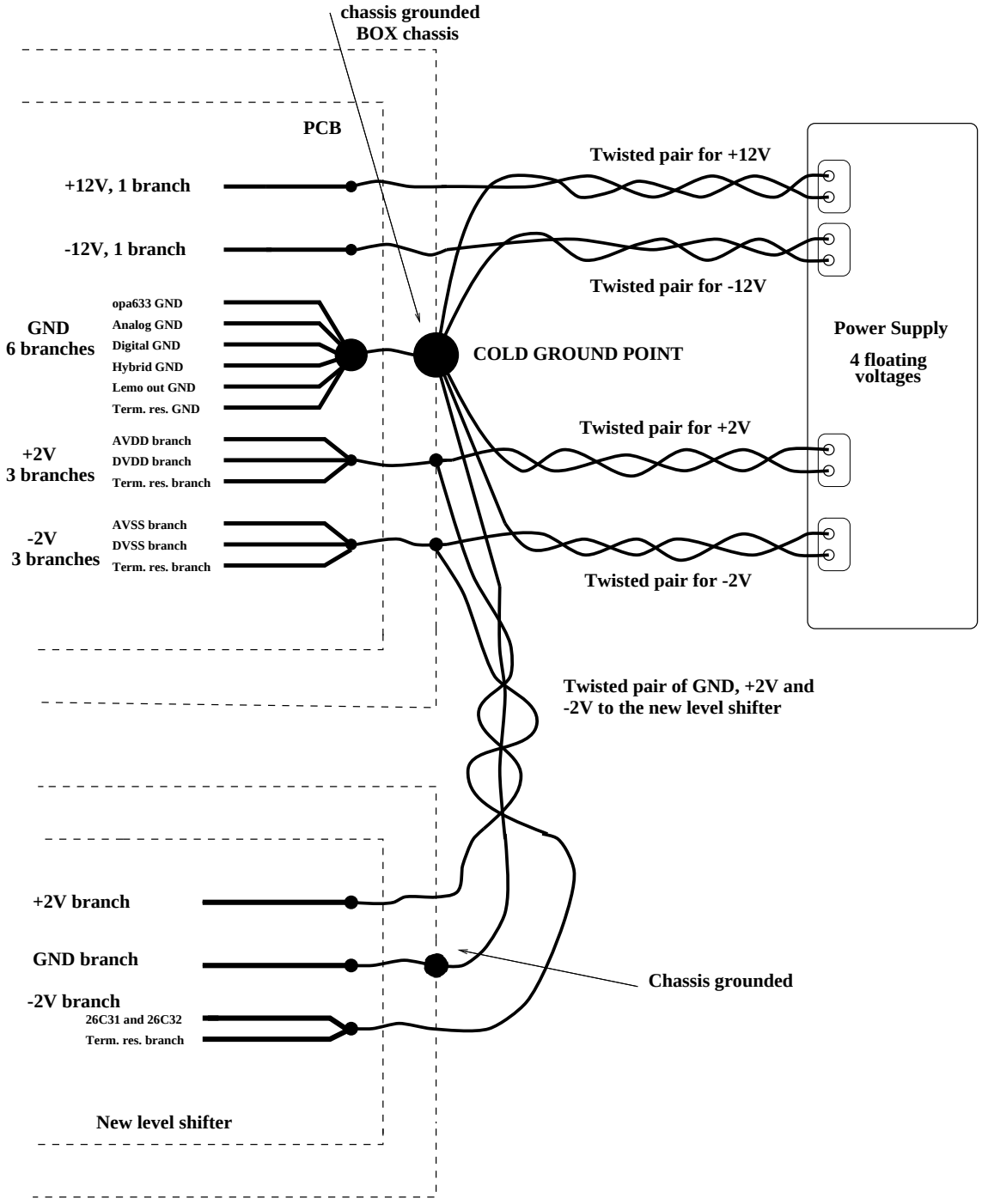

Figure 3.32: New strategy for providing ground and supply voltages for the test setup.

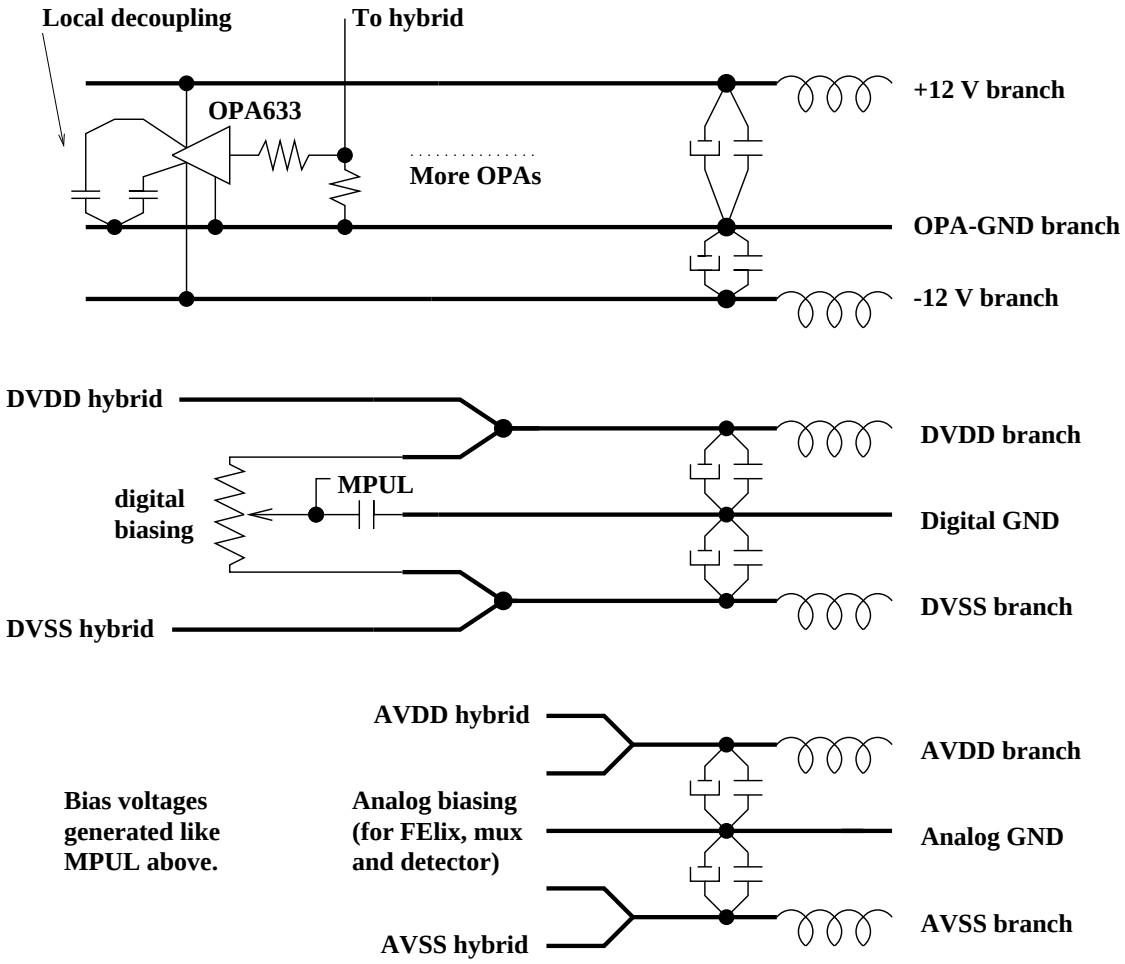

Figure 3.33: Filtering and decoupling of supply voltages and what happens on the different branches of the supply voltages for the PCB.

To change the PCB to look like figure 3.33 a lot of cutting of tracks and soldering in of new wires was needed. On the new level shifter a similar scheme of decoupling and supplying was followed.

3.7 Performance of the new test setup

After these improvements the test setup was very stable. Pickup from the BCO could not be found on the different power, biasing and signal lines. The digital signals were not found to introduce noticeable pickup on each other.

The hybrids were split in two groups, one with Felix chips with old logic and the other with Felix chips with new logic. The FElix chips with new logic had not been proven to work earlier.

The broken channels (INP inputs) were tested. A many MIP signal was injected. The OUTAMP11 and OUTAMP21 gave output signals, which could be shaped as by altering VFP as expected. This indicated that the pre-amp/shapers were working on all hybrids.

To check that nothing was wrong with the setup, the hybrids with detectors and old logic chips were tested to see if they could give DTA outputs. These chips had been proved working before. The first test of these hybrids did not give a DTA. This indicated an error in the setup. The error was found in the end, and was located in the circuitry for bringing out the DTA. The pull up resistors for the DTA signals was not connected to ground on the PCB. This error occurred when the new ground/power and decoupling strategy was implemented.

With the removal of this setup error all four hybrids and all chips (both new and old logic) were found to be working, in the sense that they gave an DTA output in response to a T1. This was a strong indication that the digital part of the chips were working.

In the new logic the DTAs do not come in groups of two. The 250 ns break between the two are removed, and the DTA extended to be a single 1.6 μs pulse. This was the first verification of a working FElix with the new logic.

Since two hybrids are glued to detectors (old logic) and two to a charge injection board for a pulse in one channel (new logic), the only way to do direct comparisons between old and new chips were through CAL.

A long T1 (12 units of 25 ns) (as used at CERN and in the sequence presented in earlier sections) gave as expected three groups of DTA pairs with old logic, but only 2 groups with new logic.

Both logics were now tested with only a 50 ns long T1, which gave only one DTA group. Biasing was adjusted to approximately correct pre-amp/shaper waveform, and peak mode read-outs for both logics were done. The sequences were modified a bit to have the HOLDB placed in the exact right spot relative to the DTA.

Very similar results where found for both logics when the CAL input was moved around in time. A 0.4 V step was used for CAL, which should be equivalent to 6 or 7 MIPs. When CAL was in the interval 1.6 to 1.8 μs ahead of T1, for both logics a DC drop was seen in all channels in the MUX read-out. The drop was not more than about 13 mV/MIP.

Figure 3.34: Oscilloscope screen dumps. FElix with new logic in peak mode. Showing channels excited (lower) and not excited (upper) with CAL.

If the shaping time was increased a bit more mV/MIP was gained and the FElix looked more alive. Figure 3.34 shows oscilloscope traces for the new logic. The old logic showed almost exactly the same behavior. The figure shows two oscilloscope screen dumps. In the upper the test pulse is too early to excite the chip and give a drop in the AMUX channel outputs. And the lower one is for the delay where the drop is at its maximum. Each screen dump shows as the upper trace the analog test input, which is a 0.4 V step, and the AMUX output as the lower trace. The sampled channels correspond to the around five last centimeters of the AMUX output. In the lower screen dump one sees a drop of about 80 mV. In the last centimeter of the lower screen dump there is a peak in the AMUX output. This is a very noisy channel, because it is bonded over to the charge injection board not in use. The T1 is placed 2 centimeters from the left edge, or about 1.7 μs after the edge of the test input.

It was very difficult to adjust the biasing of the chips to obtain stable operation. This can maybe be contributed to the fact that ADB storage capacitor backplanes and the APSP capacitor backplanes are only decoupled to ground, and there is no way of setting up specific voltages on them. This is different from the test setup at CERN.

The problem that one had to sample in the second DTA group, which was seen at CERN, because the values from the first was garbage, was not observed. When a longer T1 was used and the sampling was done in the second DTA group, no noticeable changes to the CAL response from what mentioned above was found.

The use of CAL is limited, and what one sees is not always easy to interpret. A possibility of exciting only some of the channels, as with the CAL10 in the FElix128, would have been nice.

Something strange was found with the new logic. When a many MIP signal was injected into one channel (this was only possible with the hybrids with FElixes with the new logic), this specific channel was very noisy in the AMUX output, but not more when the injected signal was on the supposed right timing, than elsewhere. Only first when the injected pulse was around 3.5 μs after the T1 (and around 0.5 μs before the long DTA) the right channel in the MUX output gave an enormous signal. No good explanation can be given. This is either an error in the new logic, or something wrong with the injection of charge via the charge injection board.

Some more digital tests to see how the chips responded to various lengths of T1s were performed. The results are stated below and are more or less as expected, which is a level sensitive T1 where new triggers seem to be accepted about each 100 ns.

With old logic it is found:

- A 300 ns T1 gave three DTA groups.
- A 200 ns T1 gave two DTA groups.
- A 100 ns T1 gave one DTA group.
- A 50 ns T1 gave one group.

With new logic:

- 25 ns T1 gave one DTA. Same CAL response as in the description above.
- Two 25 ns T1s with 125 ns in between gave 2 DTAs as expected.
- With only 100 ns in between only one DTA was found. By extending the length of the two T1s to 50 ns two DTAs were again observed.

To test the full hybrids with detectors, which is beyond the scope of this thesis, a β-setup is needed. In this setup a β-source put on top of the detector provides particles (MIPs). By putting a scintillator underneath the detector one can get a signal to trigger the sequencer. A β-setup will hopefully be set up during the end of this year or early next year in the Particle Physics group lab. Only then can a full evaluation of the FElixes and hybrids performance be done and signal-to-noise of the module be measured.

3.8 Algorithmic State Machine for read-out of FElix and AMUX

In the read-out of the FElix and the AMUX, usually the VME sequencer is used. I found it interesting to try to use some of the signals that the FElix provides to make an algorithmic state machine (ASM), that could read-out the FElix and AMUX using these signals as a kind of handshake synchronizing the read-out. To make this machine [10, chapter 8] was used as a reference text to an algorithmic state machine.

Every time the FElix puts something on its output, it pulls the DTA signal high. As described in the FElix section, the DTA signal is high twice during the read-out associated with one trigger. First it is high for 550 ns when the peak value is output, then it is low for 250 ns, which is the signal reset time, before its high again for another 550 ns, when the de-convoluted value is output. Since the minimum read-out period for the FElix is $4\,\mu$s, there will not be a rising edge of a DTA before at least $(4 - 0.55 - 0.25 - 0.55)\,\mu\text{s} = 2.65\,\mu\text{s}$ after the falling edge of the last DTA of the previous event.

If the DTA signals are used (the first for the peak value, and the second for the de-convoluted) to control the sample/hold of the AMUX and to generate a read-out clock of a wanted frequency, it should be possible to read-out the FElix without the sequencer. Since the read-out clock is often slow, it will often take more than $4\,\mu$s to read-out the FElix. Therefore a BUSY signal is made, which can be hooked up to the FElix, but only for the full hybrid, since the prototype hybrid has the BUSY pulled low internal to the hybrid. While BUSY is high the FElix will not initiate another read-out (even if it has got a trigger) before it is pulled low again. The BUSY logic has not been used earlier and it would be interesting to see if this part of the logic works.

Figure 3.35 describes the signals wanted, in response to the inputs DTA and BCO-clock. The task is to make a state machine that can give this sequence.

Figure 3.36 shows such a machine. The machine has four states. In state T_0 it waits for the first or second DTA pulse. In T_1 the sampling is done, depending upon the choice of peak or de-convoluted value. After the sampling, it is in state T_2 where it remains until

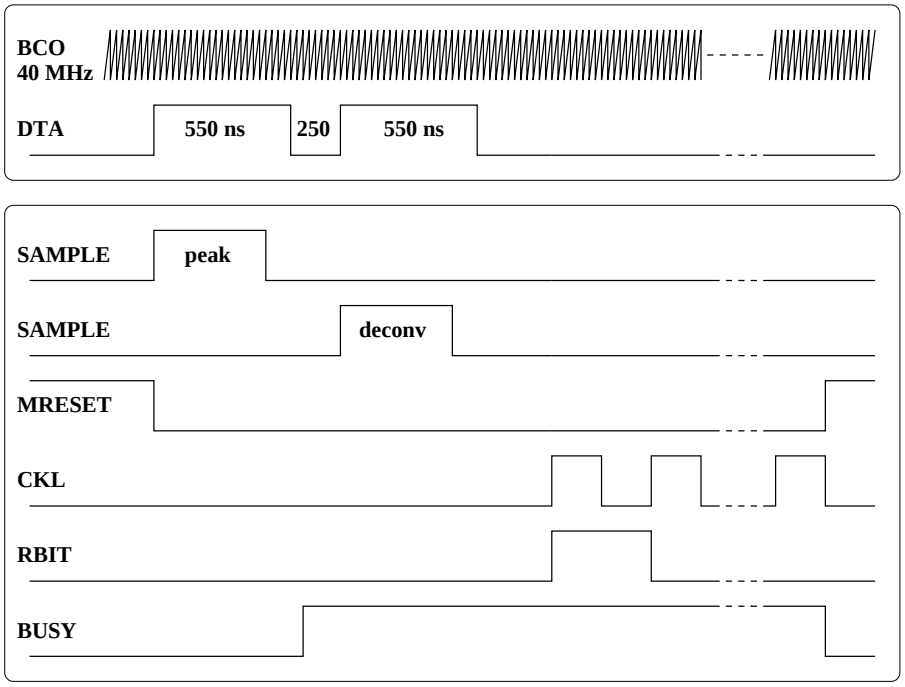

Figure 3.35: The wanted response of the state machine to DTA.

DTA goes low. The reason for finishing the sampling before the end of the DTA, is that using the end of DTA for this purpose would risk that one sampled a bit after the signal reset is started. This would give the wrong value. When DTA goes low it leaves T_2 and goes either to T_0, if it was the first DTA, or to T_3, if it was the second DTA. In T_3 the read-out (running AMUX clock) is done.

The circuit is built with TTL-logic using 74F-circuits, and implemented as a wire-wrap card. To synchronize the card with the FElix the 40 MHz BCO for the FElix is used as the master clock. It is divided by two to 20 MHz (named OSC in the schematic), and this clock is used by the state machine. All flip-flops used are positive edge triggered.

The construction of the physical machine from figure 3.36 was made in five steps:

1. Make the controller part.
2. Make the data processor part of the machine.
3. Build outputs from the information in the data and controller part.
4. Simulate the circuit.
5. Wire wrap the card.

Since the three first items describe the design of the machine, the schematic of the full circuit will not be presented before in the subsection describing the simulation (figure 3.39).

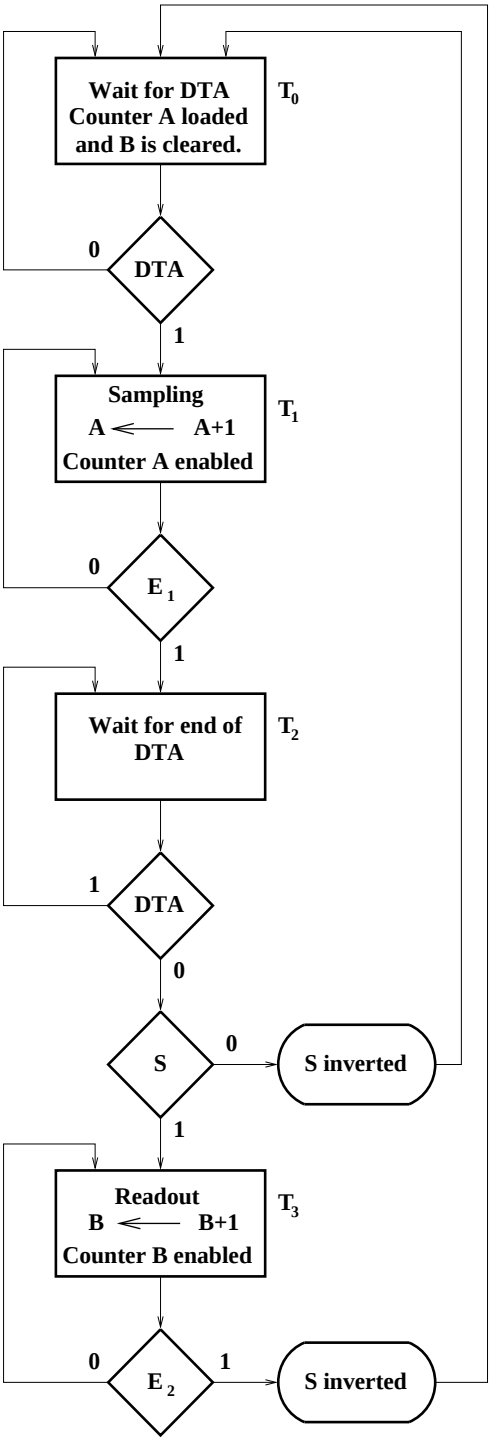

Figure 3.36: The algorithmic state machine.

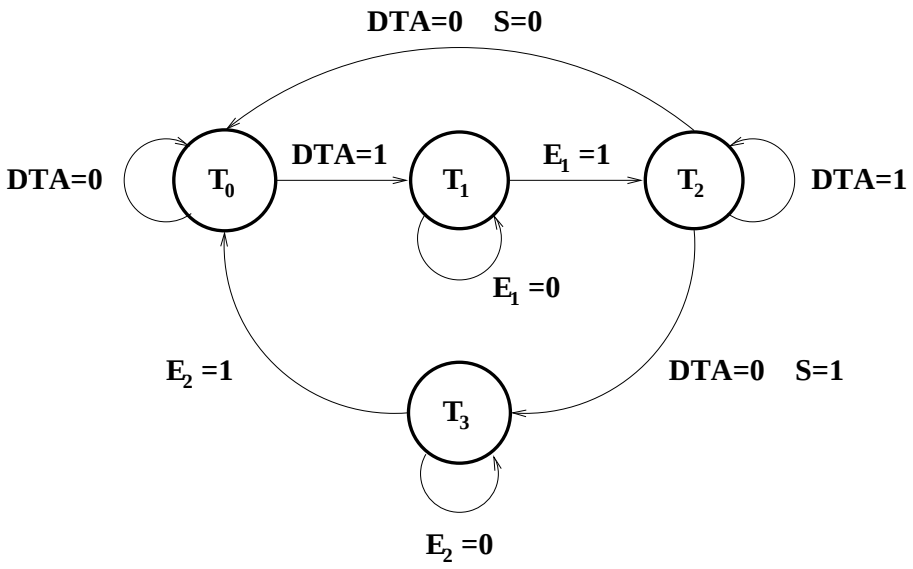

Figure 3.37: Flow of states in the controller for the ASM.

3.8.1 The controller

The transitions of states in the controller part of the state machine is shown in figure 3.37. Two implement this controller a D-flip-flop for each state is used. The total controller requires a 4-bit register (a 74F175 D-flip-flop 4-bit register with asynchronous clear and outputs both for the Q's and the $\overline{Q}$'s) to keep the state information. To be in state T_0 means that the Q-output of the flip-flop for this state is 1. The other three flip-flops must be zero. A D-flip-flop puts on the Q-output the value that was on the D-input before it was clocked. Logic gates are put around the 4 bit register in order to implement the flow of states according to figure 3.37.

If one takes state T_0 as an example it is seen from figure 3.37 that the machine ends up in state T_0 after clocking if one of the three following conditions apply before clocking:

- The machine was in state T_0 ($Q_0 = 1$) and DTA was zero.
- The machine was in state T_3 ($Q_3 = 1$) and E_2 was one.
- The machine was in state T_2 ($Q_2 = 1$) and both DTA and S was zero.

If one of these conditions apply, the D-input of the T_0-flip-flop must be 1 before clocking (and the other D-flip-flops must have zero on their inputs), so that the machine ends up in state T_0 (Q-output is one) after clocking. The D-input of the T_0-state D-flip-flop is given by

$$D_0 = Q_0 \cdot \overline{DTA} + Q_2 \cdot \overline{DTAS} + Q_3 \cdot E_2 \tag{3.26}$$

Here the bars mean Boolean negation, the sums are Boolean OR and the multiplications are Boolean AND, according to common practise.

The D-inputs of the rest of the flip-flops (register part of controller) are found in the same way, and the full logic for the controller part is given by the set of equations

$$\begin{aligned} D_0 &= Q_0 \cdot \overline{DTA} + Q_2 \cdot \overline{DTAS} + Q_3 \cdot E_2 \\ D_1 &= Q_0 \cdot DTA + Q_1 \cdot \overline{E_1} \\ D_2 &= Q_1 \cdot E_1 + Q_2 \cdot DTA \\ D_3 &= Q_2 \cdot \overline{DTA} \cdot S + Q_3 \cdot \overline{E_2}. \end{aligned}$$

There is one little problem. When the 4-bit register is reset, for instance after turning on the power, all Q-outputs of the register will be zero, and the machine is therefore in none of the states. This is solved by naming the $\overline{Q_0}$-output of the register T_0 and putting an inverter on the D_0-input. When the register is reset the machine will be in state T_0 afterwards since $\overline{Q_0}$ is one. The inverter on the input just assures that what was initially wanted on the Q_0-output now ends on the $\overline{Q_0}$-output.

3.8.2 The data processor

In figure 3.36 there are two counters A and B. Counter A (4 bits) counts the length of the sampling, and counter B (12 bits) counts the number of read-out cycles for the AMUX. 74F161 4-bit synchronous counters with asynchronous clear are used to implement counters A and B. The counter has two pins, ENP and ENT, for enabling of the counting. These two enables are coupled together to one enable, hereafter called EN.

The desired functionality is as follows. Counter A counts during T_1, which means it must be enabled in that state, from its loaded value until it reaches 15, using the 20 MHz OSC. That means that the condition E_1 in figure 3.36 of the state machine is the equality of 15 and the counter value. The length of the sampling is then 15 minus the DIP-switch value, measured in units of $\frac{1}{20\,\mathrm{MHz}} = 50\,\mathrm{ns}$. The counter is loaded during T_0. To load requires both that the $\overline{\mathrm{LOAD}}$-pin is asserted and that the chip-clock-pin has a positive edge. Since the 20 MHz OSC clocks this counter, and it is always running, one is sure to load the counter during T_0. The clear of counter A is not used since it is loaded already during T_0.

B counts up from its initial value during state T_3. This counter is clocked by the read-out clock, CKL[3], that only is running during T_3. When the counter reach 1024 the read-out state T_3 is ended, and CKL stops. The condition that the counter reach 1024, only means that the 11 bit is high for the first time, and condition E_2 in figure 3.36 of the state machine can then be taken as the 11th bit of counter B. The number of read-out cycles is going to be 1025 minus the DIP-switch value. The reason for 1025 instead of 1024 is that during the first CKL-cycle counter B is loaded with the DIP-switch value. This is done by using the RBIT as the counter LOAD. The counter is reset during state T_0. Since B is a counter, which has more than 4 bits, three 74F161s counters need to be connected together to give a 12 bit counter.

[3]In reality $\overline{\mathrm{CKL}}$ so that the last read-out clock cycle is not cut before it is as long as the other cycles.

S is a one bit memory. It keeps track on whether it is the first or second DTA-pulse (peak or de-convoluted). It is zero initially and during the first DTA. From the first clock cycle after the first DTA goes low and until the end of the read-out S is one. This is seen from figure 3.36. A 74F109 J/$\overline{\text{K}}$-flip-flop is used for S. The S bit should be a T-flip-flop, which means that the input to $\overline{\text{K}}$ must always be opposite to J.

Figure 3.36 of the state machine describes what is happening in the data processor in the various states.

In state T_0 counter A is loaded, and during RBIT counter B is loaded. In state T_1 counter A is enabled for counting, and in T_3 counter B is enabled. Counter A is never cleared, while B is cleared during T_0. If the machine is in state T_2 and DTA and S are both zero, the S-bit T-flip-flop will have to be inverted. The T-flip flop has the feature that it inverts its Q-output after clocking, when the T-input before clocking was one. If the T-input was zero, the output does not change. If in state T_3 and E_2 is one, the S is inverted again. The list of equations for the data processor will then read

$$\begin{aligned}
\overline{\text{LOAD}_\text{A}} &= \overline{\text{Q}_0} \\
\overline{\text{LOAD}_\text{B}} &= \overline{\text{RBITB}} \\
\text{EN}_\text{A} &= \text{Q}_1 \\
\text{EN}_\text{B} &= \text{Q}_3 \\
\overline{\text{CLR}_\text{A}} &= \overline{0} \\
\overline{\text{CLR}_\text{B}} &= \overline{\text{Q}_0} \\
\text{T}_\text{S} &= \text{Q}_2 \cdot \overline{\text{DTA}} \cdot \overline{\text{S}} + \text{Q}_3 \cdot \text{E}_2
\end{aligned}$$

3.8.3 The state machine outputs

For the outputs care is taken not to create them from signals changing at the same time. This avoids typical digital problems like hazards and races. An example is given in figure 3.38, which shows what can happen if two signals that are supposed to change at the same time have some small delay. The OR-ing of the two signals produce one clean output if the delay is in one direction, and an ugly output with a spike if the delay is in the other direction.

The FElix specifications say that the BUSY must be asserted somewhere between one BCO before the first DTA and 13 BCOs after the second DTA. S is therefore used as BUSY. It is asserted between the two DTAs and are high until the read-out (T_3) is finished. The equation is

$$\text{BUSY} = \text{S}.$$

The sampling is done inside T_1, but there are two T_1s. One for the de-convoluted and one for the peak DTA, in the last one the S is one and in the first one S is zero. By setting a switch on the wire wrap board one can choose between de-convoluted or peak. This switch is called DCV in schematic, DCV is one for de-convoluted and zero for peak. The

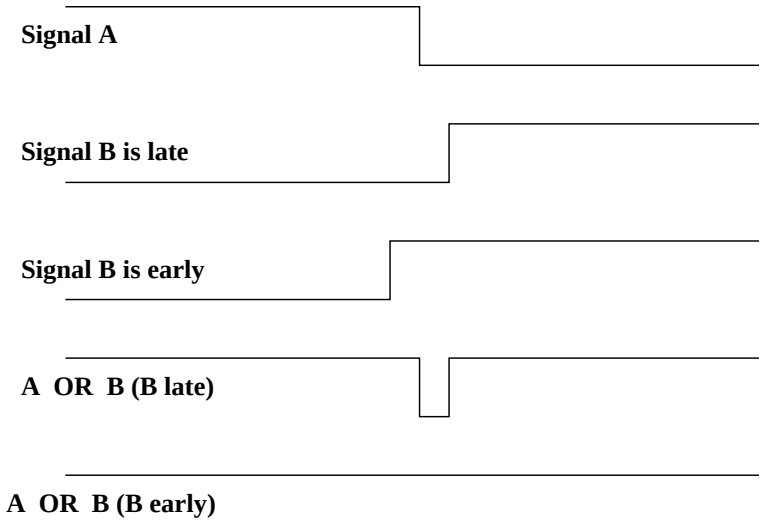

Figure 3.38: The wrong way to generate output signals.

SAMPLE can be obtained from the equation

$$\overline{\mathrm{SAMPLE}} = \mathrm{Q}_1 \cdot (\mathrm{S} \cdot \mathrm{DCV} + \overline{\mathrm{S}} \cdot \overline{\mathrm{DCV}}).$$

As a remark, remember that the two signals SAMPLE, used on the 4-chip hybrid, and HOLDB, used on the prototype hybrid, are equivalent. Both names indicate that the sampling is done when the signal is high, and the holding when the signal is low. The B in the end of HOLDB has the same function as the bars used in this section about the state machine. These are two ways of indicating that a signal is asserted low.

The AMUX should be reset in state T_0, but only in the idle phase outside the sequence, and not for the T_0 in between the two DTAs. There S = 0 so the obvious solution would be to set MRESET = $\mathrm{Q}_0 \cdot \overline{\mathrm{S}}$. This is not true, since both the S and Q_0-flip-flop can change state at the same clock edge. When the machine goes from state T_2 to T_0, S is inverted as one can see from figure 3.36 of the state machine.

The solution is to generate a new signal, which is called DTAT. A T-flip-flop, where the T-input is permanently at one, is clocked by the DTA-pulse. Its Q-output, called DTAT, goes high at the first clock cycle (OSC) after the first DTA and goes low again at the first clock cycle after the second DTA-pulse starts. If one now generates MRESET from S and DTA one will have

$$\overline{\mathrm{MRESET}} = \mathrm{DTAT} + \mathrm{S}.$$

For the read-out clock, CKL, an alterable frequency is desirable. This is done by using a 4-bit counter as a clock divider. For the clock input of the counter the 20 MHz OSC is used. The least significant output bit will then be a 10 MHz, the next bit a 5 MHz, then a 2.5 MHz, and finally the most significant output bit of the counter will be a 1.25 MHz clock. These 4 clocks are sent into a multiplexer, a 74F153 dual 4-to-1 multiplexer. The two bits address lines of this multiplexer, which controls which clock is output, is controlled by a

DIP-switch. The value on this DIP-switch is called n. It is important to note that the $\overline{\text{CLR}}$ of this counter is connected to Q_3 so it is only counting in state T_3, to assure that it starts with all outputs (clocks) at zero. The enable of the counter is always on. The read-out clock for the AMUX is given by the n'th output of the multiplexer

$$\text{CKL} = \text{MUX}_{\text{line n}},$$

where n is one of the four output bits of the clock divider.

The read-out bit, RBIT is clocked into the AMUX on a negative edge of the CKL. To clock it into the AMUX on the first negative edge of the CKL-cycle, one needs a RBIT that is high the whole first CKL-cycle. Then the RBIT will be clocked into the AMUX on the negative edge of the CKL in the middle of the first clock period. This can seen in figure 3.35 of the desired signals. This is done by using two D-flip-flops. Both are reset during T_0 and clocked by CKL. The first has its D-input hardwired at 1. This D-flip-flop goes high at the first CKL. The next D-flip-flop uses the output of the first as its D-input. And it will therefore go high at the second CKL pulse. If the Q-outputs of these two flip-flops are called U and V respectively, one finds that $\text{U} \cdot \overline{\text{V}}$ is one during the first CKL cycle. The RBIT for the AMUX is then given by

$$\text{RBIT} = \text{U} \cdot \overline{\text{V}}.$$

3.8.4 Simulations of the state machine

The schematic of the state machine is shown in figure 3.39, drawn in Viewdraw. The signals with bars in the text have names ending with B in the schematic. The labels PLUS and ZERO in the schematic denote the +5V and the ground, respectively. The signal CLEAR in the schematic is coupled to a push button and returns the circuit to state T_0.

In the schematic one finds only 74LS and not 74F circuits, since the simulation library only had the former components. The 74LS circuits are slower, so the simulation is done at lower frequency than the real machine operates at. This does not change the relative timing between signals. The main purpose of the simulation is to demonstrate the correct implementation of the logic. From the data sheets for the 74F-circuits one can convince oneself that the state machine can run at 20 MHz.

Since only NAND-gates are used in the schematic, one needs to show that the typical expression

$$A \cdot B + C \cdot D \tag{3.27}$$

used in the text can be implemented using only NAND-gates. The relevant theorem is

$$X + Y = \overline{\overline{X} \cdot \overline{Y}} \tag{3.28}$$

easily verified by inserting all four combinations of X's and Y's into both sides of the equation. By using equation 3.28 on equation 3.27 one obtains the result

$$A \cdot B + C \cdot D = \overline{\overline{A \cdot B} \cdot \overline{C \cdot D}}. \tag{3.29}$$

The operation of sending A and B through a AND-gate, C and D through another AND-gate, and sending the output of these to gates through a OR-gate, is obtained just as easily by replacing AND-gates and OR-gates with NAND-gates.

Inverting signals is easily done by a two input NAND-gate, by connecting both inputs together and call this the inverter input. Dedicated inverters are used instead since a 74F04 package of inverters contains six inverters, while a 74F00 package only contains 4 two-input NAND-gates.

The simulation result of the circuit, using Viewsim, gives the output waveforms in figure 3.40 as presented by Viewtrace, a waveform display program. These waveforms can be compared to figure 3.35 of the wanted sequence, and full agreement is found. Several of the internal signals in the state machine are also shown, which makes it possible to follow the flow of data and control.

3.8.5 Wire wrapping of the card and testing

Figure 3.41 shows the wire wrap card, as seen from the component side.

The circuit was tested by using two pulse generators. One of the generators provided the 40 MHz BCO as TTL-levels. The other provided pulses of one μs length separated by 20 μs or longer. This should simulate DTA pulses. Even though this is not exactly how the DTA looks it is sufficient to test the state machine. The DIP switches was set to make very few CKL-cycles, typically eight or so, which made them easy to count.

The machine worked well. It made groups out of two and two DTAs. The SAMPLE was in every other of the DTAs, and its length could be controlled by the switch for counter A. The CKL and the RBIT was correct, and the amount of CKL-cycles could be controlled by the counter B switch. A 2-bit DIP-switch controls the CKL-frequency, an ordinary switch changes between de-convoluted and peak mode and a push button can reset the machine to state 0, waiting for a new DTA.

The board has not been tested together with the PCB and hybrid. This would need some amount of interfacing.

- A BCO must be provided both to the PCB/hybrid and to the state machine as TTL-levels. This can be obtained by using the NIM-output BCO sent through a NIM-to-TTL converter in the NIM-crate.

- A 26C32 receiver should be placed on the state machine board. One of the four channels on this 26C32 should receive the DTA before it is provided to the rest of the state machine. This can be done by sending the DTA-signal from the PCB/hybrid (DTA from both FElixes are output on its own lemo-connector) to one input leg of the differential receiver. The other leg should be adjusted to a DC-value in the middle of the high and low values of the DTA signal.

- The setup, with the state machine and the FElix doing handshaking, does of course need some external logic to provide the T1 for the FElix. If the setup is for testing a hybrid with a charge injection board one can just send in the T1 trigger (via the level

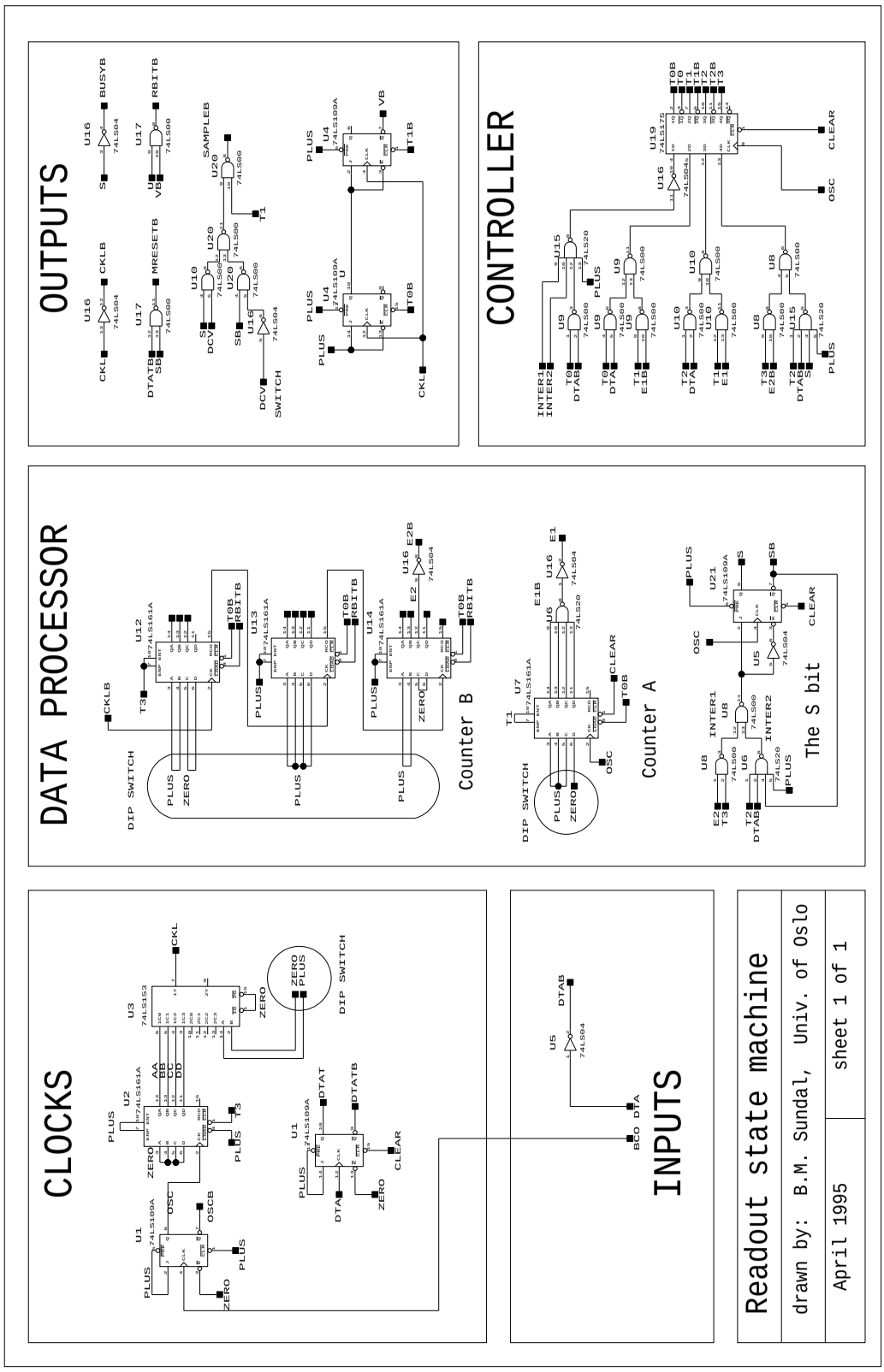

Figure 3.39: The schematic for the algorithmic state machine.

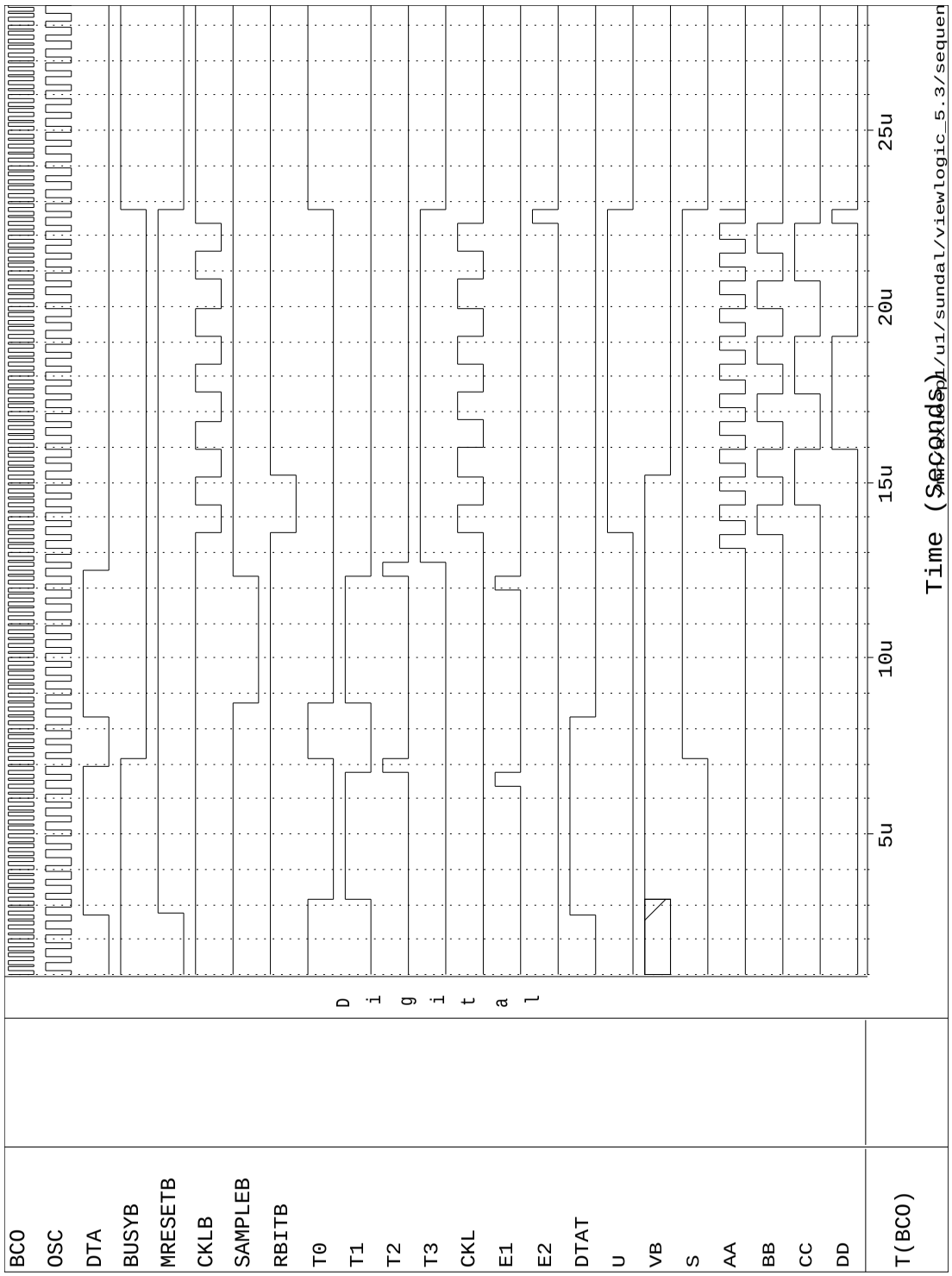

Figure 3.40: Simulation waveforms for the algorithmic state machine. The sequence is for de-convoluted modus.

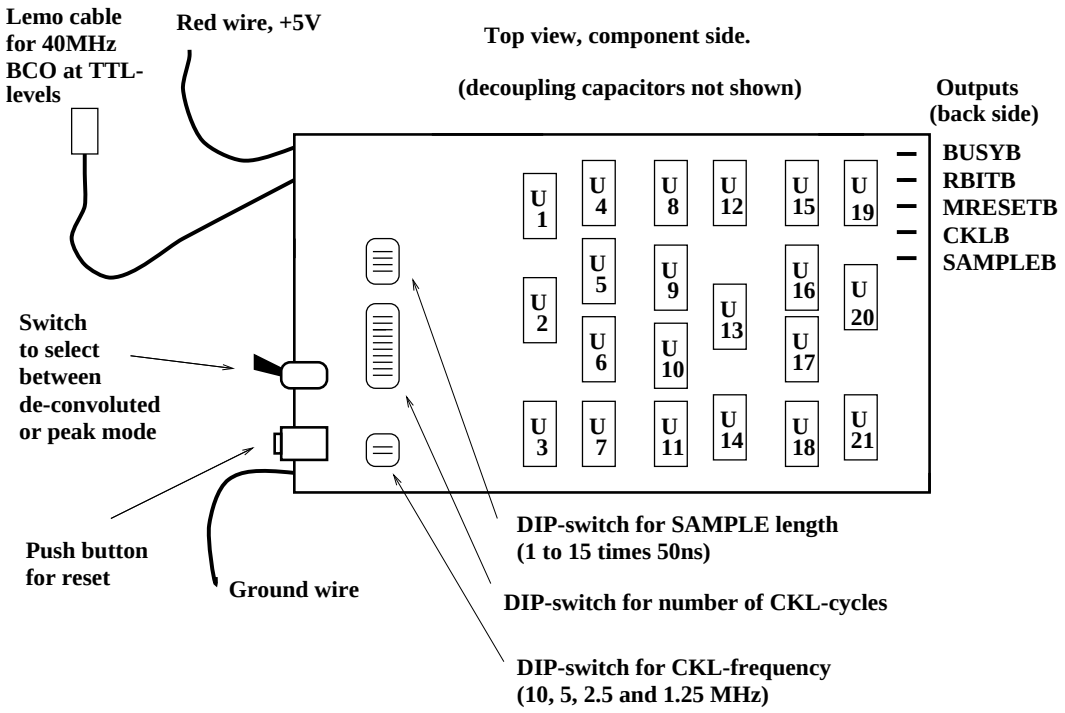

Figure 3.41: The state machine wire wrap card.

shifter) the right amount of time, which is about 1.7 μs, after the charge injection pulse was sent. If one uses a β-setup for hybrids with detectors, one needs to send a T1 trigger to the FElix about two μs after one receives a pulse from the scintillator, which indicates that a particle has passed the detector.

Chapter 4

The Z-module hybrid

The schematic for the Z-module hybrid, was made during early May 1995. The hope was to finish the hybrid in time for the H8 test-beam at CERN in the autumn of 1995.

The goal was to make a hybrid which could be used to put together a realistic prototype Z-module, except from the fact that the prototype would be single sided.

For the hybrid this means that one side must house four 128 channels front-end amplifiers, on an area not much bigger than the expected final size of 3 cm by 8 cm. To read-out the FElixes, AMUXes will be used as earlier.

It was decided to make the hybrid compatible with a UK hybrid[1] in terms of size and chip placement, in order to use UK fan-ins, detectors and boxes for test beam.

Even though the test hybrid had not undergone complete electrical tests by May, the concept of using four functional layers was believed in. Gandhis workshop at CERN was selected to make the Z-module hybrid. The possibility of using smaller line-widths combined with shorter production time, was the main motivation for choosing Gandhis instead of the Norwegian company AME. The large number of signals to route out for the chips, made the change to thinner lines rather essential.

4.1 The changes in the 128-channel FElix and AMUX

The 128 channel FElix was produced in July 1995. Since all tests of the previous two 32 channel versions had not been finalized, SI/Sintef decided to keep the old well proven digital concept.

The only major difference in the new FElix, is that all the digital control signals are differential, and can use signals directly from SEQSI ECL-drivers. For testing this is very convenient. But in the end ECL can not be used, because of high power consumption due to small terminating resistors.

There is now just one broken channel, but the channel is only broken between the preamp/shaper and the ADB. Between the ADB and the APSP the signal passes a bonding pad, so that it can be brought out.

[1] UK groups makes a Z-module prototype for the front-end chip APV5.

There is introduced a new calibrate signal, called CAL10, which a 0.07 V step will give a 1 MIP signal in every tenth channel of the FElix.

A description of the FElix128 is given in appendix B. The information assembled in the appendix was made on request by the chip designers. In this appendix there is a extensive list of all signals, showing typical voltages and currents for the biasing, together with other information.

The 128 channel AMUX was produced early in 1995. Also for the AMUX the digital controls are differential. For the biasing only one of the three original is left, this is the SFBI for the biasing of the sample and hold buffer. The read-out bit is output after it has passed through the shift register, in this way several AMUXes can be daisy chained. The output of the read bit from one AMUX to the next is differential, and each line should be pulled to DVSS by a 470 Ω resistor. The analog output (differential) is kept on a high impedance as long as there is no read bit in the shift register. In this way several daisy chained AMUXes can have their output on to the same analog bus line. This relieves the hybrid designer from the problem of routing out analog signals from four MUXes, and saves connector pins. It is recommended that the analog bus line is pulled to AVSS by a 10 kΩ resistor.

In appendix C, a list of the AMUX128 signals are given. The placement of pads on this chip is very regular. The analog inputs from the FElix128 are on the top edge, whereas the pads for bonding is on the bottom edge. Here top and bottom edge refers to the schematic and layout of the hybrid. The AMUX128 symbol in the schematic (figure 4.2) looks very much like the chip itself.

4.2 The Z-module hybrid schematic

The schematic for the hybrid can not be made without thinking of how the components will be placed in the layout. Therefore a rough preliminary drawing of the layout is needed. Such a drawing is found in figure 4.1.

The size of the hybrid and the placement of the FElixes, were the easiest parts. Both were defined by the UK hybrid. The size of the hybrid is 45 mm by 90 mm.

To have as many pins as possible on as little space as possible, 24-pin Dupont connectors were used. The layout drawing indicated that there were room for six of these connectors.

The connectors was numbered from CON1 to CON6. CON1 houses analog power and ground, and all biasing for the left detector. CON6 has the same purpose for digital power and the right detector. Later discussions led to the removal of digital ground. The hybrid would therefore have one ground plane brought out only on CON1.

For the supply voltages AVSS, AVDD, DVSS and DVDD, and for ground, as much as four pins each on the connectors were allocated. In this way the tracks on the kapton cables providing these supplies could be as wide as possible. Each Felix use over 100 mA, which ends up mostly in AVSS. The whole hybrid could therefore use as much as 0.5 A, which requires a fat track for the supply voltages.

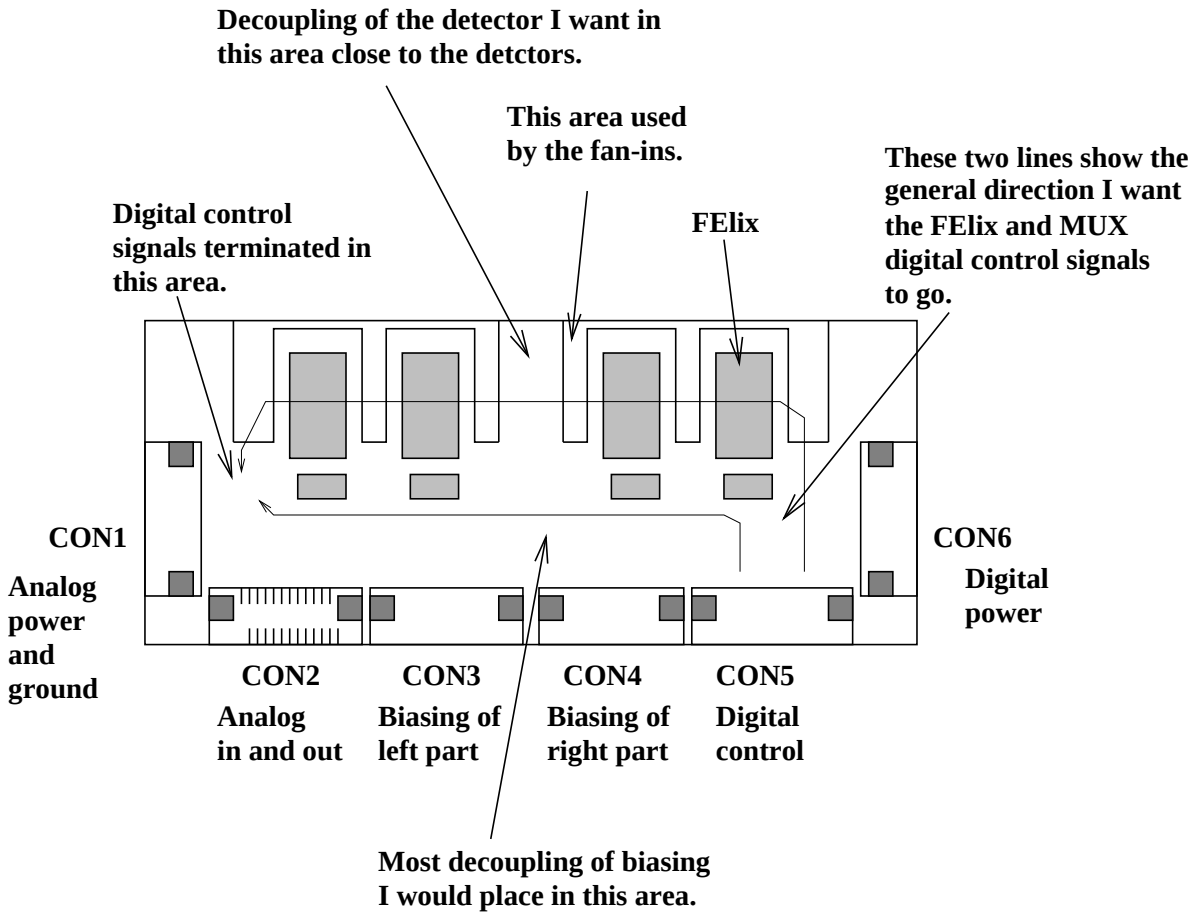

Figure 4.1: A first layout drawing used as guideline in the making of the hybrid schematic.

The test inputs and the analog outputs were placed on CON2. This is mostly because the AMUX placed right above this connector was to be the last in the daisy-chain.

CON5 has all the digital control signals. A total of eight differential signals requires 16 pins, which means that there are room for screening in between each signal pair.

To ease the routing of the biasing the hybrid was divided into two biasing parts. CON3 provides all biasing for the chips on the left half, and CON4 all the biasing for the right part. The placement of the biasing is the same on both connectors, such that identical cables could be used.

The drawing shows the natural position for decoupling capacitors for the biasing. The placement of the digital control lines is also indicated. These digital lines are placed in the bottom routing layer such that they are screened by power and ground from below and above, respectively. The placement of the terminating resistors for these lines is shown in the middle left part. Each line of a differential pair is terminated in each other by a $120\,\Omega$ resistor.

The schematic for the hybrid is drawn on four sheets. As for the test hybrid Viewdraw, the design entry tool from Viewlogic is used. The first sheet shows the chips and the digital control, the next the biasing and the decoupling of the biasing. Sheet 3 shows the test inputs and analog outputs, whereas sheet 4 shows the supply voltages and detector biasing. These four sheets are shown in figures 4.2, 4.3, 4.4 and 4.5.

A description of the schematic follows. On sheet 1 the digital control is shown. The fat tracks indicates that a bus is used. On the FElix the digital controls are BCO, RESETB, T1 and BUSY. On the AMUX the control signals are RBIT, CKL, MRESET and SAMPLE. The RBIT signals are special, and are each terminated by $470\,\Omega$ resistors to DVSS before entering the AMUX named U8 in the schematic. The read-out bit is output again after it has passed through the AMUX on the RBOUT-pins and led to the RBIT-inputs of the next AMUX in the chain, U7. Both lines between the AMUXes are pulled to DVSS by $470\,\Omega$ resistors, as specified by the AMUX designer. All the other differential digital control signals are terminated in each other by a $120\,\Omega$ resistor.

In the layout a digital control differential pair is routed as two close track from the connector to the terminating resistor. On the way the four chips (either FElixes or AMUXes) that need this signal are fed from these lines using short stubs. Short stubs reduce reflection, and the tight tracks reduce pick up effects from this signal pair on other signals. The terminating resistor is placed in the end of the two lines.

Sheet 2 shows the chip biasing and the decoupling capacitors. A discussion between chip designers and the chip testers ended in a list of which biases should be separately provided for each chip, and which signals that could have common biasing. For some of these the decoupling capacitors are on the hybrid, which should be most critical for the voltages. No biases were only decoupled to ground, as for some of the voltages on the test hybrid. The reason for not providing each bias separately, is mainly to reduce the number of signals that one needs to get off the hybrid by means of connectors. The list is given in table 4.1. The AMUX biasing current SFBI was decided to provide separately for each AMUX.

From sheet 3 it is worth noting that only the DTA-signals from the FElixes U1 and

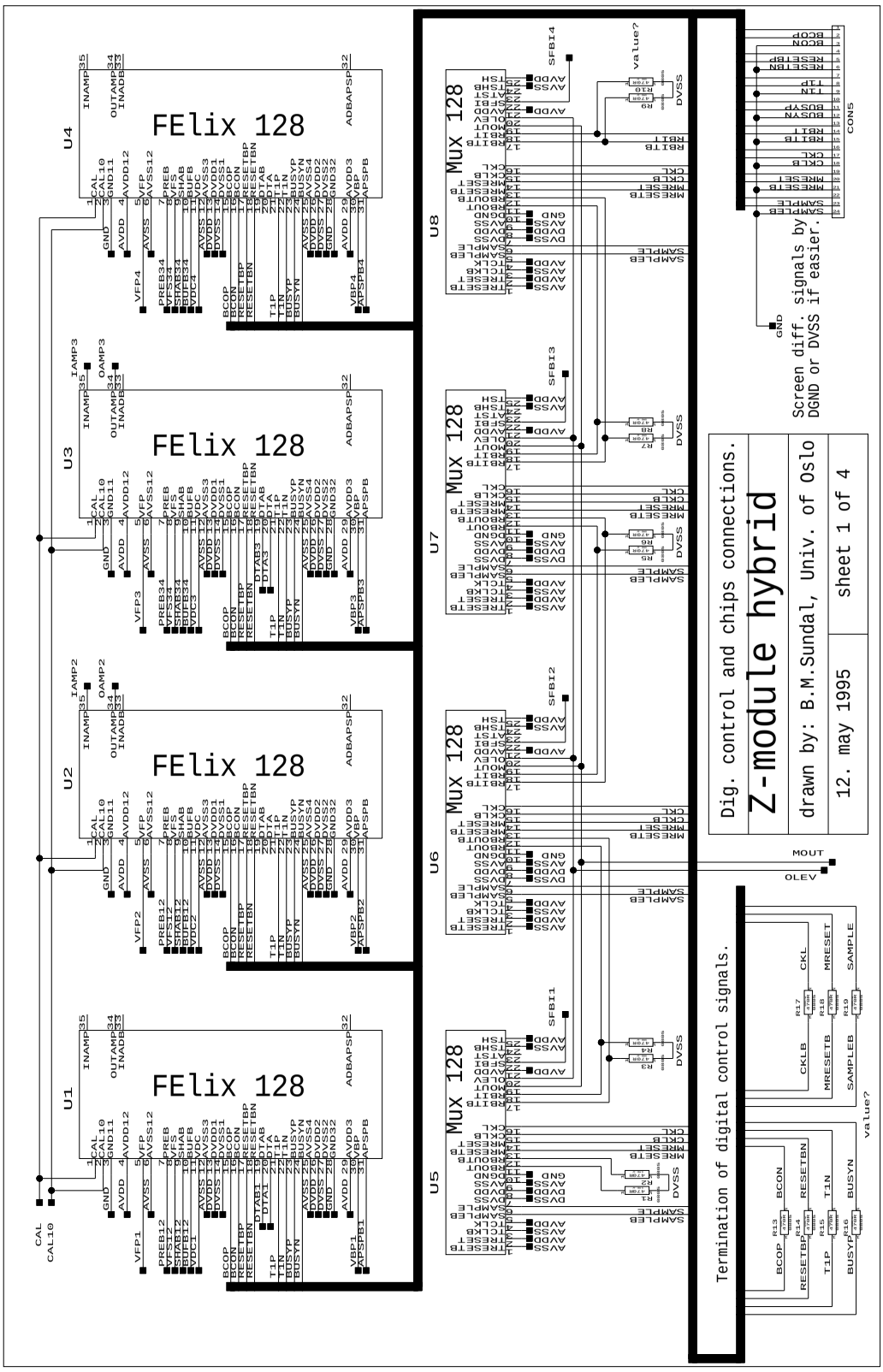

Figure 4.2: Sheet 1 of the Z-module hybrid schematic.

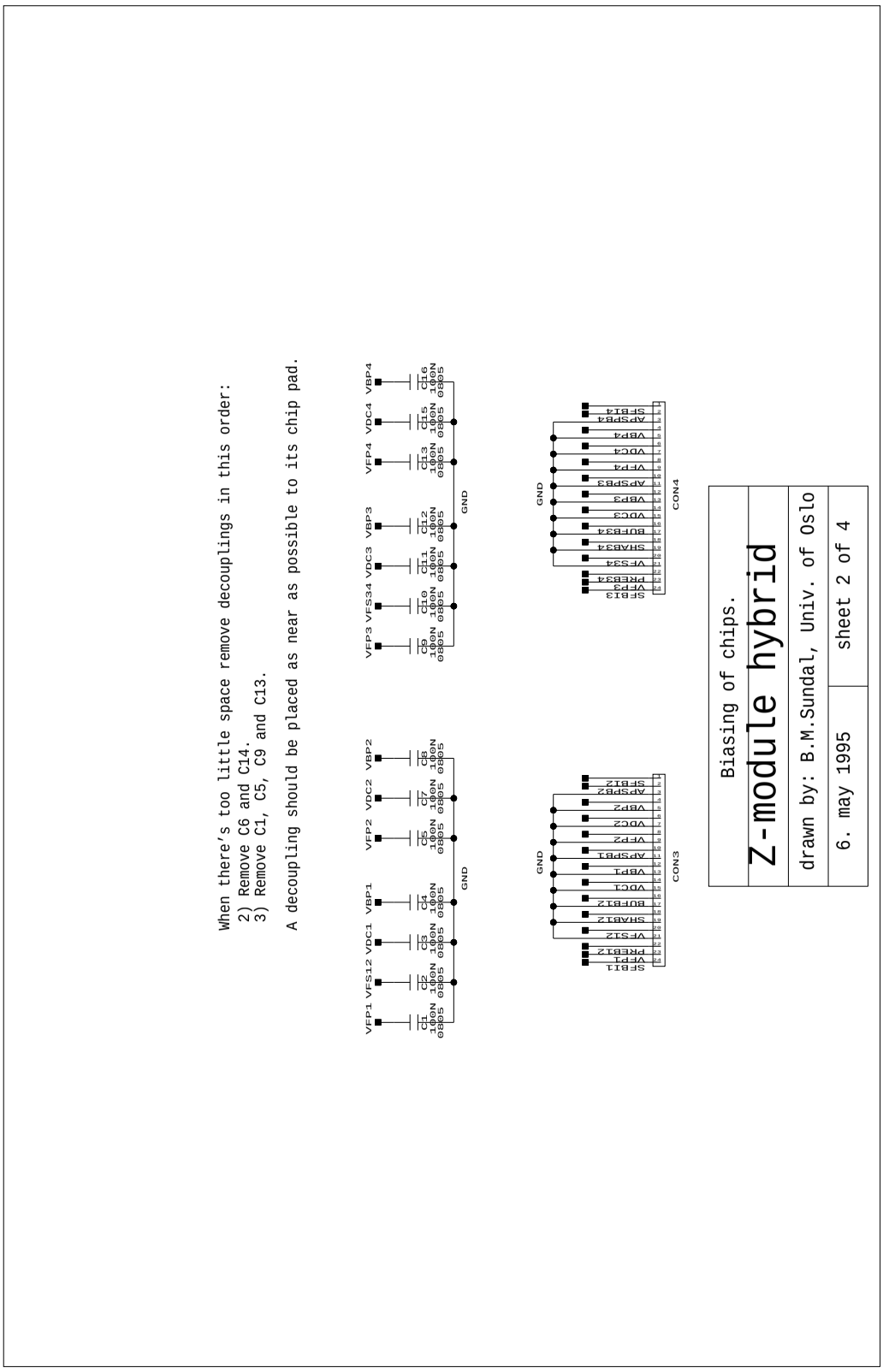

Figure 4.3: Sheet 2 of the Z-module hybrid schematic.

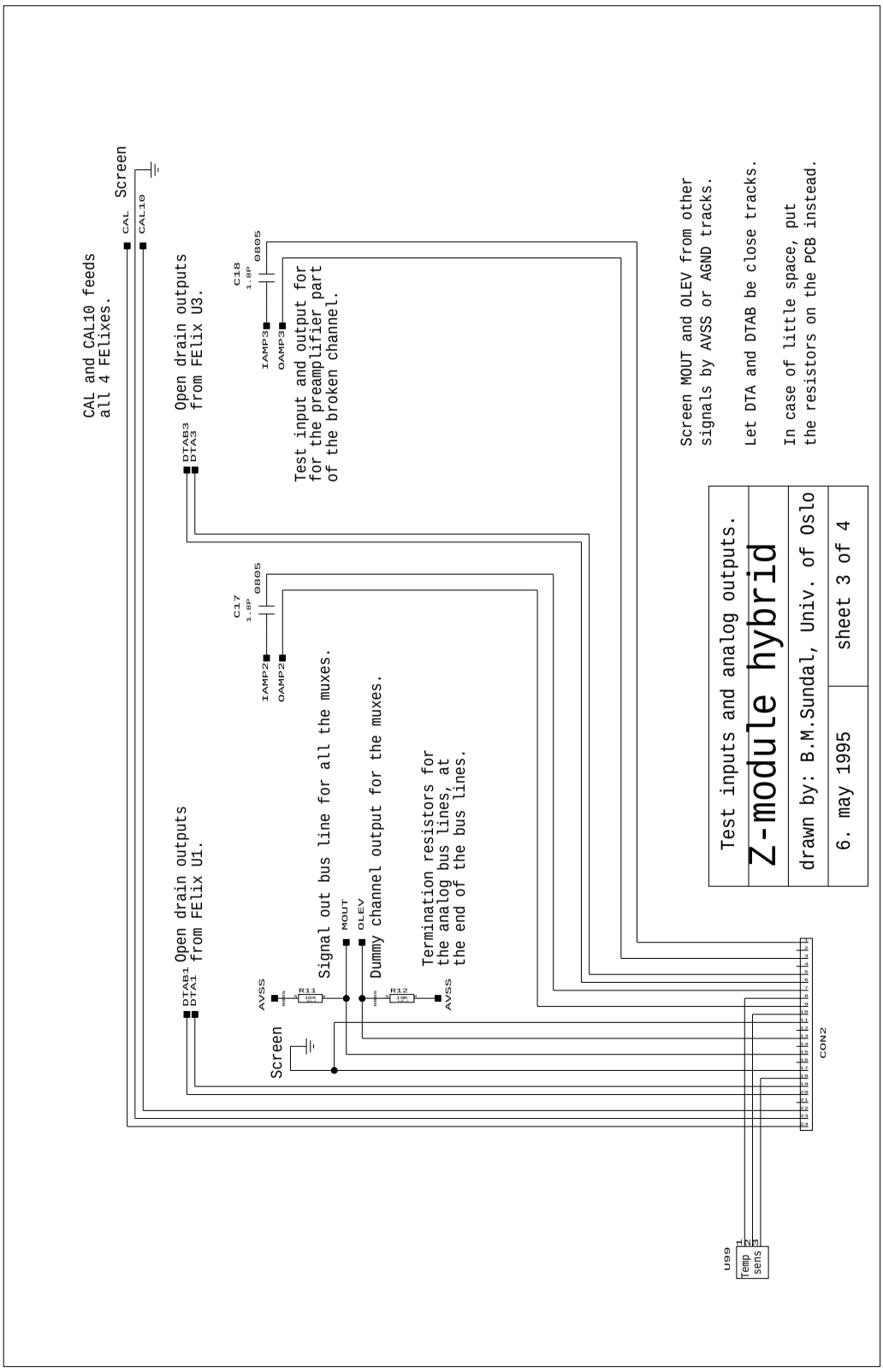

Figure 4.4: Sheet 3 of the Z-module hybrid schematic.

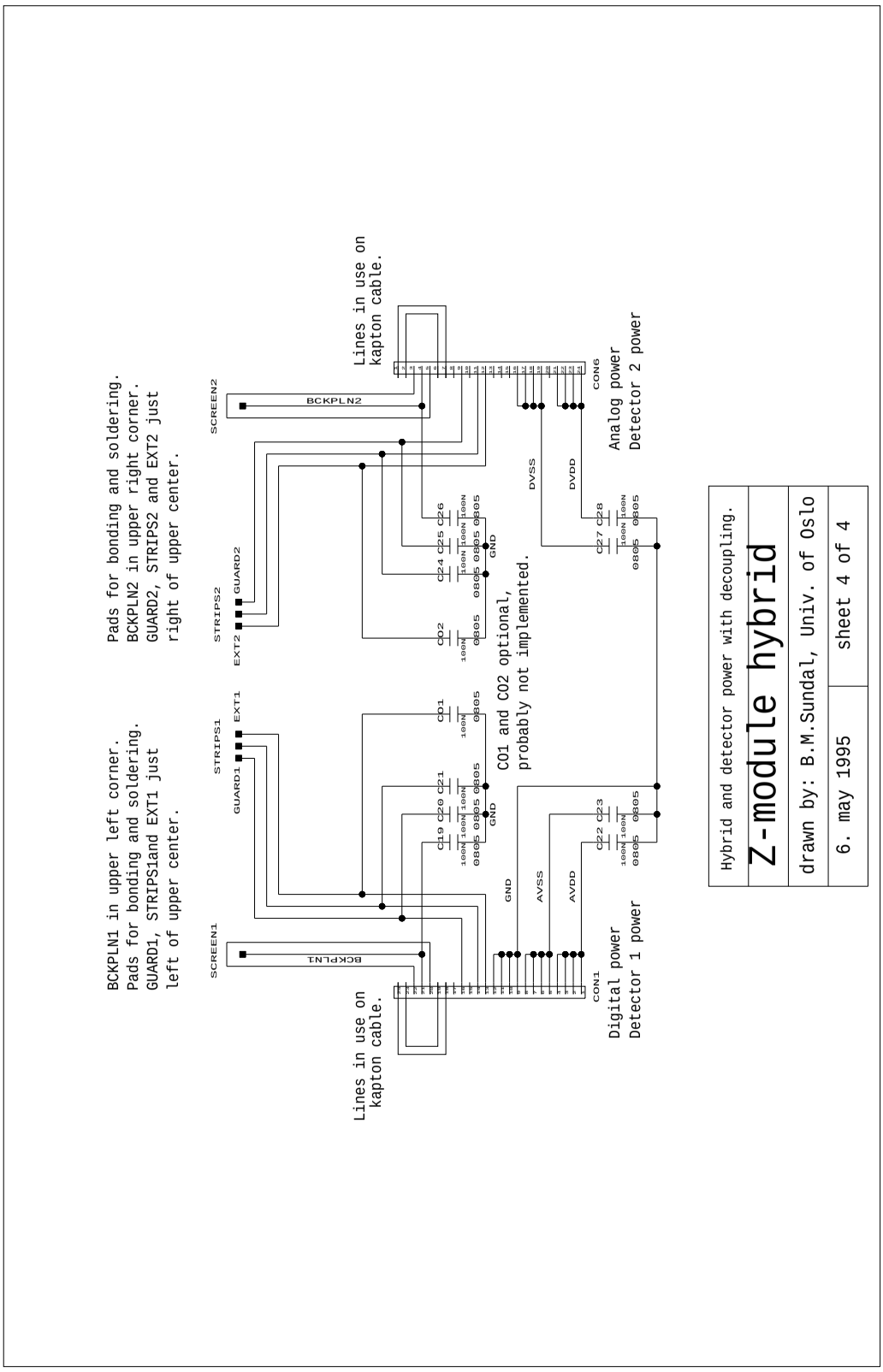

Figure 4.5: Sheet 4 of the Z-module hybrid schematic.

Bias	Implementation
VBP	**Separate.** Decoupling on hybrid.
VDC	**Separate.** Decoupling on hybrid.
VFP	**Separate.** Decoupling on hybrid.
VFS	**Common.** Decoupling on hybrid.
APSPB	**Separate.**
BUFB	**Common.**
PREB	**Common.**
SHAB	**Common.**
SFBI (AMUX)	**Separate.**

Table 4.1: How the biasing is provided on the Z-module hybrid.

U3 are brought out, see also sheet 1 in figure 4.2. This is to save connector pins, and to ease the routing of the hybrid. One also find that the broken channels are only used on FElixes U2 and U3, for the same reason. As on the previous hybrid there are 1.8 pF capacitors on the input to the broken channels. A charge equivalent to a MIP is injected into the broken channel if a 2 mV step is provided to the hybrid. The hybrid is provided with a CAL and a CAL10 line over CON2 and all 4 FElixes are connected to these lines. This system provides a way of injecting an equivalent of a detector pulse to every channel and every tenth channel, respectively. Here the capacitors used on the broken channel are not necessary because they are implemented in the FElix. The analog bus lines from the AMUXes, called MOUT and OLEV for the real AMUX output and the dummy reference channel respectively, are pulled to AVSS by 10 kΩ resistors. There is provided room for a temperature sensor in a SOT23 package. All three pins for this sensor are brought to the connector.

Sheet 4 shows the voltage supplies AVSS, AVDD, DVSS and DVDD. All of these are decoupled to ground. Typically 100 nF ceramic capacitors are used for this purpose. The detectors should be provided with at least three voltages, for the backplane, strips and guard respectively. These tracks should end on the upper edge of the hybrid, facing the detector.

The tracks for the guard and strips end in bond pads midway across the top of the hybrid edge. The backplane for the left detector is in the upper left corner of the hybrid, both a pad for bonding and a pad for soldering are provided. The equivalent is true for the right detector. All detector biases mentioned so far are decoupled to ground. The decoupling for the guards and strips are placed midway on the upper edge, close to the bonding pads to the detector. For the backplanes the decoupling capacitor is near to the connector for this detector.

The tracks EXT1 and EXT2 in the schematic are provided and go along the strip and guard tracks, one for each detector. This track can be used if one wants to use a detector

that needs more than three connections to the outer world. In the schematic these two signals are decoupled with the resistors CO1 and CO2. These capacitors were removed in the layout, in order to reduce the number of components.

A screen is drawn around the backplane signals to indicate that a screen is wanted in the layout. It is important to screen the detector backplane from noisy digital signals.

The screen has an additional function. The backplane can be at a rather high voltage relative to the rest of the voltages on the hybrid. 80 V is typical for non-radiated detectors, but radiated detectors with increased leakage currents may need more than 200 V. Externally this screen can be put on some intermediate voltage, to reduce the risk of breakdown between tracks. The breakdown would probably come on the kapton cables leading to the hybrid. The cables have a breakdown voltage around 100 V.

The bottom of the chips, the chip substrate, should always be connected to AVSS. This is the reason for the big pads for the chips that are seen in the layout. In the schematic this can not be seen. This is because the backplane connection does not have a pin on the FElix or AMUX symbol in the schematic, but is instead assigned to the symbol as an attribute. Such attributes are usually invisible in the schematic, compared to schematic drawings of TTL-chips where the pins for +5 V and ground are omitted. When the design is transfered to the layout program these connections are of course made visible.

4.3 The Z-module hybrid layout and production

On the basis of the layout guidelines and the four sheets of schematic, the design was transferred to the CADSTAR layout tool, and routed at the electronics workshop at the University of Oslo [19]. The layout tool had been prepared for this in advance, incorporating the design rules for the production of thick film hybrids used by Gandhis workshop at CERN. The full layout of a design of this size takes about two weeks.

A list of Gandhis workshops thick film process parameters, with gold as the conducting material as the process settled for, is given in table 4.2. This can be compared to the similar list in table 3.3 describing the AME thick film process.

It is not possible to solder onto the gold, therefore a special layer of a solderable gold alloy material is printed onto the solder pads. These are the pads for connectors, capacitors and resistors. With gold no special actions need to be taken when it comes to bonding. One can bond directly to the gold. Note that the possibilities of soldering and bonding are just the opposite for the silver/palladium process of AME.

The bond pads are not wider than the tracks themselves, which are 100 μm. This small width is only possible through a final processing step known as the Fodel process. Normally tracks and bond pads have a slightly rounded cross-cut, as can be seen from figure 4.6. The Fodel process consists of an etching of the gold tracks in the top conducting layer to make them flatter. The typical cross-cut of a track after this processing is shown in figure 4.6. The bondable width is now much bigger. Without this processing step the typical bond pad width is 200 μm, which would have made it almost impossible to route out all signals from the FElix and AMUX.

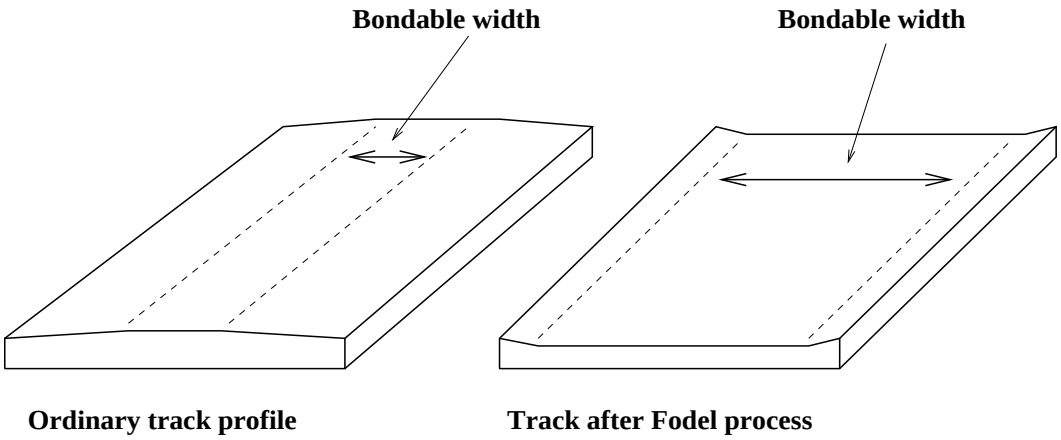

Figure 4.6: Fodel processing of thick film tracks.

Specification	Value
Min. conductor width	100 μm
Min. conductor distance	100μm
Min. via dimension	200μm (diameter)
Min. via pitch	400μm
Bonding pad size	200μm x 400μm
Bonding pad size (Fodel)	100μm x 400μm

Table 4.2: A list of layout design rules from Gandhis workshop.

Note that the typical thickness of a conductor (or power/ground plane) is 8 μm, whereas the approximate thickness of four insulation prints is 50 μm. The reason for using four insulation layers, was to reduce the capacitance between signal tracks and the planes. The AMUXes can not drive a very high capacitive load. When the length of the analog bus lines are around 7 cm and they are sandwiched in between the two planes (ground and power), this could be a problem if the insulation was very thin. Measurements done on the finished hybrids found that the capacitance between an analog bus line and a power/ground was in the area of 30 pF or below, an acceptable value for the AMUXes.

The final result is given in several plots to follow. Figure 4.7 shows the component footprints and their names in scale 2-to-1.

The three following figures named 4.8, 4.9 and 4.10 show the Gerber files Gandhis workshop was provided with.

The Gerber files are all positives, at least if one calls the insulation layers (the ones with black dots for vias) for via-fill layers. This is the same as was done on the prototype hybrid. The via-fill-4 layer is special. This via-fill is never printed, only the inverted mask of it is used to print the fourth insulation layer. It is only about 12 μm thick, so that one does not need to print via-fill. The holes are filled when the next layer with the solder

Figure 4.7: Component placement on the Z-module hybrid.

Bottom layer, power plane.
(**Layer 1**).

First via-fill layer.
(**Via-fill 1**).

Second layer, bottom route.
(**Layer 2**).

Figure 4.8: The three first layers of the Z-module hybrid.

Second via-fill layer.
(**Via-fill 2**).

Third layer, ground plane.
(**Layer 3**).

Third via-fill layer.
(**Via-fill 3**).

Figure 4.9: The three middle layers of the Z-module hybrid.

Fourth layer, top route.
(**Layer 4**).

Fourth via-fill layer.
(**Via-fill 4**).

Solder pad layer.
(**Solder-pad-layer**).

Figure 4.10: The three last layers of the Z-module hybrid.

Print no.	Screen name	Via dimension
1	Layer 1* (power plane)	
2	Insulation 1	200μm x 200μm
3	Insulation 1	200μm x 200μm
4	Insulation 1	200μm x 200μm
5	Insulation 1	200μm x 200μm
6	Via-fill 1*	200μm x 200μm
7	Layer 2* (bottom route)	200μm x 200μm
8	Insulation 2	200μm x 200μm
9	Insulation 2	200μm x 200μm
10	Insulation 2	200μm x 200μm
11	Insulation 2	200μm x 200μm
12	Via-fill 2*	200μm x 200μm
13	Layer 3* (ground plane)	200μm x 200μm
14	Insulation 3	200μm x 200μm
15	Insulation 3	200μm x 200μm
16	Insulation 3	200μm x 200μm
17	Insulation 3	200μm x 200μm
18	Via-fill 3*	200μm x 200μm
19	Layer 4* (top route)	200μm x 200μm
20	Insulation 4**	200μm x 200μm
21	Solder-pad-layer*	

Table 4.3: The different layers printed for the Z-module hybrid.

pads are printed.

The steps of the printing process are shown in table 4.3. The files Gandhis workshop was provided with is marked with a star. The inverted Insulation layer 4 is marked with a double star.

4.4 Hybrid testing and component mounting

The first 12 hybrids were back from production early July. All these were single sided hybrids. Five more hybrids with the same print on both sides of the hybrid were produced in September. These five hybrids were to be used by the Max Planck Institute in Munich to test double sided detectors.

Gandhis workshop is typically a producer of prototype hybrids and PCBs in small series, and hence the yield is not guaranteed. All test hybrids from AME were tested for shorts and other production errors, not so with the Gandhi workshop hybrids.

All testing for shorts and broken tracks on these 12 first hybrids were done at CERN the first week after the production. A check list was made. The physical testing was done with a multi-meter. For all checks that needed contact with bonding pads a probe station was used to avoid ruining the bond pads by the multi-meter probes.

The check list was as follows:

- Check connection of every track from a bond pad to a connector pad.
- Check shorts between all possible combinations of power/power and ground/power.
- Check that the chip pad is connected to AVSS on connector CON1.
- Check shorts of all signals to either power or ground.
- Check resistor and capacitor pad connections to correct signal line.
- Check for cuts in the long tracks between the input connector pad and the terminating resistor pad for digital signals.
- Check for shorts between any pair of neighboring digital tracks.

This extensive list should be enough to pick out most possible errors on the hybrid. The result of the testing was not too encouraging. One hybrid had a broken track. The MRESET pad on the AMUX U8, see figure 4.7 and figure 4.2, was not connected with the MRESET track between terminating resistor and connector. The hybrid was used as a mechanical dummy.

Four hybrids had shorts between power and ground. Two of them between AVSS and ground and the two others between DVDD and ground. The two first and one of the latter were fixed by putting 12 V between the respective power and ground. The 12 V supply was put on a 3 A current limitation. The last hybrid was ruined in this procedure. For the AVSS to ground shorts a spark on the edge of the hybrid was observed in both cases. Maybe the error in this case were that the ground plane printing mask was a bit to big somewhere along the edge. When printed on top of the insulation layers, there could be some paste down along the edge of the insulation layers making contact to the AVSS in the bottom. For the two ground to DVDD shorts the error is suspected to be in the long vias between the bottom power plane and the top electric plane. This via will have to cross the ground plane along its way.

In total, after repair, we were left with 10 good hybrids out of 12, which must be characterized as a reasonable yield. Six of these hybrids were equipped with components at the assembly workshop at CERN.

By mid of July the initial testing of the FElix128 was finished. The FElix128 seemed to function, after a few initial problems.

Three of the hybrids were equipped with one FElix and two AMUXes each. The chips were glued to their big AVSS pad by conducting glue. It was decided not to put on more chips before it could be verified that the hybrid would work with only one FElix. From the

schematic and layout these were the chips named U3, U7 and U8. The FElix was placed at U3, since this one has its DTA brought out, and is connected to a broken channel input. Since the AMUXes daisy-chain the read-out bit, AMUX U8 is needed to bring the read-out bit to U7, which is connected to the FElix.

The bonding is straightforward. The 129 outputs from the FElix, that is the 128 full channels plus the broken channel, are bonded one-to-one to the 129 AMUX input channels. The full channels are bonded to the 128 AMUX inputs, whereas the broken channel is bonded to the AMUX reference channel. The bonding from the AMUX to the hybrid is a simple one-to-one bonding. For the FElix to hybrid most bondings are one-to-one. Four of the pads are however a bit wider than the others. This is because on the chip two neighboring pads are the same supply voltage. Then these two chip pads are bonded with a bond wire each to the same wide hybrid bond pad. This is shown in figure 4.11.

In the schematic the symbol of the FElix reflects its function on the hybrid. This means that in the schematic the FElix symbol has as many pins as there are FElix pads on the hybrid. A description of all pads are given in tables in appendix B.

4.5 Testing of the hybrid in a lab setup

During the middle of September, the hybrid was working in a lab setup at CERN for the first time.

The setup was similar to the test hybrid setup in figure 3.22. The charge injection board was not used, only the CAL and CAL10 signals. The hybrid was equipped with two AMUXes and one FElix.

Outputs were found both in de-convoluted and peak mode. The sequence used for peak mode is shown in figure 4.12. It contains two groups of 128 AMUX clock cycles (CKL), which are marked with crosses in the figure. The first 128 cycles clocks the read bit through the first MUX, so that it is in the first channel of MUX bonded to the FElix when it outputs data. In this way the APSP can be seen working. The sequence for the de-convoluted mode looks almost exactly the same, the only difference is that the positive part of SAMPLE is extended 800ns so that the sampling continues until the de-convoluted value lies on the APSP-outputs.

The values used for the different biases were, VFP $= -0.2\,\mathrm{V}$, VFS $= 0.33\,\mathrm{V}$, VDC $= -0.85\,\mathrm{V}$ and VBP $= -1.0\,\mathrm{V}$ for the voltages, and PREB $= 700\,\mu\mathrm{A}$, SHAB $= 300\,\mu\mathrm{A}$, BUFB $= 80\,\mu\mathrm{A}$, APSPB $= 24\,\mu\mathrm{A}$ and SFBI $= 73\,\mu\mathrm{A}$ for the currents. The voltage supplies were $-2.02\,\mathrm{V}$ and $+2.06\,\mathrm{V}$.

The figures 4.13, 4.15 and 4.14 show printings from the oscilloscope. Figure 4.13 shows two traces. The upper one is the DTA. One sees three groups of DTAs. The reason is that the T1 is high for several BCO-cycles, and the FElix then believes it receives several triggers. A good proof that the trigger logic of the FElix is level triggered and not edge triggered. The lower trace is the AMUX output for the FElix in peak mode. This output looks rather chaotic in the beginning (first $20\,\mu\mathrm{s}$). The read-out bit is in the first AMUX channel, so we see the time continuous output from the APSP of the first channel. The

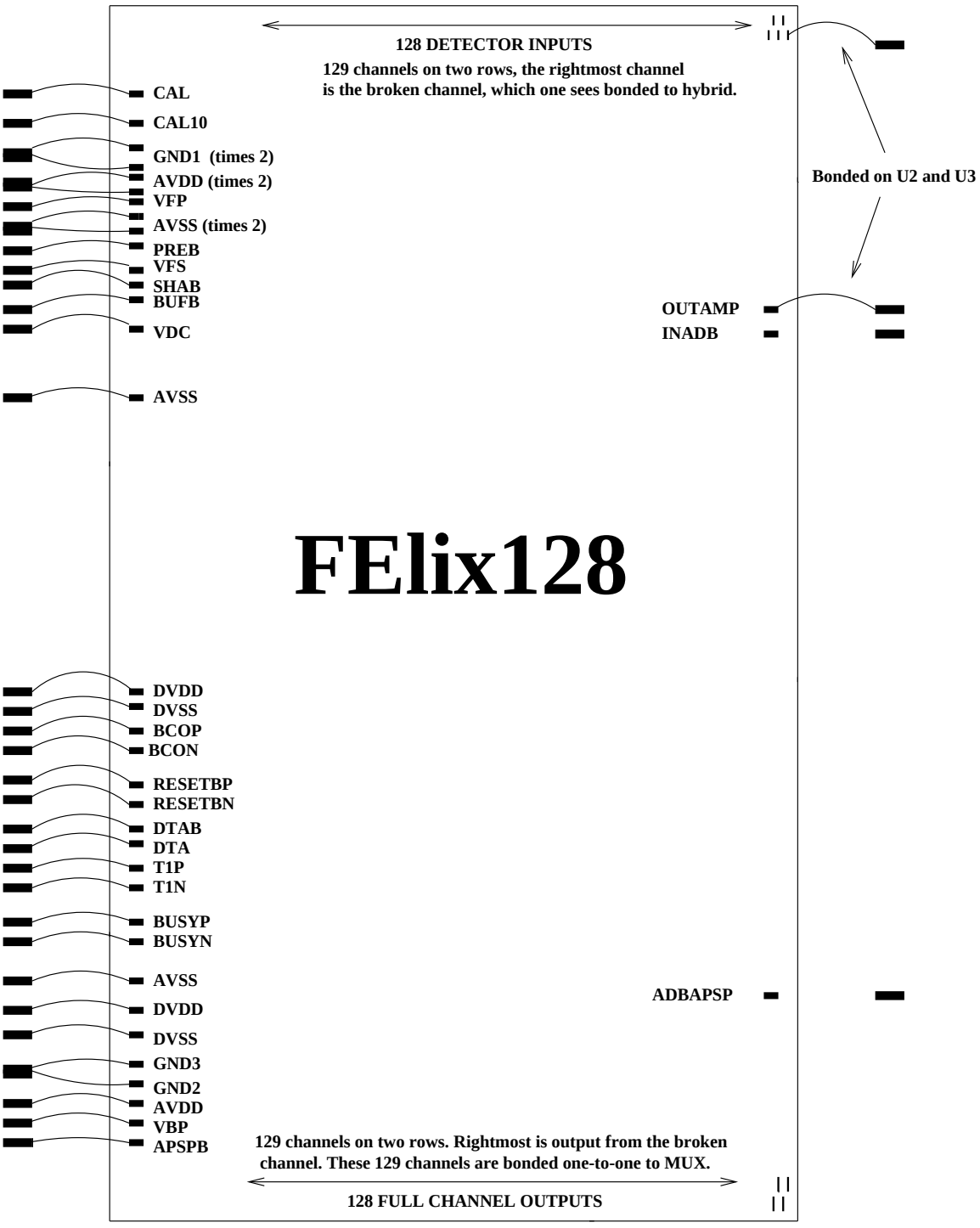

Figure 4.11: Bond map for FElix128 on Z-module hybrid.

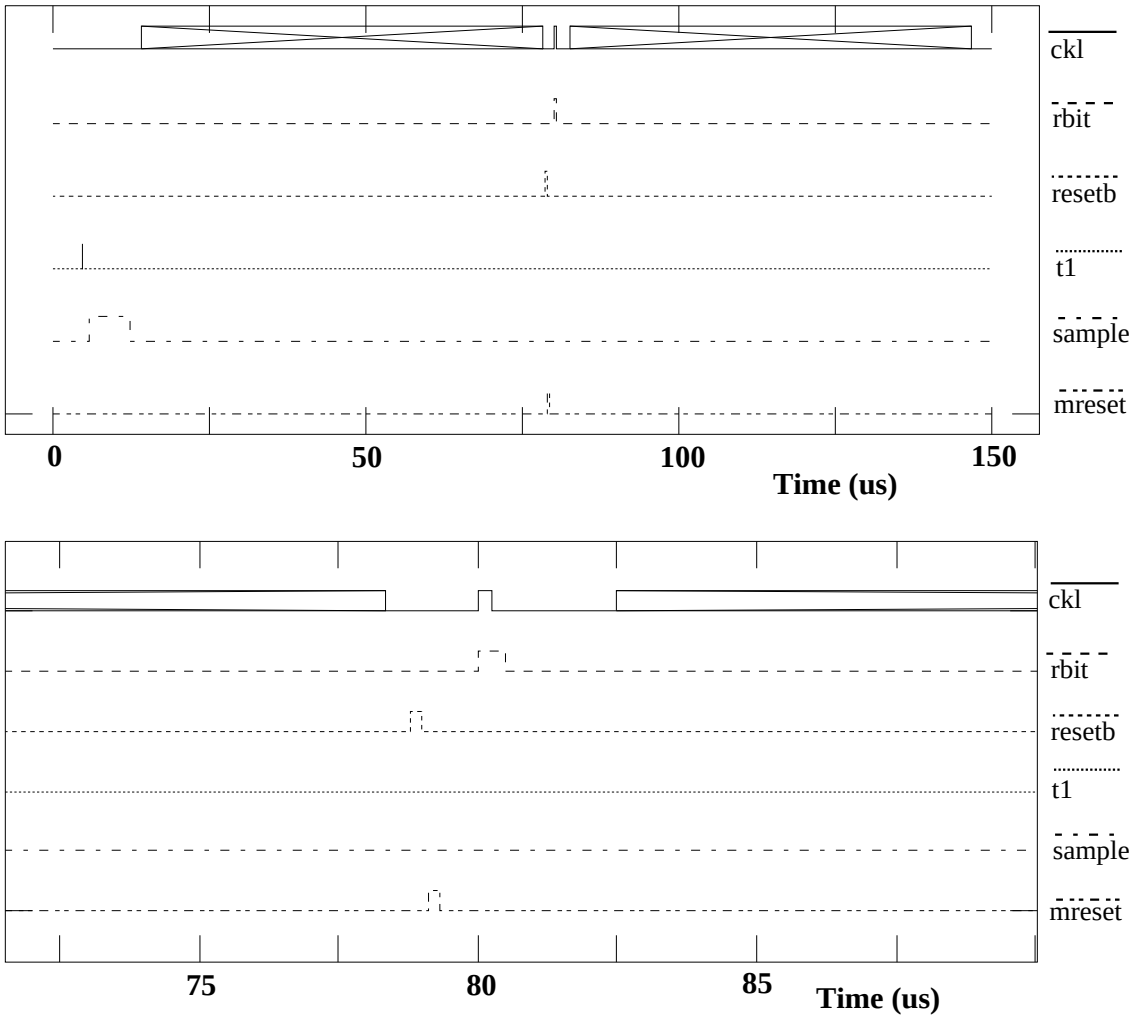

Figure 4.12: The sequence for test of hybrid with one FElix and 2 AMUXes.

Figure 4.13: Oscilloscope printout for AMUX output and DTA of FElix128 in peak mode. The test is performed on the Z-module hybrid.

Figure 4.14: Oscilloscope printout for AMUX output with FElix128 in de-convoluted mode.

Figure 4.15: Oscilloscope printout for AMUX output in de-convoluted mode. Only around 30 AMUX channels are shown.

chaotic mess is the APSP working on building the de-convoluted value and then outputting the peak value. Then the MUX starts holding this value, before it outputs this hold value from all 128 channels.

The FElix is excited with the CAL10, so a signal in every tenth channel is seen. The negative amplitude of the channels which have a signal, is approximately 90 mV. The input to CAL10 is a 0.14 V step, which should be equivalent to 2 MIP. The amplitude of the real APSP signal should be around 80 mV if one takes into account that the gain of the AMUX is approximately 0.75 and the gain of the support PCB for this hybrid is about 1.5. The pedestal levels for the channels without a signal drops a bit with the channel number. The last channels lying on a DC-level about 60 mV lower than the first channels. Such pedestal variations creates no problem since they can be corrected offline.

By moving the delay of the CAL10 and observing how the amplitude of the every tenth channel excited varied, a picture of the pre-amp/shaper output could be drawn. This technique was explained in the test hybrid section. Amplitudes from the oscilloscope screen were measured and are shown in figure 4.16. It can be compared with figure 3.25 found in the test hybrid section. The figure clearly indicates that the biasing is not optimally adjusted. The peaking time is too short, and the peak is too flat and too long. There is also an undershoot. The whole undershoot is not seen because it was not possible to set the pulse generator delay below 65 ns.

Figure 4.14 shows a figure similar to 4.13. The input is still a charge equivalent to 2 MIP, but this time in the de-convoluted mode. It is observed that the channels with a

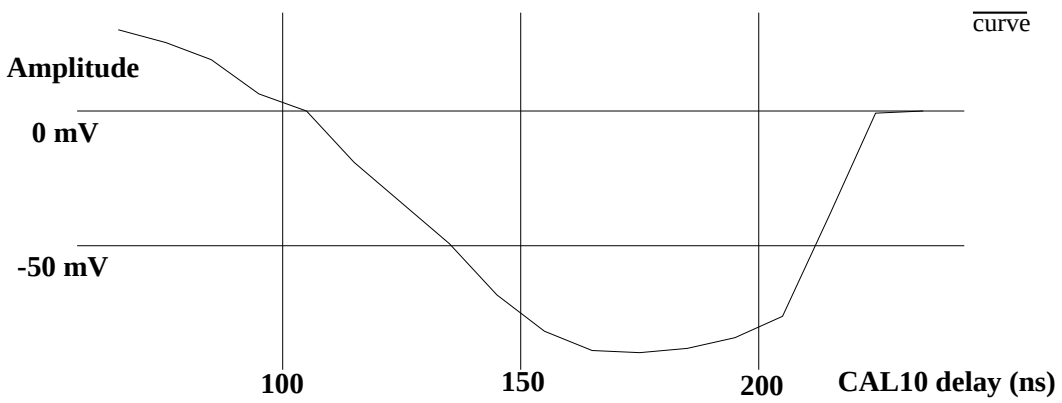

Figure 4.16: Amplitude of excited AMUX channels as function of CAL10 delay. The FElix in peak mode.

signal now have positive amplitudes around 120 mV. For both figures it applies that the timing of the CAL10 pulse was adjusted to give the highest possible amplitude. Figure 4.15 shows the same as figure 4.14 but with a closer look at the first few channels. Here the APSP output is seen in more detail. From the output one sees three channels exited by CAL10. For the channels in between one clearly observes that each channel lies on its own specific DC-level, its pedestal. The AMUX read-out clock frequency was 2 MHz so four channels are output for each 1 cm (the grid) of the oscilloscope screen.

As for peak mode, the delay was varied. The result is shown in figure 4.17. This can be compared to the ideal shape shown in figure 3.27 ($x = 1/3$). Figure 3.27 must be watched from right to left, to do the comparison. Figure 3.26 can be compared directly to figure 4.17. The former figure was made for a Felix on a simple PCB and with an automated Labview setup.

Figure 4.18 shows the output of the broken channel, OAMP3, when the FElix was excited with a 4 MIP equivalent charge in CAL. The biasing is as before, but VFS is lowered to 0.16 V and SHAB lowered to 200 μA. The waveform is not ideal, since the peaking time is too short. From the figure the peaking time is 50 ns instead of the required 75 ns. The change of the SHAB in conjunction with the change of the VFS got rid of the flat peak and the undershoot. The broken channel output cannot however be fully trusted because of long lines on hybrid and PCB which gives a big capacitive load and maybe some distortion of the signal. It is usual to see an undershoot in the full channel even when the broken channel output has the perfect shape.

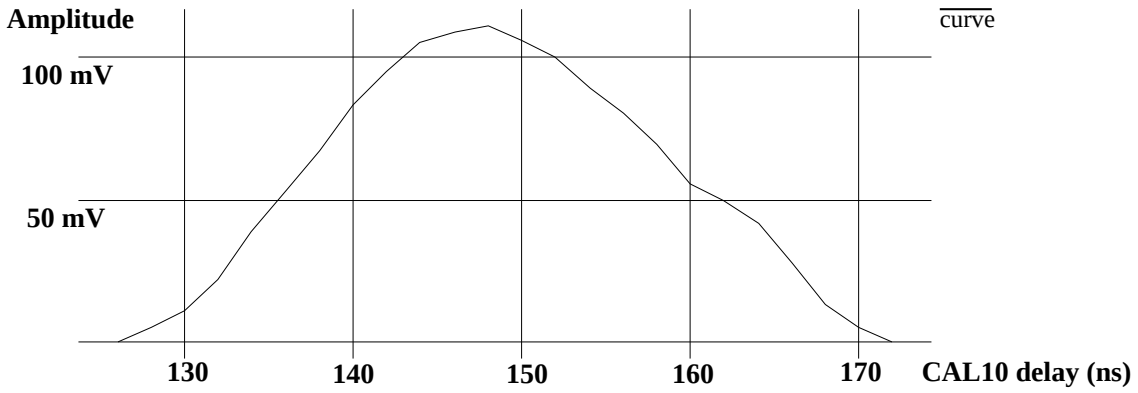

Figure 4.17: Amplitude of excited AMUX channels as function of CAL10 delay. The FElix in de-convoluted mode.

Figure 4.18: Broken channel pre-amp/shaper output of FElix on Z-module hybrid.

4.6 The future for the Z-module hybrid

A lot of testing of this module is needed in the future. The hybrid equipped with more FElixes and AMUXES does already work with CAL10 in a lab situation. Detectors and fan-ins will be put on to obtain a full (single sided) Z-module.

There are several interesting features of the FElix128 Z-module that need to be tested. The first and most important thing is that the analog performance must be good, the signal-to-noise must be kept better than 15-to-1 in de-convoluted mode.

A signal-to-noise of 17-to-1 in de-convoluted and 32-to-1 in peak mode were measured for the FElix128, on a simple PCB with one chip, during the September H8 test beam. These results only indicates the FElix' performance.

The following questions need to be answered:

- How does the fan-ins affect the signal-to-noise? For the test PCBs in the test beam the FElix is bonded directly to the detector. And how will the the signal-to-noise vary along the channels, because of the big difference of track length on the fan-in for detector strips in the lower left and upper right corners of the two detectors bonded together?
- How does a FElix behave on a hybrid occupied by several other FElixes and AMUXes?
- When detectors are radiated to levels near the equivalent of 10 years of LHC operation, how will this affect the signal-to-noise?
- The FElix produced by AMS is not radiation hard. How will the chip behave when made in a radiation hard technology?

The list could be much longer. The future will show if the Z-module solution with full analog read-out by FElix successors can reach the signal-to-noise specifications. Other modules, using digital, binary or analog read-out, might nevertheless outperform these results, and end up as the modules used in the inner detector of ATLAS.

The FElix will at least survive for one more year. A new version incorporating a MUX working at 40 MHz is being constructed. This will bring it closer to a final read-out chip. 128 channels can then be output in 3.2 μs. Two and two chips will form a group which will have to output its data in a maximum of 10 μs, since this is the maximum average time between T1s.

Even one more FElix is being planned within the next year. Here the wish is to incorporate bias generators internal to the chip. Commands on a bit serial form can be sent to the chip telling it the values for the biasing voltages and currents. Commands that tell the chip to send back information about its state are also needed. All this is part of the control and monitoring functions that will be needed in the future.

For each of these FElix iterations, new hybrids will be needed. Hopefully these will resemble more and more a final hybrid.

Chapter 5

The effect of hybrids on traversing particles

In the introduction it was explained that the inner detector would need to have as little mass as possible, in order not to distort the trajectory of the particles too much. The two effects to be considered are the energy loss and the path deviation, which manifests themselves through physical effects such as bremsstrahlung, pair-production, ionization and multiple Coulomb scattering. The understanding of these effects is vital to the effort of minimizing the disturbance of the particle trajectory.

5.1 Stopping of particles in matter

The most important energy loss mechanism for relativistic particles in most materials is ionization. This is not true for electrons where bremsstrahlung dominates above some 10 to 20 MeV.

Together with the electron, the energetic photon will also be covered, since these are related through electromagnetic showering. The energetic photon produces a pair of electrons, and again the electrons produce photons by bremsstrahlung.

5.1.1 Radiation length and energy loss of electrons

Too much material in the inner detector gives rise to several problems when it comes to identification and momentum measurements of electrons. Photons converting into electrons and positrons give fake tracks, which make room for uncertainties. Energy loss of electrons by bremsstrahlung degrades the electromagnetic calorimeter performance, which is bad for the measurements of E and p. This is discussed in [11].

When measuring the thickness of materials with respect to penetration of electrons, the radiation length X_0 is a useful quantity. It is defined as the distance over which a high energy electron looses $1/e$ of its energy by bremsstrahlung. This can be expressed [8,

chapter 10] by the formula

$$E(x) = E_0 \exp(-x/X_0), \tag{5.1}$$

where $E(x)$ is the electron energy after traversing a distance x of the media. E_0 is the initial energy, and X_0 is measured in the same units of length as x.

This formula is valid for electrons of energies higher than the critical energy, E_c. For solids this energy is approximately given by the empirical formula [8, chapter 10]

$$E_c = \frac{800MeV}{Z + 1.2} \tag{5.2}$$

where Z is the atomic number of the medium traversed. This is the energy where the radiation loss by bremsstrahlung, which grows linear with energy, crosses the ionization loss, which grows logarithmically.

For a given media X_0 is tabulated in units of g/cm^2. If it is divided by the density, ρ (g/cm^3) of the media it is given in cm [8, chapter 10],

$$X_{0,cm} = \frac{X_{0,g/cm^2}}{\rho}. \tag{5.3}$$

The $X_{0,g/cm^2}$ for the elements is given by the empirical formula [8, chapter 10]

$$X_{0,g/cm^2} = \frac{716.4\text{g/cm}^2\,\text{A}}{\text{Z}(\text{Z}+1)\ln\left(287/\sqrt{\text{Z}}\right)}, \tag{5.4}$$

where A is the atomic mass in g/mol and Z is the atomic number. This formula is correct to 2.5% for all elements except helium.

In a compound of elements the radiation length can be found to a good approximation by [8, chapter 10]

$$1/X_0 = \sum_{i=1}^{N} \omega_i / X_{0,i}, \tag{5.5}$$

where ω_i and $X_{0,i}$ are the fraction of mass and the radiation length (g/cm^2) of the i'th element.

In a detector or hybrid, it is customary to give the thickness of it as a fraction of a radiation length,

$$t = T_{material}/X_{0,cm}, \tag{5.6}$$

where $T_{material}$ is the thickness of the material in centimeters. Multiplying t by 100% gives the thickness of the material as a percentage of a radiation length. For a whole system of detectors the total thickness in radiation lengths is found by summing the percentage contribution from each part.

High energy electrons and photons produce electromagnetic showers in matter. An electron emits bremsstrahlung after a typical length of X_0, and produces a photon. This photon, or another energetic photon incident on the media will later form an electron-positron pair by pair production. The typical length a photon will traverse before pair production is $\frac{7}{9}X_0$ [8, chapter 10].

5.1.2 Energy loss by ionization in matter

For relativistic charged particles other than electrons, the dominating energy loss is caused by ionization. This loss has its minimum around $\beta \approx 0.96$, corresponding to $\beta\gamma \approx 3.5$. β and γ are the relativistic quantities $\beta = v/c$ and $\gamma = 1/\sqrt{1-\beta^2}$, where v is the particle speed and c the speed of light.

At this broad minima, the particle is called a minimum ionizing particle, MIP, and the energy loss grows very slowly (logarithmically) with energy after this minima.

If $\frac{-dE}{dx}$ for a particle is normalized with the density, ρ (g/cm^3), of the media we get the mass stopping power $\frac{-dE}{\rho dx}$. This quantity is given by the Bethe-Bloch equation [8, chapter 10].

To a first approximation the mass stopping power is independent of the media the particle traverse, as long as the particle is a MIP or higher in energy. The value is given by

$$\frac{-dE}{\rho dx} \approx 2\,\mathrm{MeV\,cm^2/g}. \tag{5.7}$$

In reality one should rather write $\frac{-dE}{\rho dx} \approx (2 \pm 1)\,\mathrm{MeV\,cm^2/g}$. MIPs have between 1 and $2\,\mathrm{MeV\,cm^2/g}$ when they traverse a media (except liquid H_2 as a media, which give $4\,\mathrm{MeV\,cm^2/g}$). The value 1 is for the heaviest media, like lead, and $2\,\mathrm{MeV\,cm^2/g}$ is for the lightest media, like helium. These values grow slowly with the energy and reach the interval 2 to $3\,\mathrm{MeV\,cm^2/g}$ for $\beta\gamma \approx 10000$, which is ultra-relativistic. See figure 5.1 for some graphs of the Bethe-Bloch equation.

A proton need a momentum around 10 TeV/c, which can be compared to its rest mass of about 1 GeV, to reach this value of $\beta\gamma$. At even higher $\beta\gamma$, bremsstrahlung starts to play a role even for these particles. For muons the radiative effects come into considerations a bit earlier, that is for $\beta\gamma$ around a few thousand. For LHC, with center of mass energy at 14 TeV, the radiative effects should not be an important concern.

5.2 Path deviation by Multiple Coulomb scattering

Vertex finding is vital to B-physics, where the track momenta is in the order of a few GeV. Since Coulomb scattering starts to play a role for track momenta below 50 GeV, and this scattering scales with the radiation length, one understands that the inner part of the inner detector should have as little mass as possible. Whenever possible material should be placed at larger radii [12].

A charged particle experiences scatters off the nuclei in the medium it is traversing. For small angle scattering, the angle can be fitted to a Gaussian distribution, with the approximated width of [8, chapter 10]

$$\theta_0 \approx \frac{13.6\,\mathrm{MeV}}{\beta \mathrm{cp}} Z\sqrt{t}(1 + 0.038 \ln t), \tag{5.8}$$

where p denotes the momentum and Z the charge number of the particle, and t is the thickness of the medium in parts of radiation lengths.

Energy loss by ionization for particles through matter.

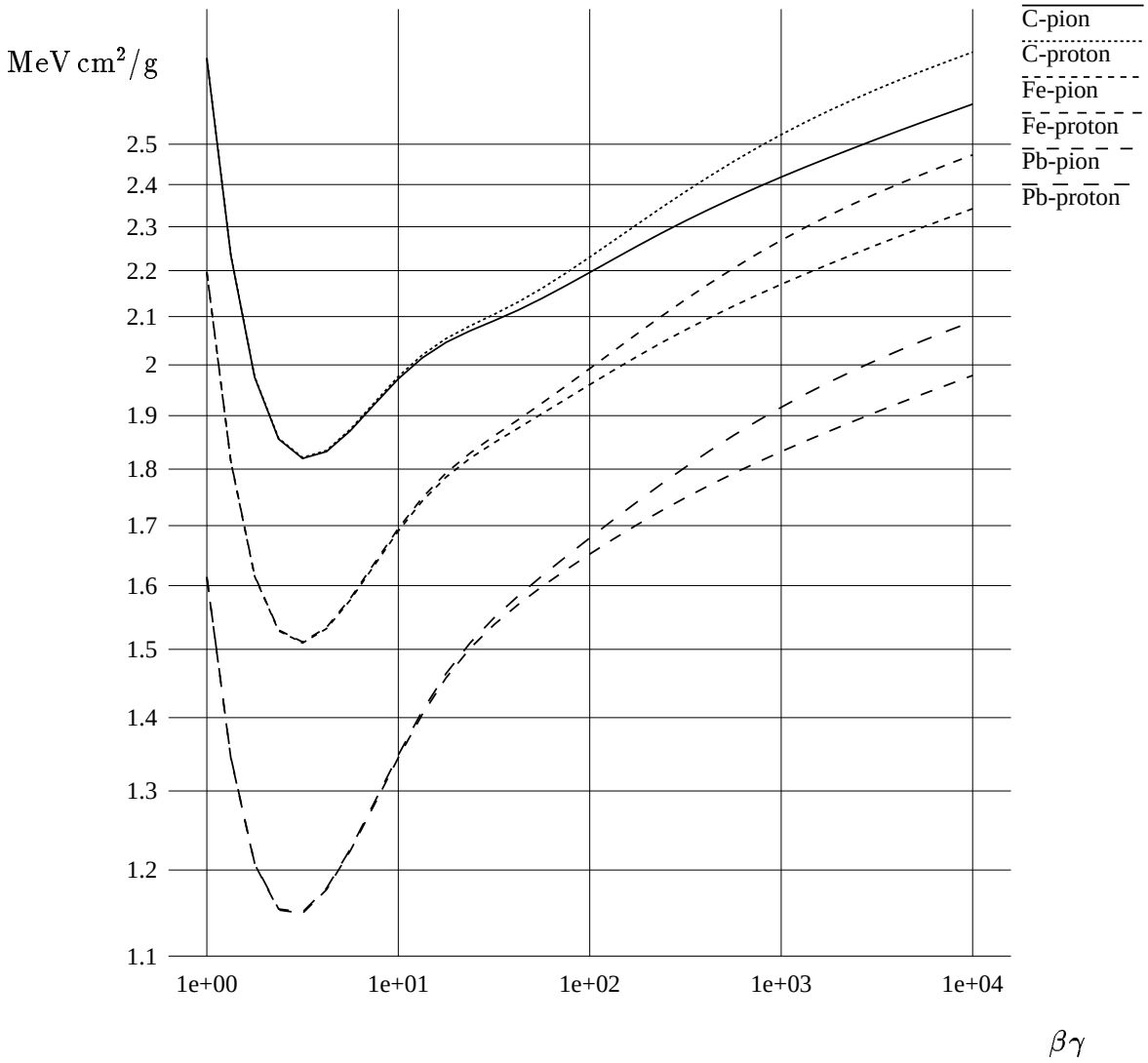

Figure 5.1: The Bethe-Bloch equation for pion and proton projectiles on lead (Pb), iron (Fe) and carbon (C) targets.

Bremsstrahlung characterized by t has nothing to do with the Coulomb scattering. The radiation length is only used in this formula because it provides a convenient way of scaling the results, whereas the physics itself in the above formula lie in the Z (charge) and the βcp (kinematic). The accuracy of the formula is in the area of 10% for single charged particles ($Z = 1$) with $1/1000 < t < 100$.

The formula for multiple Coulomb scattering is not in a form that allows us to sum the contributions from different parts that the particle is traversing. However since θ_0 is a Gaussian width, the individual contributions can be root mean squared.

Simplification of formula 5.8 to get a a crude estimate of the scattering angle is possible. If the thickness, t, is in the order of 0.01, the parenthesis term can be evaluated once and combined with the 13.6 MeV constant to form a new 'constant', E_{norm}, which is approximately 11 MeV. The term βcp can be expressed in terms of the particle energy and is equal to $\beta^2 E$ by using the relativistic formulas $E = pc$ and $\gamma = 1/\sqrt{1-\beta^2}$.

A combination of these simplifications gives the formula

$$\theta_0^2 \approx \frac{Z^2 E_{norm}^2}{\beta^4 E^2} t. \tag{5.9}$$

The formula is now linear in t. If one has found the total radiation thickness t_{TOT} of the hybrid by adding individual contributions, the square width of the total multiple Coulomb scattering is proportional to this thickness,

$$\theta_{0,TOT}^2 \approx \frac{E_{norm}^2}{\beta^4 E^2} t_{TOT}, \tag{5.10}$$

in the case of single charged particles. This estimate should not be trusted to more than 30% accuracy, but should be good enough to estimate the effect of multiple Coulomb scattering.

5.3 An estimate of X_0 for standard thick film hybrids

Table 5.1 contains data for some important elements used in thick film production. These values are found in [8, pages 224–226]. For the elements where measured values could not be found, formula 5.4 was used. In the calculated values for the compounds in table 5.2, by means of formula 5.5, measured values of X_0 were used wherever possible.

Ceramic substrates have a standard thickness of 0.635 mm = 0.0635 cm, found to be correct for the hybrids produced. The percentage values for radiation length of beryllia and alumina is then $t_{BeO} = 0.44\%$ and $t_{Al_2O_3} = 0.84\%$ from formula 5.6 and table 5.2.

Beryllia (BeO) has almost half the radiation length of alumina (Al_2O_3). Beryllia also has a much higher specific thermal conductivity than alumina, 2.1 $\frac{\mathrm{W}}{\mathrm{Kcm}}$ compared to 0.35 $\frac{\mathrm{W}}{\mathrm{Kcm}}$. This can also be compared to silicon, which has 1.45 $\frac{\mathrm{W}}{\mathrm{Kcm}}$. Further good properties of beryllia is a thermal expansion coefficient of 6.1 ppm/K, closer to silicons 4.2 ppm/K than aluminas 6.4 ppm/K.

Element	**Atomic no. Z**	**Atomic mass A, g/mol**	**Density g/cm^3**	X_0 **g/cm^2**	X_0 **cm**
Beryllium, Be	4	9.012	1.85	65.19 (meas.)	35.2
Boron, B	5	10.81	≈2.35	53.17 (calc.)	≈22.6
Oxygen, O	8	16.00	(gas)	34.24 (meas.)	(gas)
Aluminum, Al	13	26.98	2.70	24.01 (meas.)	8.89
Silicon, Si	14	28.09	2.33	21.82 (meas.)	9.36
Copper, Cu	29	63.55	8.96	12.86 (meas.)	1.43
Zinc, Zn	30	65.39	7.14	12.72 (calc.)	1.78
Palladium, Pd	46	106.4	12.0	9.42 (calc.)	0.78
Silver, Ag	47	107.9	10.5	9.17 (calc.)	0.87
Cadmium, Cd	48	112.4	8.64	9.19 (calc.)	1.06
Barium, Ba	56	137.3	3.51	8.45 (calc.)	2.41
Gold, Au	79	197.0	19.3	6.43 (calc.)	0.33

Table 5.1: Radiation lengths for various elements used in the production of thick film hybrids.

Compound	**Density, d (g/cm3)**	X_0 **(g/cm^2)**	X_0 **(cm)**
Beryllia, BeO	3.01	41.3	13.7
Beryllia, ceramic	2.86	41.3	14.4
Alumina, Al_2O_3	3.97	27.9	7.03
Alumina, ceramic	≈3.7	27.9	≈7.5
BaO	5.72	9.17	1.60
BaO_2	4.96	9.85	1.98
B_2O_3 (glass)	1.81	38.5	21.3
CdO (2 types)	≈7.5	10.1	≈1.3
SiO_2	≈2.2	27.0	≈12
ZnO	5.61	14.5	2.59

Table 5.2: Calculated radiation lengths in both cm and g/cm^2 for various compounds used in the production of thick film hybrids.The values for X_0 can not be trusted to more than about 5%. The values are given by more digits than this should indicate, but only since the values are used in further calculations

Component	Weight % in paste	Weight % after firing	Thickness % after firing	Rad.length (cm)
Au	80-90	≈98	≈94	≈0.33
CdO (binder)	2	≈2	≈6	≈1.3

Table 5.3: Composition of a paste for conductors. This is typical values for gold paste used at Gandhis' workshop at CERN. Missing percentages in the first column are solvent that evaporate during firing.

Beryllia substrates are not as usual as alumina, because they are poisonous. A bare substrate can easily contribute to 30% of the total hybrid cost [18], whereas for alumina this cost is much less. But the advantages are so important in terms of radiation length and thermal conductivity that it has to be used.

For the printing process used by Gandhis workshop on the Z-module hybrid, the conducting material is gold. Other common conductors are silver, and often silver and gold in alloys with palladium or platinum [9, chapter 8].

For the mixture of two typical pastes used for printing of conductors and insulation, see table 5.3 and table 5.4 [18]. The percentages by weight of the active ingredients are given in the first column. The second column, the percentage of weight after firing, is obtained by normalizing the first column to a total of 100%. From the second column, the percentages of thickness in a fired layer is calculated, being the important numbers in following calculations. This is done by dividing each entry in the second column by its density. The result is then normalized to give 100% total. The percentage of volume and thickness is the same as long as the area is the same.

The contents of the paste can mostly be divided into three parts [9].

- **Solvent:** It gives the paste its viscosity, so that it is suitable for screen printing. It evaporates during the firing of the layer.
- **Binder:** Typical glass particles (silicon oxides).
- **Functional element:** For conductors this is the metal, and for dielectric it is oxides, which gives the wanted dielectric constant. (As small as possible for insulators).

An estimate for the radiation thickness of a conducting layer and an insulating layer is then easily calculated from tables 5.3 and 5.4. If p_T^i is the relative thickness for the i'th element/compound in a layer and $X_{0,cm}^i$ its radiation length, one has

$$X_{0,cm}^{LAYER} = \sum_{i=1}^{n} p_T^i X_{0,cm}^i. \tag{5.11}$$

For the values in table 5.4 and 5.3 this give

$$X_{0,cm}^{CONDUCTOR} = \sum_{table\ 5.3}^{2\,rows} (column\,4)_i (column\,5)_i \approx 0.39\,\mathrm{cm}$$

Component	Weight % in paste	Weight % after firing	Thickness % after firing	Rad.length (cm)
Al_2O_3	30-40	47-53	36-44	7.0
BaO, BaO_2	10-20	13-27	10-16	$\approx$1.8
B_2O_3 (glass)	5-15	7-20	15-33	21
SiO_2	5-15	7-20	12-28	$\approx$12
ZnO	5	7	4	2.6

Table 5.4: Composition of paste for insulation.

and

$$X_{0,cm}^{INSULATOR} = \sum_{table\ 5.4}^{5\,rows} (column\,4)_i (column\,5)_i \approx 10.6\,\mathrm{cm}.$$

Measurements of the 4-chip-hybrids produced at CERN, showed that the thickness of the printed layers on one side is $220 \pm 10\mu$m. Measurements were made by a micro-meter over the thickness of several processed hybrids, and then subtracting the thickness of the substrates. The number and types of layers are probably close to the final Z-module hybrid design.

Approximate values for the thickness of conduction layers and insulation layers are $8\,\mu$m and $50\,\mu$m, respectively. A rough estimate is then that each side consists of $20\,\mu$m conductors, mostly from the ground and power planes, and the rest are contributions from the tracks, solder pads and bond pads in the other layers. The insulation layers then contribute the additional $200\,\mu$m, which should be in agreement with $50\,\mu$m for each layer.

For both sides one then have $40\,\mu$m conductor and $400\,\mu$m insulator. This gives $t_{CONDUCTOR} = 1.0\%$ and $t_{INSULATOR} = 0.38\%$.

The big contribution to the radiation length from the gold, excludes the use of gold, at least if one wants the design to contain a ground or power plane. Such planes usually improves the electrical properties. An alternative could be to use grids instead of full planes to reduce radiation length.

Of the other common materials, silver has the highest $X_{0,cm}$. If 100% silver is assumed, an estimate of the lowest percentage radiation length contributed by the most common conductor materials, is found. If again $40\,\mu$m of pure metal thickness is assumed, the result is $t_{Ag} = 0.46\%$. This is a solid improvement over gold.

The silicon detectors will be $300\,\mu$m thick if double sided, or $600\,\mu$m if single sided detectors are glued together. The thickest solution contributes to 0.70% of a radiation length.

A hybrid with a beryllia substrate, the insulator used in the produced hybrid and silver as a conductor will have a total thickness of $(0.44 + 0.38 + 0.46)\% \approx 1.3\%$.

For a silicon detector barrel, a particle will have to cross a silicon detector. The probability of crossing a hybrid is only given by the fraction of hybrid area to the silicon detector

area in one module. The hybrid will in the end hopefully be a little smaller than our 4 chip hybrid, which has an area of $9.5\,\mathrm{cm} \cdot 4.0\,\mathrm{cm} = 38\,\mathrm{cm}^2$. In the calculation below a hybrid area of $8\,\mathrm{cm} \cdot 3\,\mathrm{cm} = 24\,\mathrm{cm}^2$ is assumed. The silicon detectors in a module consists of two 6 cm by 6 cm silicon detectors, with a total area of $72\,\mathrm{cm}^2$. The probability of a particle crossing a hybrid is therefore $p_{hit} = \frac{24\,\mathrm{cm}^2}{72\,\mathrm{cm}^2} = \frac{1}{3}$.

The average thickness of a barrel is then given by $t_{AVERAGE} = t_{detector} + t_{hybrid} \cdot p_{hit}$. For the example, this is equal to $0.70\% + 1.3\% \cdot \frac{1}{3} \approx 1.1\%$.

For the average case a barrel will have a percentage X_0 of approximately 1.1%, while in the worst case (crossing of both a hybrid and a detector) the percentage will be approximately 2.0%. Remember these calculations do not say anything about the support structure of the barrels, cables for the modules and components on the module.

The ATLAS technical proposal [3, page 90] limits the radiation length of the four barrels to 6.4%, support and other materials included. This limit evolves from the sensitivity of the detector to the wanted physical processes. This limit gives an average of 1.6% per barrel. Even though the example gives 1.1% without the support structure and other materials, the 0.5% margin should be sufficient to make the barrels with hybrids close to the example mentioned above.

Chapter 6

Conclusions

The ATLAS experiment is meant to start datataking in 2004. In this thesis three related projects and problems have been addressed :

- A test hybrid has been designed and built. Valuable insight in the design and producion of thick film hybrids was gained. Support electronics for the read-out of FElix chips from these hybrids have been designed and successfully tested in a lab setup, using an oscilloscope and a VME-system. FElix32 chips with two versions of the digital logic have been proved working, contradictory to earlier belief that the one of them did not function correctly.
- A hybrid for a complete Z-module, incorporating 4 full 128-channel FElixes, has also been designed and built. This hybrid was made in thick film technology based on gold as conductor. Initial testing of the hybrid with only one FElix chip was performed successfully in a lab setup. These hybrids have later been tested with more than one front-end chip on the hybrid, and the design still seems to work.
- The Z-module hybrid has been shown to fulfill the technical specifications in ATLAS in terms of radiation length with the minor change of conductor material from gold to silver.

Appendix A

Sequencer tools listing

This appendix contains the program listing for `seq_tools.c`. This program can make a sequence file to be used with the prototype hybrid test setup. It can also make a file `xgraph.dat`, which is readable by the graph drawing program `xgraph` found on most Unix systems. To run xgraph, just type:

```
xgraph -tk -x 'TIME (us)' -y 'SIGNALS' xgraph.dat
```

The appendix contains two more programs as well. The first one is `seq_start`. It can read a sequence file of the now well known file format and download it to the SEQSI sequencer. This program is installed on the VME-crate. The only specific OS9-feature in this program is the use of the function `_os_permit()`. When porting this program to another VME-system this function may be something else. The reason for the function call is to tell the machine that you want to access the VME adress space, which is outside the area where our running `seq_start` is located in memory. This is because access to memory not in the adress space occupied by your own process, is restricted.

The last program, `seq_visual`, is a program for visualizing sequences. It asks for a sequence name and which bits in that file one wants to look at. The program then makes a xgraph file, and the sequence can be viewed with the same command as above, on a UNIX-system.

A.1 Program listing for seq_tools.c

```
#include <stdio.h>
#include <strings.h>

#define RBIT    1  /* Signals numbered from 1 to 20, corresponds to the */
#define T1      2  /* row number on the output connector of sequencer. */
#define RESETB  3  /* Start numbering at 1 on the bottom of connector. */
#define MRESETB 6
#define CKL     7
```

```
#define HOLDB   12

#define INV_MASK 0x0003   /* Bit 1 and 2 are LOW when the sequence is not
                             running, the other signals are HIGH */

#define PERIOD      25   /* Assumes 40MHz BCO-clock, that is 25ns period */
#define MAX_LENGTH  3000 /* Maximum length of sequence in units of 25 ns
                                This assumes sequencer running at 40MHZ */
#define NO_OF_BITS  32
#define CLOCKS      32   /* Number of clock cycles for AMUX clock */
#define RBIT_LENGTH 20
#define END_LENGTH  100

static char *name[] =                  /* The name of the signals used */
 { /* Mark that some signals are used internally in sequencer. */
   /* 20 first signals are on the output connector, used freely. The
      two named B29 and B30 in the end are output on NIM levels on the
      two lemo-plugs on top of the sequencer panel */
  "non-existent", "rbit","t1", "resetb", "?", "?", "mresetb",
  "ckl", "?", "?", "?", "?", "holdb", "?", "?", "?", "?",
  "?", "?", "?", "?", "DONT_USE", "DONT_USE", "DONT_USE", "DONT_USE",
  "DONT_USE", "DONT_USE", "DONT_USE", "DONT_USE", "DONT_USE",
  "B29", "B30",
  "DONT_USE"
 };

int bits[MAX_LENGTH][NO_OF_BITS+1];        /* Here lies the sequence */
int end_point;                            /* End of sequence posistion */

int t1_length, t1_delay, resetb_length, resetb_delay, holdb_delay,
    rbit_delay, ckl_delay, ckl_freq, holdb_deassert,
    mresetb_delay, mresetb_length;

void make_seq(void);
void make_xgraph(void);
void file_seq(void);
void read_seq(void);
void dump_line(FILE *f, int i);

void main(void)
{
 char command[50];
```

```
 printf("-------------------- SEQUENCER TOOLS ---------------------\n\n");
 printf("Output file for the sequencer gives the inverted of all\n");
 printf("signals. That is, as they are found on right column on\n");
 printf("the sequencer output connector. The picture presented\n");
 printf("by xgraph gives the signals not inverted, as they appear on \n");
 printf("the left column of the output connector on the sequencer.\n\n");
 printf("The making of sequences is just for making sequences for \n");
 printf("the prototype hybrid.\n");

 do
  {
   printf("\n*******************************************************\n");
   printf("***                   MAIN MENU                       ***\n");
   printf("*******************************************************\n");
   printf(" m) Make sequence and dump it to sequencer file and xgraph");
   printf("file.\n r) Read a sequence from file and dump it to xgraph");
   printf("file.\n q) Quit this program.\n");
   printf("Choose m,r or q:");
   gets(command);

   if (!strcmp(command,"m"))
     { make_seq(); file_seq(); make_xgraph(); } else
   if (!strcmp(command,"r"))
     { read_seq(); make_xgraph(); } else
   if (!strcmp(command,"q"))
     exit(0); else
   printf("\nUnknown command.\n\n");
 } while (1);

}

void make_seq(void)
{
 int i,j,k;

 for (i=0; i<NO_OF_BITS; i++)    /* Reset bit-pattern */
   {
     if ( (1<<i)&INV_MASK ) bits[0][i+1]=1; else bits[0][i+1]=0;
     for(j=1; j<=MAX_LENGTH; j++) bits[j][i+1]=bits[0][i+1];
   }
 printf("\n\n----------- MAKING SEQUENCE FOR SEQUENCER -----------\n\n");
 printf("\nRemember that all times are in units of %dns!\n",PERIOD);
 printf("Default values are in parenthesis.\n\n");
```

```
printf("The sequence starts with RESETB (FElix) at time (50)?");
scanf("%d", &resetb_delay);
printf("The length of RESETB (15)?");
scanf("%d", &resetb_length);
printf("Then from end of RESETB until T1 is (300)?");
scanf("%d", &t1_delay);
printf("It has the lenghth (15)?");
scanf("%d", &t1_length);
printf("From the end of the T1 until the start of HOLDB,");
printf("the delay is (310)?");
scanf("%d", &holdb_delay);
printf("From the start of the HOLDB until the start of CKL,\n");
printf("the delay is (20)?");
scanf("%d", &ckl_delay);
printf("The CKL consists of 32 clock cycles, of frequency\n");
printf("5 MHz, 4 MHZ, 2 MHZ or 1 MHZ, choose 5, 4, 2 or 1?");
scanf("%d", &ckl_freq);
if (!(ckl_freq==5 || ckl_freq==4 || ckl_freq==2 || ckl_freq==1))
  ckl_freq=1;
printf("After the CKL-cycles there is a delay before HOLDB\n");
printf("is deasserted, which is (100)?");
scanf("%d", &holdb_deassert);
printf("The MRESETB is asserted a time after the HOLDB\n");
printf("is deasserted, which is (20)?");
scanf("%d", &mresetb_delay);
printf("The length of the MRESETB is (15)");
scanf("%d", &mresetb_length);
printf("After end of MRESETB, RBIT is clocked into the mux by\n");
printf("CKL, after a delay of (50)?");
scanf("%d", &rbit_delay);

k=resetb_delay;                          /* Here starts the RESETB */
for (i=0; i<resetb_length; i++) bits[k+i][RESETB]^=1;
k=k+resetb_length+t1_delay;              /* Here starts the T1 */
for (i=0; i<t1_length; i++)     bits[k+i][T1]^=1;
k=k+t1_length+holdb_delay;               /* Here starts the HOLDB */
j=k+ckl_delay+1000*CLOCKS/PERIOD/ckl_freq+holdb_deassert;/* HOLDB ends */
for (i=k; i<j; i++) bits[i][HOLDB]^=1;
k=k+ckl_delay;                          /* Here starts the CKL */
for (i=0; i<CLOCKS; i++)
  for (j=0; j<500/PERIOD/ckl_freq; j++)
    bits[k+i*1000/PERIOD/ckl_freq+j][CKL]^=1;
```

```
 k=k+1000*CLOCKS/PERIOD/ckl_freq+holdb_deassert+mresetb_delay;/* MRESETB */
 for (i=0; i<mresetb_length; i++) bits[k+i][MRESETB]^=1;
 k=k+mresetb_length+rbit_delay;                    /* Start of RBIT */
 for (i=0; i<40; i++)  bits[k+i][RBIT]^=1;
 for (i=20; i<40; i++) bits[k+i][CKL]^=1;
 end_point=k+40+100;

 printf("\n-----------------------------------------------------\n");
}

void file_seq(void)
{
 FILE *f;
 int i,j,k;
 char filename[40];

 printf("\n\n------------- SENDING SEQUENCE TO FILE ---------------");
 printf("\n\nName of file to write sequence to:");
 scanf("%s", filename);
 f=fopen(filename,"w");

 fprintf(f,"blocks= 14\n");
 k=0;
 fprintf(f,"offset= %d length= %d width= 1\n", k, resetb_delay);
 dump_line(f, k);
 k=resetb_delay;                              /* Here starts RESETB */
 fprintf(f,"offset= %d length= %d width= 1\n", k, resetb_length);
 dump_line(f, k);
 k=k+resetb_length;                            /* Here ends RESETB */
 fprintf(f,"offset= %d length= %d width= 1\n", k, t1_delay);
 dump_line(f, k);
 k=k+t1_delay;                                  /* Here starts T1 */
 fprintf(f,"offset= %d length= %d width= 1\n", k, t1_length);
 dump_line(f, k);
 k=k+t1_length;                                  /* Here ends T1 */
 fprintf(f,"offset= %d length= %d width= 1\n", k, holdb_delay);
 dump_line(f, k);
 k=k+holdb_delay;                             /* Here starts HOLDB */
 fprintf(f,"offset= %d length= %d width= 1\n", k, ckl_delay);
 dump_line(f, k);
 k=k+ckl_delay; i=1000/PERIOD/ckl_freq;     /* The CKL-cycles */
 fprintf(f,"offset= %d length= %d width=%d\n", k, i*CLOCKS, i);
 for (j=0; j<i; j++) dump_line(f, k+j);
```

```
 k=k+i*CLOCKS;                                  /* HOLDB ends */
 fprintf(f,"offset= %d length= %d width= 1\n", k, holdb_deassert);
 dump_line(f, k);
 k=k+holdb_deassert;                           /* Before MRESETB */
 fprintf(f,"offset= %d length= %d width= 1\n", k, mresetb_delay);
 dump_line(f, k);
 k=k+mresetb_delay;                              /* MRESETB */
 fprintf(f,"offset= %d length= %d width= 1\n", k, mresetb_length);
 dump_line(f, k);
 k=k+mresetb_length;                            /* Before RBIT */
 fprintf(f,"offset= %d length= %d width= 1\n", k, rbit_delay);
 dump_line(f, k);
 k=k+rbit_delay;                              /* First half of RBIT */
 fprintf(f,"offset= %d length= %d width= 1\n", k, RBIT_LENGTH);
 dump_line(f, k);
 k=k+RBIT_LENGTH;      /* Rest of RBIT and the CKL to clock it in */
 fprintf(f,"offset= %d length= %d width= 1\n", k, RBIT_LENGTH);
 dump_line(f, k);
 k=k+RBIT_LENGTH;       /* Extra delay in the end of the sequence */
 fprintf(f,"offset= %d length= %d width= 1\n", k, END_LENGTH);
 dump_line(f, k);

 fclose(f);
 printf("\n-----------------------------------------------------------\n");
}

void read_seq(void)
{
 FILE *f;
 char infile[40], s[40];
 int offset, length, width, blocks;
 int i,j,k,l;

 printf("\n\n-------------- READ A SEQUENCE FROM FILE -------------");
 printf("\n\nName of sequence file to read:");
 gets(infile);
 f=fopen(infile,"r");
 if (f==NULL) {printf("Couldn't find file."); exit(0); }

 fscanf(f,"blocks= %d\n", &blocks);
 printf("blocks=%d\n", blocks);

 for (i=0;i<blocks;i++)
```

```
   {
     fscanf(f,"offset= %d length= %d width=%d\n", &offset,&length,&width);
     printf("offset=%d length=%d width=%d\n",offset,length,width);

     for (j=0; j<width; j++)
       {
         fgets(s,40,f);
         printf("%s",s);
          for (l=0; l<length/width; l++)
           {
            for (k=1;k<NO_OF_BITS+1;k++)
             {
              if (s[k-1]=='1') bits[offset+j+l*width ][k]=1;
              else             bits[offset+j+l*width ][k]=0;
             }
           }

       }

   }
 end_point=offset+length;
 fclose(f);
 printf("\nThe file is read!\n");
 printf("\n-----------------------------------------------------------------\n");
}

void make_xgraph(void)
{
 FILE *f;
 int l,j,k=0;

 printf("\n\n------------------ MAKING XGRAPH FILE --------------- \n\n");
 printf("Making xgraph-file of the sequence and calls it xgraph.dat.\n");
 printf("Take a look at it on unix systems with:\n");
 printf("xgraph -tk -x 'TIME (us)' -y 'SIGNALS' xgraph.dat\n");
 printf("on unix systems. See man xgraph on your system for more info.\n");

 f=fopen("xgraph.dat","w");
 fprintf(f, "TitleText: A sequence for the prototype hybrid.\n");

 for(l=1; l<NO_OF_BITS+1; l++)
  {
     if (  strcmp(name[l],"?") && strcmp(name[l],"DONT_USE")
```

```
        && strcmp(name[l],"B29") && strcmp(name[l],"B30")   )
      {
       fprintf(f,"\"%s\n",name[l]);
       for (j=0; j<end_point; j++)
         fprintf(f, "%3.2lf %d\n",((double)(PERIOD*((long)j)))/1000.0,
                                      (bits[j][l]^1)+2*k);
       k++;
       fprintf(f,"\n");
      }
  }
 fclose(f);
 printf("\n---------------------------------------------------------------\n");
}

void dump_line(FILE *f, int i)
{
 int j;

 for (j=1; j<NO_OF_BITS+1; j++)
   {
     if (bits[i][j]&1) fprintf(f,"1"); else fprintf(f,"0");
   }
 fprintf(f,"\n");

}
```

A.2 Program listing for seq_start.c

```
#include <stdio.h>
#include <process.h> /* For the _os_permit */

#define BASE       0xFE0F0000 /* Base adress for the sequencer */
#define INTR_START 10    /* Adress for sequence start when triggered */
#define JUMP1      5     /* First jump bit placement. Less than INTR_START */

#define DUMMY      0
#define PERMISSION 3                /* Read and write on VME-bus */
#define SIZE_SEQ   32               /* Size of SEQSI in VME-adressspace */
#define MAX_LENGTH 0xFFFF           /* Memory depth of sequencer */

int read_seqfile();
void download_data(int);
```

```
void insert_control();

/* The 11 SEQSI register addresses follow */
short *MEM_LOW_WORD  = (short *)(BASE+0x00);
short *MEM_HIGH_WORD = (short *)(BASE+0x02);
short *JUMP_ADDR     = (short *)(BASE+0x04);
short *INTERRUPT_ADDR= (short *)(BASE+0x06);
short *CLOCK_CTR     = (short *)(BASE+0x08);
short *POLARITY_CTR  = (short *)(BASE+0x0A);
short *DIRECT_CTR    = (short *)(BASE+0x0C);
short *SIGNAL_CTR    = (short *)(BASE+0x0E);
short *MEM_ADDR_COUNT= (short *)(BASE+0x16);
short *MEM_DATA      = (short *)(BASE+0x18);
short *TRIGGER_CTR   = (short *)(BASE+0x1A);

long word[MAX_LENGTH];

main()
{
    int seq_length;

    /* Make the SEQSI adress memory accessible from this process */
    printf("OS9 reply to wanted access of VME-adress space:%d\n",
           _os_permit((void *)BASE, SIZE_SEQ, PERMISSION, 0) );

    seq_length=read_seqfile();  /* Read the sequence file */
    download_data(seq_length);  /* Download data part to sequencer */
    insert_control();           /* Set the sequencer control registers */
    exit(0);
}

void insert_control()
{
    *INTERRUPT_ADDR = INTR_START;

    *POLARITY_CTR   = 0x0;   /* Use bit pattern as in file */
    *DIRECT_CTR     = 0x0;
    *SIGNAL_CTR     = 0x0;
    *TRIGGER_CTR    = 0xF;   /* All triggers accepted */

    *MEM_DATA       = DUMMY;
    *CLOCK_CTR      = 0x1;   /* 40 MHz clock on */
}
```

```
void download_data(int length)
{
    int i;

    *CLOCK_CTR      = 0x200; /* Clock off for the download... */
    *MEM_DATA       = DUMMY; /* First operation on sequencer */

    *JUMP_ADDR      = 0    ; /* load adress to start downloading */
    *MEM_ADDR_COUNT = DUMMY; /* move it to MEM_ADDR_COUNT */

    for (i=0; i<length; i++)
      {
        *MEM_LOW_WORD  = (short) ( word[i] & 0xFFFF);
        *MEM_HIGH_WORD = (short) ((word[i] >> 16) & 0xFFFF);
      }

    *JUMP_ADDR      = 0; /* Start address for sequencer */
    *MEM_ADDR_COUNT = DUMMY;
}

int read_seqfile(void)
{
 FILE *f; char infile[40], s[40];
 int offset, length, width, blocks, i, j, k, l;

 printf("\n\n---------------- READ A SEQUENCE FROM FILE ---------------\n\n");
 printf("Name of sequence file to read:");
 gets(infile);
 f=fopen(infile,"r");
 if (f==NULL) {printf("Couldn't find file."); exit(0); }

 fscanf(f,"blocks= %d\n", &blocks);
 printf("blocks=%d\n", blocks);

 for (i=0;i<blocks;i++)
   {
     fscanf(f,"offset= %d length= %d width=%d\n", &offset,&length,&width);
     printf("offset=%d length=%d width=%d\n",offset,length,width);

     for (j=0; j<width; j++)
       {
         fgets(s,40,f);
```

```
        printf("%s",s);
        for (l=0; l<length/width; l++)
          {
            word[offset+j+l*width]=0; /* Clear */
            for (k=0;k<32;k++) /* The bits from the file are bit 0 to 31 */
              { if (s[k]=='1') word[offset+j+l*width ]|= (1 << k ); }
            /* Now make sure the file can't touch bits 27,28 and 31 */
            word[offset+j+l*width]|=0x08000000; /* All outputs enabled */
            word[offset+j+l*width]&=0xEFFFFFFF; /* Clock outputs enabled */
            word[offset+j+l*width]&=0x7FFFFFFF; /* Don't set JUMP bit */
   }
       }
   }
 fclose(f);
 word[JUMP1]|=0x80000000;           /* Set jump bit for idle loop */
 word[offset+length-2]|=0x80000000; /* Set jump bit for interrupt sequence */
 printf("\n----------------------The file is read!-----------------------\n");
 return offset+length; /* Return length of sequence */
}
```

A.3 Program listing for seq_visual.c

```
#include <stdio.h>
#include <strings.h>

void make_xgraph(int);
int read_seq(void);
void define_bits();

void dump_bit(int, int, int, FILE *); /* Helping function */

unsigned char bits[65536][32];   /* Here lies the sequence */
unsigned char should_out[32]=  /* Default for bits to display */
 {1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0};

void main(void)
{
 int length;

 printf("\n---------------- SEQUENCE VISUALIZATION ------------------\n\n");
 printf("The graph presented by xgraph gives the signals as they appear\n");
 printf("on the left column of the output connector on the sequencer.\n");
```

```
 printf("This is the inverted of the input file itself.\n");
 printf("\n************************************************************\n");

 length=read_seq();
 define_bits();
 make_xgraph(length);
}


int read_seq(void)
{
 FILE *f; char infile[40], s[40];
 int offset, length, width, blocks, i,j,k,l;

 printf("\n\n-------------- READ A SEQUENCE FROM FILE ------------");
 printf("\n\nName of sequence file to read:");
 gets(infile);
 f=fopen(infile,"r");
 if (f==NULL) {printf("Couldn't find file.\n"); exit(0); }

 if(fscanf(f,"blocks= %d\n", &blocks)!=1)
   { printf("Error in first line of input file.\n"); exit(0); }
 printf("blocks=%d\n", blocks);

 for (i=0;i<blocks;i++)
   {
     if
      (fscanf(f,"offset= %d length= %d width=%d\n", &offset,&length,&width)!=3)
{ printf("Error in block header %d of input file.\n",i+1); exit(0); }
     printf("offset=%d length=%d width=%d\n",offset,length,width);

     for (j=0; j<width; j++)
       {
         fgets(s,40,f);
         printf("%s",s);
          for (l=0; l<length/width; l++)
           {
            for (k=0;k<32;k++)
             {
              if (s[k]=='1') bits[offset+j+l*width ][k]=0; else
              if (s[k]=='0') bits[offset+j+l*width ][k]=1; else
               {
                printf("Error in input file, not 0 or 1 in line above.\n");
```

```
                exit(0);
               }
             }
           }
       }
   }
 fclose(f);
 printf("\nThe file is read, no syntactical errors.\n");
 printf("But who knows about logical errors.....\n");
 printf("\n-------------------------------------------------------------\n");
 return offset+length;
}

void define_bits()
{
 char string[40];
 int i;
 printf("\n-------------  DECIDE WHAT BITS TO VIEW --------------------\n");
 printf("Press return for default, select 0 for not viewing,\n");
 printf("any thing else (like 1) for viewing.\n");

 for (i=0; i<32; i++)
   {
    printf("Bit %2d, has default %d, and should be:",i,should_out[i]);
    gets(string);
    if (!strcmp(string,"")) { } else
    if (!strcmp(string,"0")) should_out[i]=0; else
    should_out[i]=1;
   }
 printf("\n-------------------------------------------------------------\n");
}


void make_xgraph(int length)
{
 FILE *f;
 int l,n=0;

 printf("\n\n------------------ MAKING XGRAPH FILE --------------- \n\n");
 printf("Making xgraph-file of the sequence and calls it xgraph.dat.\n");
 printf("Take a look at it on unix systems with:\n");
 printf("xgraph -tk -x 'TIME (us)' -y 'SIGNALS' xgraph.dat\n");
 printf("See man xgraph on your system for more info.\n");
```

```
 f=fopen("xgraph.dat","w");
 fprintf(f, "TitleText: SEQSI sequence visualization.\n");

 for(l=0; l<32; l++)
  {
     if ( should_out[l] ) { dump_bit(length, l, n, f); n++; }
  }
 fclose(f);
 printf("\n---------------------------------------------------------------\n");
}

void dump_bit(int length, int l, int n, FILE *f)
{
 int count=0, offset=0;
 unsigned char value;

 value=bits[offset][l];

 fprintf(f,"\"BIT %2d\n", l);

 while(offset<length)
  {
   while(bits[offset+count][l]==value && offset+count<length) count++;
   fprintf(f,"%4.3lf %d\n", ((double)offset)*0.025, value+2*n);
   offset+=count; count=0;
   fprintf(f,"%4.3lf %d\n", ((double)offset)*0.025, value+2*n);
   value=bits[offset][l];
  }
 fprintf(f,"\n");
}
```

Appendix B

FElix128 specifications

Most information in this appendix, except from the description of the FElix functionality to follow, can be found in a similar paper made by Joar Martin Østby at SI/Sintef in Oslo, on the 25.th of April 1995.

SI/Sintef uses different names on signals and specifies some different bias currents, than the people at CERN and the University of Oslo that have done most of the testing of the previous 32 channel versions of the FElix. This paper use the names and values on signals used by the University of Oslo and CERN.

During testing and read-out of the 32 channel versions of the FElix, an analog MUX, made by Jan Kaplon at CERN was used. A 128 channel version of this chip was produced in early 1995 to be used with the FElix128. The FElix128 was back from production in July 1995. Testing shows that this FElix function well.

Both chips are 1.2 μm CMOS by Austria Mikro Systeme, AMS.

B.1 A brief description of the FElix functionality

The small current spike from the detector is first put through a fast charge-sensitive pre-amplifier, which has a gain of 1 mV/fC. The signal is then shaped by a slower CR-RC shaping amplifier network to give a pulse with a peaking time of 75 ns, which is 3 beam crossing intervals, BCOs. The gain of this stage is approximately 20.

The analog delay and buffering unit, ADB, samples the signal at 40 Mhz (the BCO-rate) and delays it 1.675 μs in its pipeline in order to let the first trigger decision arrive. This trigger decision is made on the basis of either muon or calorimeter data. If a trigger pulse (T1) arrives, four samples concerning the event are pulled out at the end of the pipeline. The continuous read-out frequency of the FElix is 250 kHz. That is, if several triggers occur within a short time interval the FElix will put them out one at a time at a rate of 4 μs per event. The processing of a single event takes 4.775 μs. This does not contradict the level one trigger rate of 100 kHz, because that is the maximum mean value of the stochastically spread out triggers.

Three of the four samples is put through the analog signal processor, APSP, which

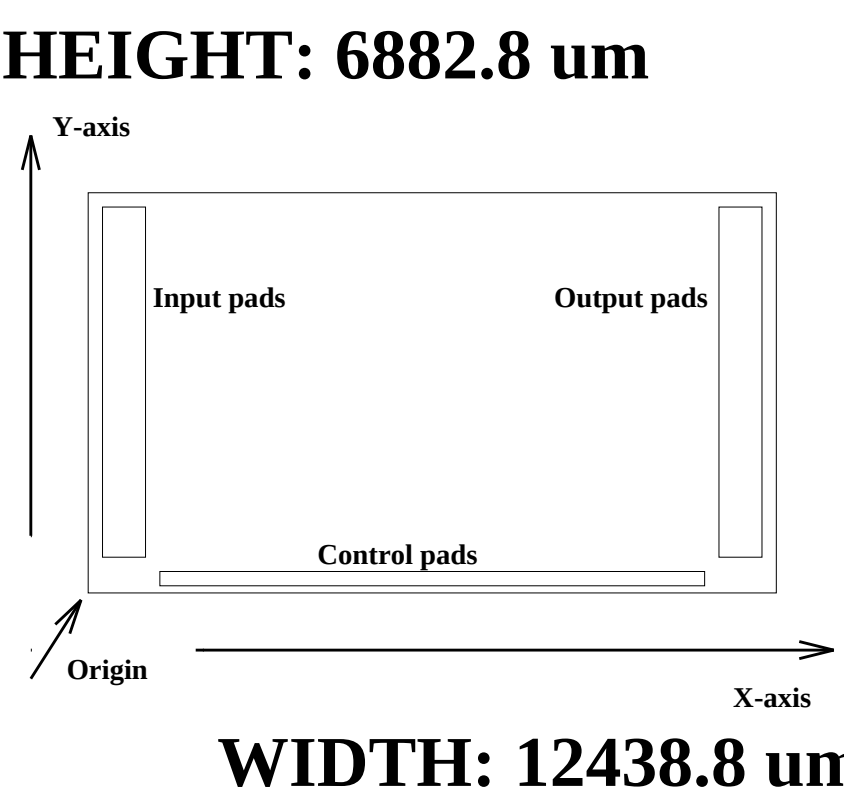

Figure B.1: The 128 channel FElix.

essentially de-convolutes the smearing done by the CR-RC shaper, and gives an output proportional to the height of the shaped signal out of the ADB. This is not the total height of the ADB signal, but only the part associated with this trigger. Because of pile-up from earlier triggers due to the long shaping time the total height of the pulse can be higher than the contribution from a specified trigger. The fourth sample associated with the total pulse height out of the ADB is also put on the FElix output. This is put out first, for a period of 550 ns. Then after 250 ns, in which the signal output is reset, the de-convoluted signal is output for 550ns. These pulse heights are supposed to be the same if there is not any earlier signal near in time that can have contributed to pile-up. To indicate that there are valid signals on the output the DTA signal of the FElix is brought high.

The BUSY signal can be used by electronics following the FElix in the read out chain, to slow down the FElix read out. BUSY can be asserted anywhere in the time slot from one BCOs after the first DTA to 13 BCOs after the second DTA. The FElix will then finish the read out the event associated with these two DTA-pulses, but will not start to read out any more events before BUSY is brought low again. Events associated with triggers in the interval BUSY was high, will be read out as soon as BUSY goes low. Is the following electronics fast enough, the BUSY signal can be hardwired low.

A simple drawing of the FELIX128 showing the size of the FElix and the placement of the coordinate system used in the next subsections, can be found in figure B.1.

B.2 The pads at the bottom edge

The edge pads in table B.1 have the size 90 μm in x-direction and 120 μm in y-direction. The coordinates give the center points for these pads. Currents are positive into the FElix. The pads are listed in order of increasing x-position.

B.3 Analog input and output pads

The analog pads have the size 112 μm in x-direction and 60 μm in y-direction. There are 129 analog input and output pads numbered 0 to 128.

There are two pads for each input and output channel. They have the same Y-coordinates, but different X-coordinates. (X1 and X2) The input and output channel pads have coordinate centers at the left edge and the right edge respectively as seen in figure B.1. The pad positions are listed in table B.2.

B.4 The three probe pads on the top edge

They have the same size as the input/output pads, and the positions are listed in table B.3.

Pad	X	Y	Description
CAL	927	160	0.1 Volt, excite all channels
CAL10	1207	160	0.1 Volt, excite one of ten channels
GND1	1467	160	Analog ground
	1667	160	
AVDD	1747	160	+2V analog power
	1887	160	
VFP	2027	160	-0.4V, pre-amp feedback resistor
AVSS	2167	160	-2V analog power
	2297	160	
PREB	2447	160	700μA pre-amp bias current
VFS	2727	160	0.3V, shaper feedback resistor
SHAB	2867	160	120μA shaper bias current
BUFB	3007	160	80μA pre-amp/shaper output buf.
VDC	3287	160	-0.9V, backplane ADB storage capacitors
AVSS	3990	160	-2V analog power
DVDD	6927	160	+2V digital power
DVSS	7067	160	-2V digital power
BCOP	7307	160	ECL pos. input, 40MHz
BCON	7507	160	ECL neg. input
RESETBP	7867	160	ECL pos. input, FElix reset
RESETBN	8067	160	ECL neg. input
DTAB	8327	160	Open drain inverted output
DTA	8467	160	Open drain output, data available
T1P	8707	160	ECL pos. input, FElix trigger
T1N	8907	160	ECL neg. input
BUSYP	9267	160	ECL pos. input
BUSYN	9467	160	ECL neg. input
AVSS	9866	160	-2V analog power
DVDD	10147	160	+2V digital power
DVSS	10427	160	-2V digital power
GND3	10707	160	Analog ground
GND2	10907	160	Analog ground
AVDD	11105	160	+2V analog power
VBP	11307	160	-1.1V APSP backplane capacitors
APSPB	11507	160	20μA, APSP bias current

Table B.1: Power, biasing and digital control for FElix128.

INPUT PADS	X1	X2	Y
Even channel numbers	165	505	6706-47i
Odd channel numbers	330	675	6706-47i
OUTPUT PADS	**X1**	**X2**	**Y**
Even channel numbers	11770	12105	6696-47i
Odd channel numbers	11935	12275	6696-47i

Table B.2: The analog input and output pads for FElix128.

Signal	X	Y	Comment
OUTAMP	3115	6705	Output of pre-amp/shaper for broken ch.
INADB	3367	6705	Out of ADB and into APSP for broken ch.
ADBAPSP	10005	6705	Input to pre-amp in broken channel

Table B.3: The three probe pads for the FElix128.

Appendix C

AMUX128 signal description

In this appendix there will be given a list with a short description of the AMUX128 signals, see table C.1. The names are the ones used in the schematic of the Z-module hybrid, but most of them are just shorter versions of the names used by the chip designer Jan Kaplon, CERN.

All digital control signals are now differential ECL. Logic levels is approximately $-0.9\,\mathrm{V}$ for logic one and $-1.7\,\mathrm{V}$ for logic zero.

In normal operation the digital test controls should be connected in such a way that no ambiguities can arise. That is, the signal or the inverted should be to for instance $-2\,\mathrm{V}$. The other should be to a higher voltage, for instance ground or +2V. On our Z-module hybrid I have connected TRESET, TCLK and TSH to $+2\,\mathrm{V}$ and the inverted inputs to $-2\,\mathrm{V}$.

C.1 Power, biasing and control for AMUX128

Pad/Signal	Description
AVDD	+2V analog power.
AVSS	-2V analog power.
DVDD	+2V digital power.
DVSS	-2V digital power.
DGND	Ground. Used by digital part.
SFBI	50μA bias for sample and hold buffer.
MRESET MRESETB	Reset of the shift register. Active high. Differential ECL.
CKL CKLB	The shift register clock. Shifts on negative edge of CKL. Differential ECL.
SAMPLE SAMPLEB	Selects sample or hold. Active (sample) high. Differential ECL.
RBIT RBITB	Input bit for shift register, active high. Differential ECL.
RBOUT RBOUTB	Output of shift register, active high. Lines pulled by 470Ω to DVSS.
MOUT OLEV	The analog MUX output. Pulled to AVSS by 10kΩ. The reference part of AMUX. Also pulled.
TCLK TCLKB	Test clock. Inverted of TCLK.
TSH TSHB	Test sample/hold. Inverted of TSH.
TRESET TRESETB	Reset in test mode. Inverted of TRESET.
ATST	Analog test input, not bonded in normal operation.

Table C.1: Description of AMUX32 signals for the prototype hybrid.

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[15] Martin Morrissey. *The SEQSI VME-module is made by Martin Morrissey at Rutherford Lab in the UK.*

[16] Lars Gundersen. *The file format used in the C-programs for the SEQSI is invented by Lars Gundersen, a student at the Particle Physics group, University of Oslo.*

[17] Shaun Roe. *Shaun Roe at CERN has made a multitude of Labview programs for automated tests of FElix chips.*

[18] Rui De Olivera. *Rui De Olivera produced the hybrids at Gandhis workshop, CERN. He provided valuable information about thick film production, in special information about the contents of the printing pastes used.*

[19] Ole Dorholt. *Ole Dorholt did the layout for all designs mentioned in this thesis, except for the level shifter layout.*