University of Oslo
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The PCB; an interface between hybrid and VME-crate

Tests and development of the ATLAS Z-module

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Chapter 1

Introduction

Physics experiments of the past hundred years have revealed the atom's structure, with its nucleus and orbiting electrons. Today's experiments use powerful particle accelerators to explore the deepest substructure of matter, the particles and forces inside the proton and neutron of the atom's nucleus. Decades of research have now given us a remarkably simple theoretical model of the elementary particles and forces of matter [1].

1.1 The standard model of elementary particles

The theory of fundamental particles and their interactions is called the Standard Model (SM). The Standard Model (SM) is an explanation of matter by means of mathematically formulated quantum theories. All known particles in SM model are called either fermions or bosons.

A fermion is any particle that has odd-half-integer (1/2, 3/2, ...) intrinsic angular momentum (spin). Fermions obey a rule called the Pauli Exclusion Principle which states that no two fermions can exist in the same state (identical spin, color charge, angular momentum, etc.) at the same place and time. Many properties of ordinary matter arise because of this rule. Electrons, protons and neutrons are all fermions. More generally, all the fundamental matter particles, quarks and leptons, and the composite particles, baryons, are fermions.
A boson is a particle that has integer spin (spin=0, 1, 2...). The particles associated with the force fields, carrier particles, related to all the fundamental interactions are bosons. Composite particles with even numbers of fermion constituents, mesons, are also bosons.

- The six leptons include the electron (e), the muon (μ), the tau (τ); and three neutral particles called neutrinos (v_e, v_μ and v_τ).

- The six quarks include the up and down quarks that make up the proton and neutron, as well as the strange, charm, bottom, and top quarks that were present at the birth of the universe and that we now produce in particle collisions.

- The gauge bosons include the gluon that transmits the strong force that holds quarks together in the nucleus; the W and Z bosons that transmit the weak nuclear force

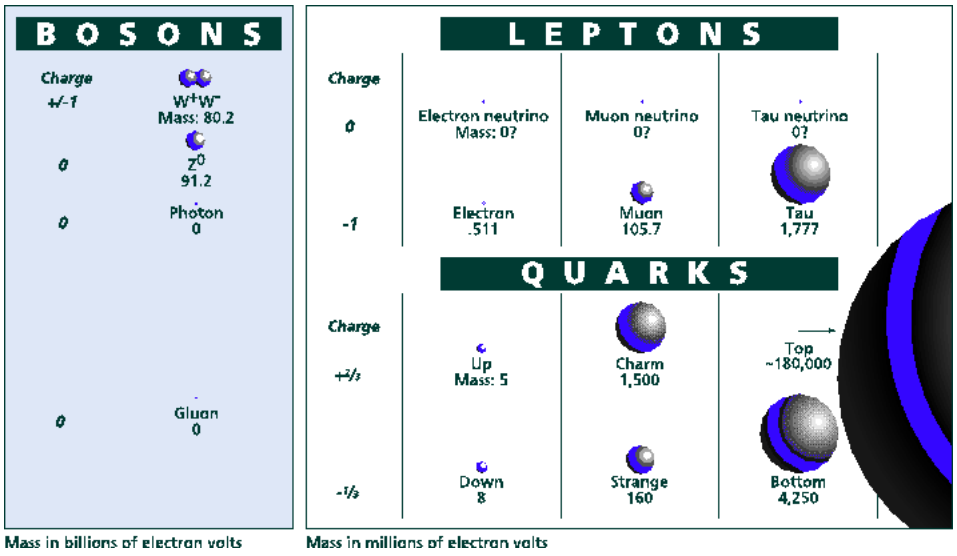


Figure 1.1: Standard model

responsible for radioactive decay; and the photon that transmits electro-magnetic force. Fig. 1.1 gives an overview of the bosons energy compared with leptons and quarks.

The SM has too many unkown quantities to be the ultimate theory. What is the origin of the mass? Why do the fundemental particles show no regularity in their mass? These questions can not be answered by the SM. In an attempt to answer some of these questions the SM applies the Higg's mechanism. It suggest that particles aquire mass by interacting with a field, the Higgs field, which is present everywhere. If we were able to discover the Higgs boson(s), we would have proved the existance of the Higg's field.
The SM calculations suggest that if the quarks energies reach 1 TeV something has to show up. This is the energy range which the LHC has been designed to explore [2].

1.2 The LHC machine

The LHC layout is defined and constrained by the LEP tunnel geometry. The LHC will be a Large Hadron Collider. One of the LHC's experiments will be p-p colliding project in which two protons will be able to collide with 14 Tev in center of mass at a luminosity $\mathcal{L}=10^{34}$ cm^{-2}s^{-1}. The machine will also provide heavy (Pb) ion collisions with a center-of-mass energy of more than 1000 TeV and a luminosity in excess of 10^{27} cm^{-2}s^{-1}. This is an extremely large amount of energy and requires the use of many sophisticated acceleration methods in achieving these energies.

1.2.1 Opposite attract

All particle accelerators start from the principle that electrically charged objects exert a force on each other–opposite charges attract; like charges repel. That is, a particle with a positive or negative charge experiences a force when it is in the presence of an electric field. When a net force acts on an object, the object accelerates. A proton accelerator keeps applying the force to accelerate protons until they are going at almost the speed of light.

A positively charged proton - a hydrogen atom stripped of its single electron- which is exposed to an electrical field will be accelerated. Accelerators in fact use this simple principle but use very sophisticated voltage sources to create large electric-field. In this way they can give protons up to many millions of electron volts of energy.

1.2.2 Raising the energy

To give the proton still higher energy, we can send it through a series of small acceleration gaps, one after another. A proton moving along its path approaches the first acceleration gap in the path. The gap is like the one between the plates connected to the battery, but with a much higher voltage. Once the proton enters the gap, it feels the force of the electric field and accelerates to the negative side of the gap, gaining energy. It speeds on its way down the path with its added energy. We now send the proton through a second gap. It gains a second boost of energy on top of the first. By sending the proton through many accelerating gaps, and shielding it from the electric field when it is between gaps, we can use a succession of small voltages to boost the proton to a higher and higher energy. Accelerators that work this way are called linear accelerators, or **linacs**, and they can accelerate protons to a few hundred million electron volts or MeV. The more gaps a linac has, the higher the energy it can give to a proton- and the longer the linac gets. When a linac runs out of real estate, it reaches its energy limit.

Now, what if we take the proton as it shoots out the end of the linac and bend its path around to the beginning, to go through the series of acceleration gaps again, but this time at a much higher starting energy? We can send it back to the beginning many times, each time at a higher energy than before.

Because the path of a moving charged particle bends in a magnetic field, we can use magnets to bend the proton's path, sending it circling back to the beginning. Each time the proton goes around the circle and through the accelerating gaps it gains more energy. To

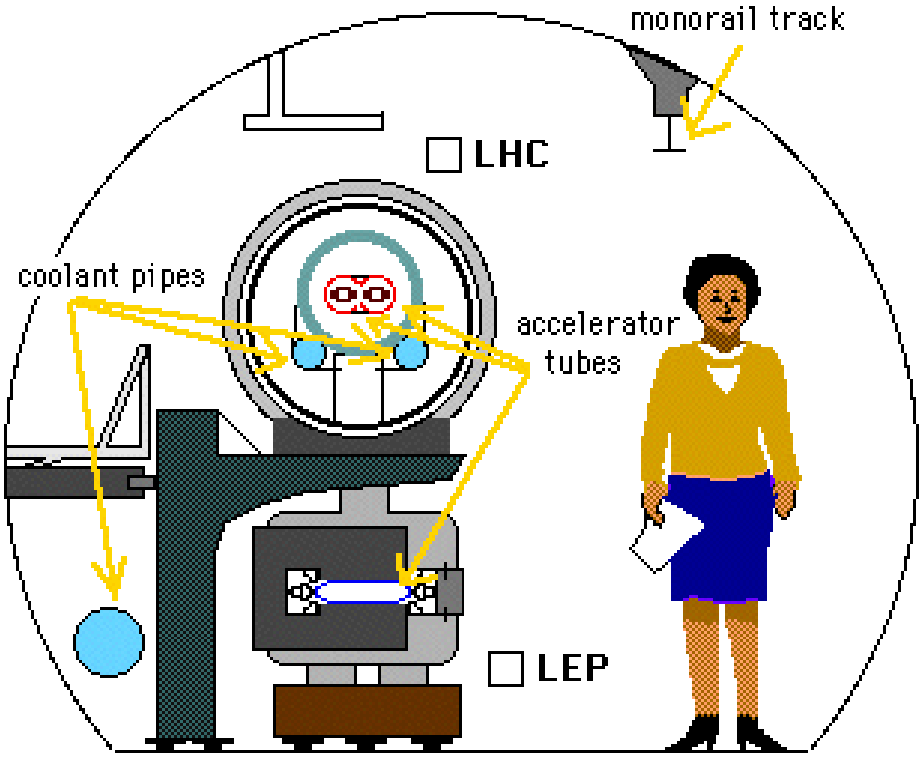


Figure 1.2: The LHC will use the existing LEP tunnel.

keep it on the same circular path as it gains energy, we must make the magnetic field slightly stronger each time it goes around. We synchronize the increase in the magnetic field with the proton's increasing energy. To keep our protons circling together, we focus them into a tight beam. This is a circular accelerator of the type called a **synchrotron** [1].

LHC proton synchrotron will be able to give protons energies of nearly 7 Tev. While the protons are speeding around the accelerator ring, we feed another batch of protons into the same ring in opposite direction. Protons charge allows them to be bent in the same circle by the magnets, but traveling the opposite way around. We have now produced two intense beams of particles orbiting the accelerator ring in opposite directions at close to the speed of light. When we decide to bring the beams together at a point in the accelerator ring, we will cause millions of high-energy collisions yielding hundreds of different kinds of particles, one of them, perhaps, an unknown particle.

1.2.3 Collision between particles

How new particles are produced?. What happens in the kind of particle collision that can produce some particles? The answer laies in energy deposition to particles in the accelerating process.

These new particles originally are created during acceleration and will become visible (by

means of detectors) after collision event. When these protons collide (head on) at a fixed crossing point, their combined energy of motion will be 14 TeV. They both smash to bits, and pieces fly off in every direction. Some of the bits that fly off can be heavier than the proton and proton combined. For instance a top quark is more than 100 times as heavy as a proton.

1.3 The LHC accelerator

The machine is constituted of eight bending arcs separated by eight insertions. The physics necessity at LHC demands to have the protons in opposite bunches. The two counter-rotating beams are separated horizontally by 194 mm in most of the machine. The beams are exchanged from the inner to the outer ring and vice versa at points 1, 2, 5 and 8 (see fig. B.1 on page 99), where they collide. Their path lengths are therefore the same. Before and after collision, the beams are brought together or separated by separation/recombination dipoles [3].

The two "colliding" synchrotrons will installed in the LEP tunnel. They will be filled with protons delivered from the SPS and its pre-accelerators at 0.45 TeV. Two super-conducting magnetic channels will accelerate the protons to 7-on-7 TeV. These super-conducting accelerating **cavities** 'kick' the protons almost to the speed of light. The magnetic channels will be housed in the same yoke and cryostat [4]. There are two rings, one ring per beam. One circulates clockwise and the other anti-clockwise. The BCO rating is 25 ns, it means that each bunch use 90 μs to travel around the ring. Thus there will be 3600 bunches in the ring at any instance. The distance between two bunch with the same direction will be 7.5 m.

Specification	Value	Unit
energy	7.0	TeV
dipole field	8.38	T
luminosity	10^{34}	$cm^{-}2\ s^{-1}$
bunch spacing	25	ns
bunches pr beam	3600	
particle pr bunch	1x 10^{11}	
stored beam energy	332	MJoule
beam life time	22	h
total radiated power pr beam	3.7	kW

Table 1.1: Basic design parameters for the LHC machine

1.3.1 The LHC Magnets

The p-p bunches circulate through the rings (beam pipes) of 27 km length in opposite direction. The purpose of the large ring is to keep the particles on curving paths. Protons

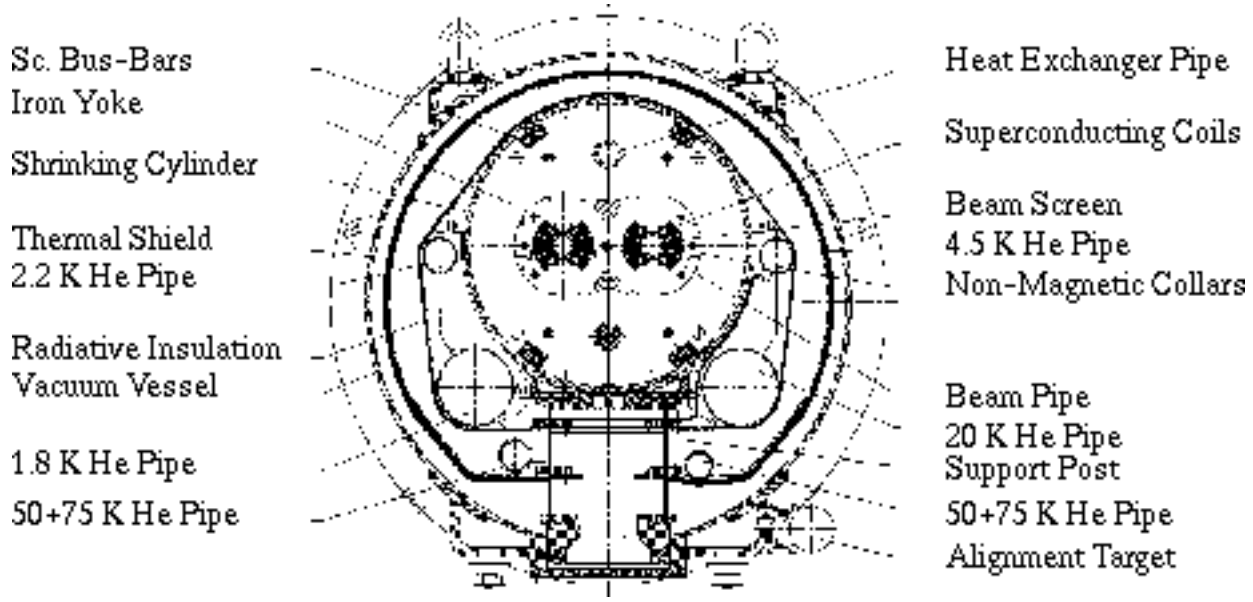


Figure 1.3: LHC magnets.

circulating around the pipe radiate energy. The reason for this is the change in their velocity due to path's bending. The amount of energy lost in this manner increases both with the energy of the particles and with the curvature of the beam pipe.

The LHC ring accelerator operates with two kinds of electromagnets. The Large Hadron Collider (LHC) will use super-conducting magnets to guide the beam around its ring, this is because magnetic field exerts a force on moving charged particles. The super-conducting magnet technology has allowed us to attain higher energies in circular accelerators. One can obtain higher magnetic fields than the conventional magnets. Fig. 1.3 shows the LHC magnets arrangement.

The LHC beams need high magnetic bending fields, to bend 7 TeV protons around the ring. To keep the protons on a desired curve we have to correct their path. The LHC **dipole** magnets are applied to do this task. These magnets steer the particle beam along it's circular path through the ring. They must be able to produce fields of 8.36 Tesla. Super-conductivity makes this possible. At very low temperature the electric current through the magnet coil, will not be exposed to any resistance and as the result power loss will be eliminate. This effects are used to produce high magnetic fields. The LHC magnets will be operated at 1.9° above absolute zero (1.9 K) [4].

The number of dipole magnets will be 1,296 each of 14.2 m. The other magnet type are **quadrupoles** which focus the particles along the beam and prevent them from straying [4]. fig. 1.2 on page 7 shows the the ring in which proton bunches will be accelerated.

The magnets lie in the LEP tunnel which is 3.8 meters wide and which forms a ring 27 km in circumference. The tunnel extends out from CERN's main site at Meyrin in Switzerland.

1.3.2 Cryogenic

It is very important to keep the system at low temperature. The cryogenic system choosed for LHC is foreseen to use super-fluid helium, which has unusually efficient heat transfer properties, allowing kilowatts of refrigeration to be transported over more than a kilometer with a temperature drop of less than 0.1 K.

The LHC's super-conducting magnets will sit in a 1.9 K bath of super-fluid helium at atmospheric pressure. This bath will be cooled by low pressure liquid helium flowing in heat exchanger tubes threaded along the string of magnets. The reliability and efficiency of this sophisticated cryoloop are key factors in achieving the required magnet performance.

The magnets coil is indirectly cooled with forced flow of two phase helium through a single pass cooling tube. The coil can be cooled down to 4.5 K° in 100 hours with a helium mass flow of 20 g/s by keeping the maximum temperature difference in the coil below 40 K.

The LHC cryogenic system is very large as well as very cold. Refrigeration power equivalent to over 140 kW at 4.5 K is distributed around the 27 km ring [5]. During the initial cool-down of LHC will 12 million liters of liquid nitrogen will be vaporised to cool-down 31,000 tons of material. And the total inventory of liquid helium will be 700,000 liters[5].

Chapter 2

A p-p experiments at LHC

The two general purpose p-p experements at LHC are ATLAS and CMS. These abbreviations stand for:

1. ATLAS: A Toroidal Large hadron ApparatuS.
2. CMS: Compact Muon Solenoid.

By general purpose we mean the detectors designed to perform high p_T physics such as studies of the top quark and search for the Higgs and supersymmetric particles in the p-p interactions at LHC in the central region. The b-quark is an important tool for high p_T physics [6]. The two high-luminosity insertions are located at diametrically opposite straight sections, point 1 (ATLAS) and point 5 (CMS). Fig. B.1 on page 99 shows these points. These detectors have been optimized for the search of the SM Higgs boson over a mass range to 1 TeV. They also allow detection of a wide range of possible signatures from alternative electro-weak symmetry breaking mechanisms, in addition they are also well adapted for the study of top, beauty and tau physics at lower luminosities [7]. In addition the following processes will be the major issues at the LHC [8]:

- The search for Super-symmetry.
- the search for extensions of the SM (heavy gauge bosons, strong symmetry breaking).

2.1 The ATLAS experiment

The ATLAS is one of the two p-p experiments at LHC. In this thesis our main concern is the ATLAS. The ATLAS is , as is CMS, a general purpose experiment. In the following will be given some information about the detector and it's building blocks.

Particles can not be detected without special made detection instruments. We must use a detector to determine the trajectories of charged particles, to measure their mass and to derive their charge and momentum from the track curvature in a magnetic field. The detector assembly is used for recording the aftermath particles after each p-p bunch crossing.

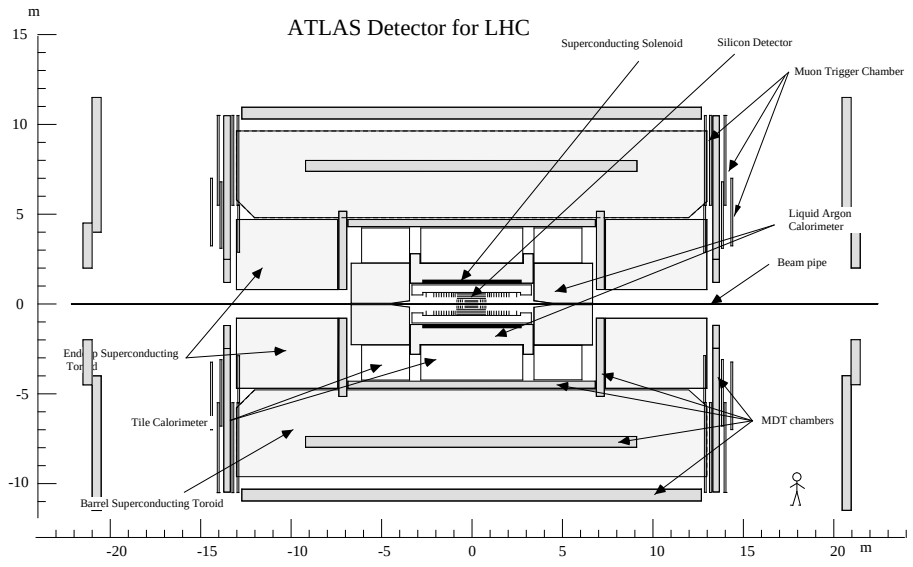


Figure 2.1: The position of different detectors within the ATLAS detector.

This detector consists of several sub-detectors mounted in **barrel** and end-caps around the interaction point. The main aim of experiment is to trap as much of the debris from each collision as possible. In addition we need to know which kinds of particle emerge and with what energies. Therefore we use a variety of detectors that can assist in identifying different particles as well as in measuring their energies. Together the detectors form a huge structure. Approximate dimensions of the ATLAS are 10 m in radius and 26 m in length [9] and weighing several thousands tons.

Most types of particles produced in collision events have lifetimes so short that they travel an extremely short distance before decaying, and therefore leave no "tracks". We must deduce their presence by examining the characteristics of their decay products [10]. As we know charged particles are subject to electric and magnetic fields. They will be deflected by these fields. These effects varies with respect to the particle charge, mass and energy. We are able to combine many components to make a multi-layered detector that has many capabilities. Each component serves a separate function in tracking the particles, measuring their energies and momenta, and/or distinguishing different particle types. Enormous number of collisions are analyzed, so large computers are needed to collect and to interpret the data. In particle collider concept we use a term called η. This term defines at which angle the detector is able to measure the resulting particles or photons after a collision.

$$\eta = -ln(tan(\frac{\theta}{2})). \tag{2.1}$$

Spheric coordinates are used to describe the detector's geometry. The angels are expressed in radians. The z-axis is along the pipeline. If we assume that the inner detector covers to $\eta = 2.5$, it means that the θ direction is covered to 9.4^0.

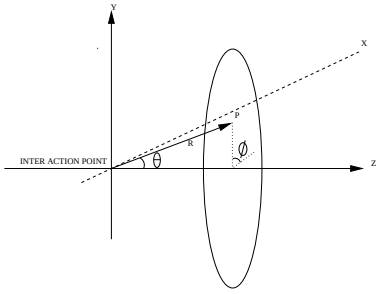


Figure 2.2: Spheric coordinate of detector

2.2 Different detector layers

The ATLAS detectors will use many different sub-detectors to identify particles. These sub-detectors combined with their mechanical, cryogenic and on board electronic will form a huge assembly. They complement each other by having different capabilities in identifying charged particles resulting from collisions. We can roughly categorize these sub-detectors in three main groups:

- Calorimeters
- Muon detectors
- Inner-detector

2.3 Calorimeters

The ATLAS calorimetry is designed to meet the following demands while operating in a very high luminosity environment. The system must be capable of reconstructing the energy of electrons, photons, and jets, as well as measuring missing transverse energy [11]. Fig. 2.3 shows the position of the calorimeters. The following goals are foreseen for calorimeters:

- Good electromagnetic calorimeter to identify and measurement of photons and electrons in the energy range 7-10 GeV up to 1 TeV.
- Accurate jet and hermetic missing transverse energy measurements.
- Resistance against radiation accumulated in 10 years of the LHC life time.

The ATLAS calorimetry is divided into:

1. Electromagnetic calorimeter.
2. Hadronic calorimeter.

The calorimetry is based on liquid argon calorimeters and a scintillator tile calorimeter which cover the radial space up to a radius of 2.25 m for electro-magnetic and up to a radius of 4.25 m for hadronic calorimetry.

2.3.1 Electromagnetic calorimetry

Outside the tracking detectors, the next layer traps and identifies all electrons, positrons and photons as they pass into a dense material. This material is interleaved with detectors to measure the energy that the particles lose as they come to a halt. The aim is to create an electro-magnetic calorimeter that measures all the energy the electrons, positrons and photons. The EM calorimeter consists of an inner barrel cylinder and end-caps.

This configuration helps in identifying particles such as neutral pions, which leave no tracks in the inner detectors. These particles decay to photons and are thereby detected in this layer. The technology used for the calorimeter is LAr which is intrinsically radiation hard. This design for EM calorimeter is called :

- Accordion design: The electromagnetic calorimeter uses lead absorbers in a noble liquid ionization calorimeter implemented in an 'accordion' geometry, both for the barrel ($|\eta|<1.4$) and for the end-caps ($1.4<|\eta|<3.2$) [9].

Lead absorbers are clad with steel and are equipped with kapton readout electronics. Gaps between electrodes (lead plates) are filled with liquid argon LAr. A barrel cryostat around the inner detector cavity contains the barrel electromagnetic calorimeter and the solenoidal coil which supplies a uniform field to the inner tracking volume. This coil is placed in front of the EM calorimeter.

2.3.2 Hadronic calorimeter

Outside the tracking detectors there is a layer incorporating the iron that forms the return yoke of the solenoid. It stops the strongly interacting particles, or hadrons[1] and measures their energy. This layer forms the hadron calorimeter. The layer measures the total energy of the particles.

Hadrons have greater mass and momentum than the electrons. The major goals of the hadronic calorimetry at the ATLAS are to identify jets and measure their energy and direction, to measure the total missing transverse energy E_T, and to enhance the particle identification capability of the electromagnetic calorimetry by measuring quantities such as leakage and isolation. The ATLAS calorimeter has been designed to meet the diverse and exacting demands of the LHC physics programme while operating in a very high luminosity environment [9]. The layout of the calorimetry sub-detector is shown in fig 2.3. The hadronic calorimetry in the barrel region uses iron absorbers with scintillator plates and it surrounds the full length of the EM calorimeter. The geometry adopted consists of scintillator and iron tiles staggered in planes perpendicular to the beam axis. In addition there will be a similar hadronic End-Cap Calorimeter.

[1] Those particles are (mesons and baryons) built from quarks and antiquarks

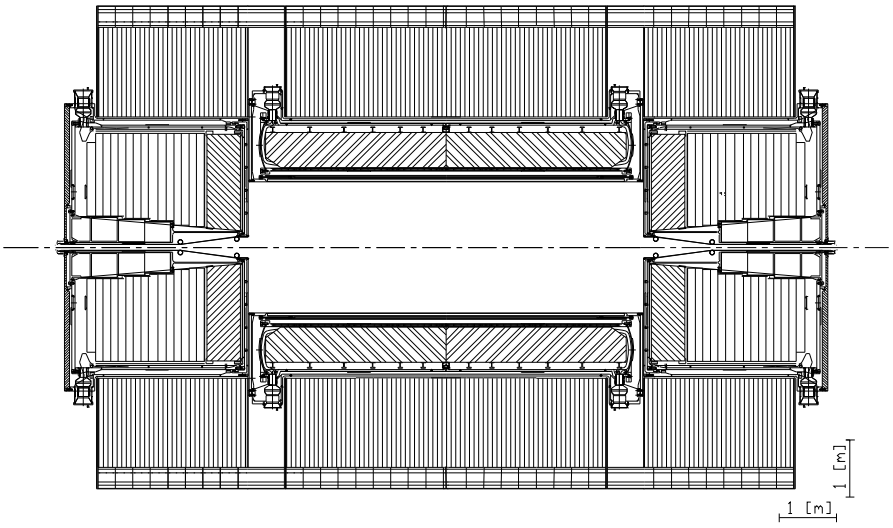


Figure 2.3: The calorimetry position in the ATLAS

2.4 Muon detector

Two kinds of particles are likely to penetrate beyond the hadron calorimeter: muons and neutrinos. The outermost layer of detectors reveals the tracks of penetrating charged particles, mainly muons. Only the neutrinos escape the apparatus without direct detection. But their existence can be deduced. The total energy of the p-p that collided is known. By adding up all the energy deposited by particles in the various pieces of the apparatus we can calculate, by using the principle of energy conservation, the energy which is gone missing. This missed energy will be the undetected neutrinos energy. The direction of neutrinos will be calculated by means of conservation of momentum. Since the longitudinal component of the interacting parton system in general is not known this argument can only be applied in the transverse plane in a pp-collider.

Muon detectors are composed of several detector layers with a magnetic field between them. Fig 2.4 shows a view of the muon spectrometer. To characterize a muon, the deflection of the muon in the magnetic field applied by the toroid magnet is measured. The muon detector consists of a 26 m long barrel part with an inner bore of 9.4 m and an outer radius of 19.5 m and two end-caps with lengths of 5.6 m and inner bores of 1.26 m. The muon spectrometer uses different types of chambers up to radii of 19.5 m to detect and trigger on muon tracks. In the barrel the layout consists of three layers of chambers and in the end-caps the chambers are placed on the front and back faces of the cryostats. A third layer is fixed on the cavern wall. Two types of chambers are used for the high-precision measurements:

- The monitored drift tube chambers (MDT) consist of two multi-layers of four planes of pressurized thin-wall aluminum tubes with a diameter of 30 mm.

- The cathode strip chambers (CSC) are multi-wire proportional chambers with a sym-

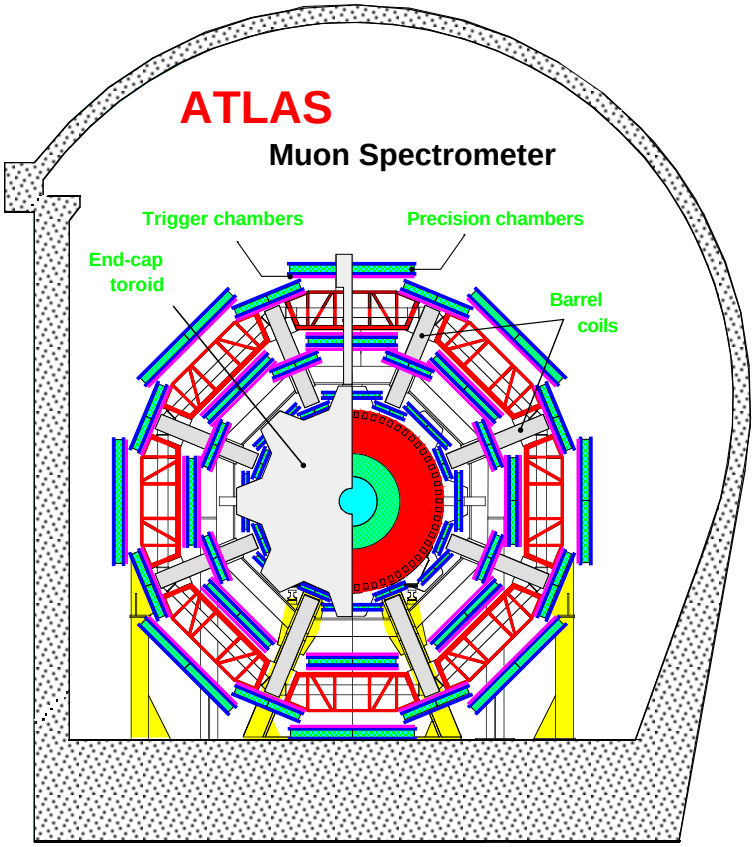


Figure 2.4: Transverse view of the ATLAS muon spectrometer.

metric cell in which the anode-cathode distance equals the anode wire spacing, both typically 2.5 mm.

The high-precision measurements are complemented with chambers for triggering. There are also two types used for this:

- The resistive plate chambers (RPC) are gaseous parallel plate detectors.
- The thin gap chambers (TGC) are used in the forward region. They are wire chambers.

The muon detector is based on super conductive air core-toroid magnet (see chapter 2.6.2) equipped with muon chambers. The muon detector is important at high luminosity, for Higgs search and asymmetry measurements. The ATLAS muon system will cover $|\eta|$=3.

2.5 Inner-detector

The ATLAS inner detector cross section is shown in fig. 2.5. It occupies the cylindrical cavity defined by the boundaries of the electro-magnetic-calorimeter cryostats, with a radius $R =$

115 cm and $|z|$ = 345 cm. Polyethene moderators are situated from $|z|$ = 340 cm to $|z|$ = 345 cm on the front face of the end-cap calorimeters to lower the energy of neutrons entering the cavity, thus reducing their damage to the detector. The cavity is enclosed in a solenoid with an axial central field of 2T [9].

The inner detector is divided into a barrel part between polar angles of 45° and 135°, and forward parts beyond. In the barrel part, detectors are concentric cylinders, parallel to the beam axis, in the forward part they consist of 'wheels' transverse to the beam axis. The following processes will be the major issues at the LHC, and in consequence they impose basic requirements on the tracker [8]:

- The search for the SM Higgs in the full mass range between $\sim$ 80GeV and 1 TeV.
- The search for Super-symmetry.
- The search for extensions of the SM (heavy gauge bosons, strong symmetry breaking).

Additional requirements on the inner detector at low luminosity running:

- Good impact parameter measurement for b- and τ-identification;
- Reconstruction of J/ψ and K_S^0 decays.

The inner-detector has to give good pattern recognition. This implies a large number of measurements per track. The detector is composed of the following sub-detectors:

1. High precision Semi Conductor Tracking (SCT)
2. Transition Radiation Tracker (TRT)

2.5.1 Inner tracker SCT

A charged particle passing through material will ionize the atoms. If the particle velocity come close to light speed i.e. if β = v/c $\approx$ 96%, and hits the material at normal incidence, the amount of electrons which are realeased is refered to as a MIP (Minimum Ionizing Particle). It has been stimated that the amount of electrons releases in this case will be 23000[2]. The Si-detector thickness is assumed to be 300μm.

The layers of tracking detectors reveal the tracks of charged particles (neutral particles do not leave tracks). A large solenoid provides a magnetic field to bend these tracks, so that a particle momentum can later be calculated from the amount of bending. The principal aims of the central tracking system is to detect high-p_T charged tracks. The central tracking devices complement the essential information from calorimetry and muon detection. They reveal the tracks of charged particles.

[2]According to Beth-Block formula a particle passing thruogh a 300μm Si-sensor will lose 84 KeV of its energy. For Si e/h pair energy is 3.6 eV resulting $\frac{84000}{3.6}\approx$23000 e^-.

The pixel, silicon and GaAs detectors together comprise the Semi-Conductor Tracker (SCT) [9]. The layout of the precision tracking is such that every track within $|\eta| < 2.5$ crosses two layers of pixels and four layers of strips. These layers and their specifications are as follows:

- Pixel layers: There are two pixel layers at radii of 11.5 cm and 16.5 cm in the barrel region. They are the first layers in the inner-detector closest to the beam pipe. In addition there will be eight pixel disk layer in forward regions. Pixels are well suited to the vertexing requirements owing to their good radiation tolerance, spatial resolution, and pattern recognition capability.
  The pixels have to be highly efficient for charged tracks, so that when we see a charged track without a corresponding hit in the first plane, we know that it originated from a photon conversion (γ -> e^+ e^-).
  The separation provides an adequate lever arm for impact parameter measurements, extrapolation to the silicon layers and two particle separation. The length of the pixel barrel layers are reduced to decrease the radiation length the high rapidity and because of the degradation in z-resolution for track far from the normal incidence. For the vertexing layer and the pixels, which are at smaller radii, the resolution is 10μm in ϕ and 87 μm along the beam axis or z-direction [12].

- Four silicon-strip layers: These layers of strips will actually be double or single, with the two sets of strips running at small angles relative to each other, to provide a desired space-point measurement. The layers provides an rϕ and a 40 mrad stereo measurement with 20μm precision. The choice of a small angel stereo is choosen to reduce the rate of fake track formed from the combinations of ghost hits produced by close tracks The actual length is choosen to ensure that high momentum particles coming from the interaction point cross the detector planes at roughly normal incidence. The lengths of these layers are given in table 2.1. The resolution of each track point measurement and the layer radii are the fundamental parameter determining performance of the tracker. ATLAS specifies that each measurement in the SCT silicon strip layers should have a accuracy of 20μm. The effective resolution along the z-direction is 500μm [12]. In addition to barrel layers there are 18 forward wheels consisting of silicon and GaAs detectors in ATLAS.

- Vertexing layer: This is a removable layer around the beam pipe. It's task will be the vertex-finding capability for B physics and other physics during the first few years of LHC operation[3]. This layer is foreseen as either an additional pixel layer at a radius of 4 cm or a double-sided silicon-strip layer at 6 cm [9].

Pattern recognition, momentum and vertex measurements, and enhanced electron identification are achieved with a combination of discrete high-resolution pixel and strip detectors in the inner part. The layer closest to the TRT permit precise extrapolation between the SCT and TRT and maximizes stand alone momentum resolution. Inner layers are used in reconstruction of decay vertices.

[3]During the first years, the LHC will run at low luminosity

System	Barrel radii (cm)	Length (cm)	Area m^2	Resolution (μm)
Pixel 1	R: 11.5	70	1.38	$\sigma_{R\phi}$=14
Pixel 2	R: 16.5	90	0.79	$\sigma_{R\phi}$=14
Silicon stripe	R: 30, 40, 50, 60	164	41	$\sigma_{R\phi}$=20

Table 2.1: The position of different inner-detector layers.

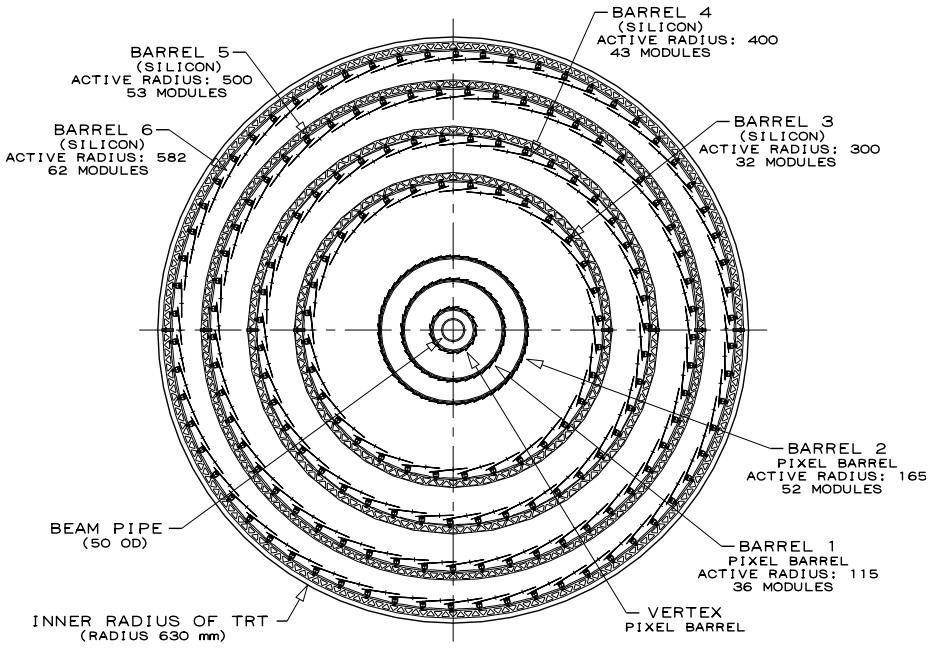


Figure 2.5: End view of the SCT in the central region.

2.5.2 Transition Radiation Tracker (TRT)

In order to achieve a high number of measurements per track, the SCT layers are complemented by a straw tube tracker. The electron-identification capabilities are enhanced by the use of transition radiators, with detection of the photons in the straw tubes. The transition radiation gives additional electron identification ability, independent of the energy-momentum matching between the calorimeter and SCT.

The transition radiation tracker (TRT) is based on straw tubes of 4 mm diameter. These tubes are made from 60 μm thin kapton walls with a 50 μm gold-plated beryllium wire along the straw axis. The straws are interleaved with polyethylene radiators to produce and detect X-ray emission from very relativistic particles. A high p_T charged particle will transverse 64 layers of the TRT and give at least 36 tracking points providing a good pattern recognition.

2.6 Magnets

The ATLAS magnet system consists of a **solenoid** and air-core **toroids**. Their positions in the detector are :

1. The solenoid occupies the inner-detector cavity, to bend charged particle trajectories.
2. The toroid is applied at the outer edges of ATLAS, giving bending to the muons.

2.6.1 Solenoid

The solenoid magnet covers the whole inner-detector. As we know a magnetic field exerts a force on moving charged particles. The reason for this kind of magnet here is to bend the charged particles trajectory inside the inner detector region. The 2 T solenoid is positioned in front of the barrel EM calorimeter. The solenoid length will be 5.3 m [11].

The solenoid is designed to provide an axial magnetic field of 2 Tesla at the center of the tracking volume. The technology of super-conducting magnets using indirectly-cooled aluminum-stabilized super-conductors is choosen to achieve the highest possible field with minimum thickness [9]. The design parameters are listed in table 2.2.

coil inner radius	1218	mm
coil length	5300	mm
central field	2.0	Tesla
peak field	2.6	Tesla
nominal current	8000	A
number of ampere-turns	$9.3 \cdot 10^6$	
total stored energy	42	MJoule
stored energy/cold mass	8.4	kJ/kg
conductor size	28×4.3	mm^2
aluminum stabilizer	99.999%+200ppm Zn	
super-conducting cable	Nb/Ti/Cu	0.5/0.5/1
cable size	6.4×2.2	mm^2
Jc in NbTi 5T,4.2K°	2500	A/mm^2
critical current 5T,4.2K°	16000	A
static thermal load	20 W + 30 ℓ/hr	

Table 2.2: Basic design parameters of the solenoid

The solenoid coil is integrated into the vacuum vessel of the LAr calorimeter barrel cryostat, thus eliminating the material and space of independent vessel walls. The super-conducting coil will be wound as a single layer on the inside of a support cylinder, with a winding radius of 1.22 m. The coil plus cryostat wall thickness in front of the e.m. calorimeter is 0.83 X_0 at normal incidence.

2.6.2 Toroid

This magnet will be used to give path deviation to muons. The field of a toroidal magnet is confined completely to the space enclosed by the windings. We can think of a toroid as a solenoid that has been bent into a circle [13].

The super-conducting air-core toroid magnet system consists of a 26 m long barrel part with an inner bore of 9.4 m and an outer diameter of 19.5 m, and two end-caps with lengths 5.6 m and inner bores of 1.26 m, inserted at each end of the barrel. Each toroid consists of eight flat coils symmetrically arranged about the beam axis, with the end-caps rotated with respect to the barrel so that the coils interleave. For the barrel, each coil has its own cryostat, with the coils connected together to form a rigid cold mass which contains the large magnetic forces acting radially inwards. Because of their smaller relative size, each end-cap toroid can be housed in a single large cryostat.
In view of the large ratio of outer/inner radius of the end-cap toroids, their windings are distributed radially to counteract excessively large peak fields towards the inner radius.

The whole magnet system represents a cold mass of 700 tons and a total weight of 1400 tons. The barrel toroid is supported on four pillars and anchored to the floor and walls of the cavern, whereas the end-cap toroids are supported on a rail system which is also used for the calorimeters [9].

Chapter 3

Si-sensors as radiation detectors

The goals for the SCT are vertex determination and the measurement of short-lived particles by precise determination of the formation and decay vertices in addition to general pattern recognition. The placement of these detectors is within the inner-detector as explained in chapter 2.5.1.

The subject of my thesis has been to make an interface for the ATLAS Z-module, and it is designed to be used on the barrel SCT. Therefore it seems naturally to have a better insight about the basic elements used on the barrel i.e. Si-sensors. In the following an overview about these sensors will be given.

3.1 Si-sensors

A high energy particle passing through the semiconductor material collides inelastically with valence electrons, exciting them from the valence to the conduction band and creating pairs of holes and conduction electrons. The conductivity increases momentarily, causing a pulse of currents in the external circuits [13].
A Si-sensor is made on a wafer[1] which can be n or p type. Si-sensors are based upon the reverse biased diodes. A reversed bias diode will cause a region of depletion on each side of p-n junction. The **depletion** region is a region around the junction which is devoid of current carriers. The depletion area will be free of charge carriers[2]. When a high energy charged particle encounter the silicon detector, the lattice silicon will loss one electron. As a result there will be created a pair of electron (e) and hole (p). The hole is used to denote a Si-atom which has lost it's electron.
If no electric field is applied, the electron/hole have a tendency to recombine again and form a neutral atom. But in presence of an electric field across the Si-sensor, these e/h can not recombine together right after ionization. Electrons and holes produced by passage of ionizing particles, drift within this bias field across the depletion layer resulting current pulse in a

[1] See the glossary at the end of this thesis.

[2] Majority charge carrier for n-type semiconductor are electrons and for p-type materials are holes. Minority carriers for n-type are holes and electrons for p-type material.

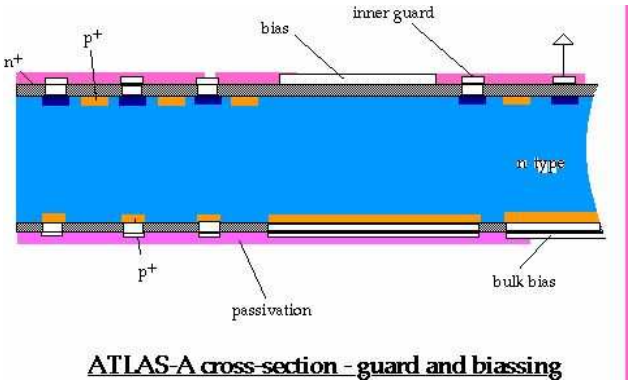


Figure 3.1: A view of a strip detector based on n-substrate.

charge sensitive preamplifier. For the readout of silicon micro-strip detectors, the magnitude and time development of the available signal put stringent requirements on the front end design. Physics considerations limit the acceptable thickness of silicon detectors used for tracking to ~300 μm , yielding a most probable value of ~22000 electrons for a minimum ionizing particle crossing the detector at normal incidence. The effects of Landau fluctuations and charge sharing between strips, especially for steeply inclined tracks, imply that much smaller charges must be detected with high efficiency. In addition it is of paramount importance to maximize charge collection. However, collection times, which in principle are only limited by carrier velocities in very high electric fields, are in practice determined by the fact that practical detector bias voltages will be in the range below 200 volts to achieve reliable operation of systems with many million channels. Detector current pulses with tails extending up to 20-30 ns may have to be tolerated [14].
By using this method and suppressing recombination we will be able to detect a signal at charge-sensitive preamplifiers just in vicinity of the Si-detector.

There has been investigations to find the best Si-detector type for ATLAS. Options are between double-sided and single sided back-back. The various detectors are categorizes in single-sided (ATLAS-A and ATLAS-B), see section 3.1.2. The other option is double-sided (ATLAS-C), see chapter 3.1.3. The choice of the optimal detector will be made after beam-tests and radiation hardness studies.
Strip capacitance is the dominant factor in the noise of LHC readout electronics. Values of 1.2-1.4 pF/cm are expected for strips on 50 μm pitch. Although there is an increase in this value after ionizing irradiation, in the high frequency range of LHC amplifier operation the change appears to be no more than10-20%. The charge distribution arriving at the strips or pixels is about 6 μm wide. The Si-detector is made of high resistivity doped Si-wafers. The magnetic field opposed from the solenoid perpendicular to the drift direction increases this width (at 1.68 T from 6 μm to about 12 μm) [15], depending on the module orientation.
The detector elements will be geometrically arranged as single or double-sided strips. The large track density requires the use of tracking layers with high granularity, and the momentum-

resolution and spatial-resolution targets demand a high precision per point in both coordinates. Semiconductor devices on silicon or GaAs substrates offer such resolutions. A combination of pixel detectors and small-angle stereo-strip tracking provides the required granularity. It has been assumed that only tracks separated by at least three strips can be resolved in the Si-detector [9].

The required resolution for Si-detectors has been suggested to be 20 μm. Depending on the direct or capacitive readout, this would be achieved in two ways.

- Direct readout: Readout strips are spaced by 75 μm if direct readout is used.
- Capacitive readout: In charge division approach the readout strips are spaced by approximately 1.5 times the direct method i.e. 112.5 μm.

3.1.1 Bulk damage

One of the most important concerns for Si-detectors is the effect of radiation on these detectors[3]. Their desired function can be deviated by long radiation expose. The radiation is responsible for an undesired effect on Si-sensors, called **bulk damage**. The major bulk damage effect is that the effective impurity concentration, N_{eff}, of n-type detectors reduces with neutron fluence and becomes p-type after about 10^{13} $\frac{neutrons}{cm^2}$. This is called the inversion fluence, above which N_{eff} for both p- and n-type detectors increases linearly with fluence at almost the same rate. Irradiated detectors also become more p-type with a time constant of several months at room temperature , which can be halted for temperatures below about 5 C°. This makes it essential for the detectors to be cooled during operation.

The reason for bulk damage is not well understood. The most attractive explanation states that a single or small number of deep levels within the silicon band gap are the probably origin of the effects observed and that the level of oxygen and carbon in the material may influence their evolution in realistic conditions. The results from pion irradiation indicate that 190 MeV pions exhibit similar damage to 1 MeV neutrons.

3.1.2 Single sided detectors

By implantation techniques, many narrow diode strips are formed, each one presents a single diode detector.

ATLAS A is a single-sided capacitively coupled sensor in rϕ. Fig. 3.1 on page 23 shows such a Si-detector. The detector is specified as follows [16]:

- **Overall area** is 60mm $\times$ 60mm
- **Thickness** 300μm
- **Number of strips** 1536

[3]In appendix A is given some more information about the radiation effects on Si-sensors and on the FE-electronics.

- **Number of read out** 512
- **Read out pitch** 112.5μm
- **Substrate** n/p type high ρ silicon
- **Strips** High doped n-implant. Pitch: 37.5μm
- **Strip dimensions:** Width 27.5μm (depends on isolation), length ~60~mm
- **Read-out** 200 $\times$ 50μm bond pads[4], $\geq$ two rows, daisy-chainable.

ATLAS B is the other single-sided option which is direct coupled in rϕ. The specifications are [16]:

- **Overall area** is 60mm $\times$ 60mm
- **Thickness** 300μm
- **Number of strips** 768
- **Number of read out** 768
- **Read out pitch** 75.0μm
- **Substrate** p-type and n-type
- **Strips** High doped n/p-implant. Pitch: 75.0μm
- **Strip dimensions** Width 15μm, length ~60~mm
- **Read-out** 200 $\times$ 50μm bond pads, $\geq$ two rows, daisy-chainable.

The detector elements will be geometrically arranged as single-sided strips. One module is made of two (four) 6 cm$\times$6 cm double (single) sided silicon micro-strip detectors. In the single side case, the butt gluing is followed by a back-to-back attachment. One side of the module measures ϕ (the 'axial strips') while the other side is rotated by the small stereo angle 40 mrad. A total of 11424 single-sided silicon-strip detectors (area = $41m^2$) is required for the four outermost barrel layers shown in figure 2.5. A guiding principle has been to make the detector highly modular and to minimize the number of different components required. All four cylinders are built from identical modules. In one proposed assembly scheme, 14 modules are first mounted onto a stave and then the staves are assembled into cylinders.

[4] An area on the periphery of the substrate for making connection to one of the component pins. A small-diameter gold or aluminum wire is bonded to the pad area by a combination of heat and ultrasonic energy.

3.1.3 Double sided detectors

ATLAS C is the double-sided option with capacitively coupled rϕ strips. The main parameters are [16]:

- **Overall area** is 60mm $\times$ 60mm
- **Thickness** 300μm
- **Number of strips** 1536
- **Number of read out** 512
- **Read out pitch** 112.5μm
- **Substrate** high-ρ silicon, type negotiable
- **Strips** High doped p&n-implant. Pitch: 37.5μm
- **Strip dimensions:** Width 27.5μm (depends on isolation), length $\sim$60$\sim$mm
- **Read-out** 200 $\times$ 50μm bond pads, $\geq$ two rows, daisy-chainable.

In the double sided case the two detectors will be butt glued to form a 12 cm long mechanical unit and strips of the two detectors are electrically connected to form 12 cm long strips.

3.2 Electronics

The options for readout electronics are binary , analogue and digital. The main considerations for them are:

- Signal/noise
- Threshold control and implications for efficiency
- Noise rate, resolution
- System performance including debugging, stability

The analog front end building blocks are manufactured in ASICs and their functions are described in section 4.3. The choice of readout pitch depends on the type of readout electronics. For a binary scheme a pitch of 75μ m is required (giving a total of 4.4 M readout channels). For analog readout (which is the one that Oslo group is working on), an equivalent resolution can be obtained with a larger readout pitch, choosen to be 112.5 μm (2.9 M channels).

3.3 Heat production

The ASICs used in the inner-detector are the main factor in producing heat. The produced heat must be removed by special cooling loops, to avoid a temperature rise of the detector elements leading to increase leakage current.

Chapter 4

ATLAS analog readout of silicon detectors

4.1 Introduction

Several ATLAS front-end prototype systems have been built. They are basicly divided into analog and digital concepts. The analog ones concerning the inner detector fall into two categories. One of them is the FElix chip and the other one the APV5. The latest versions of these chips were constructed with 128 channels. The evaluation of front-end electronics concepts has been made by lab tests and special tests at the H8 beam line. In this thesis the FElix chip is the main concern.

A better understanding of the read-system for an experiment such as ATLAS demands to have some knowledge about the basic parameters of the machine. The noise is a factor which affects greatly the read-out system. In the following will be given some information about the origins of noise in the system.

4.2 Noise in the system

When small signals are amplified or measured, we can usually reach a lower limit of signal that is detectable. This limit is set by spontaneous fluctuations in the equipment we are using. This spontaneuos fluctuations are called noise, since if the audio-frequency component of the fluctuating voltage were amplified and fed to loudspeaker, we would hear a hissing noise. This type of fluctuation extends across all frequencies.

We use the term noise to describe random noise of a physical origin. Noise can be characterized by it's frequency spectrum, it's amplitude distribution and the physical mechanism responsible for it's generation.
In Si-detectors (see chapter 3) the typical charge deposited by a charge particle is refered to as one MIP. It is around 22400 e^-. Due to charge sharing between detector strips, even smaller charge have to be detected. It is essential to know the origins of the noise in the system. A limit on the noise in the system is imposed by the limit for a minimum detectable signal. The noise contribution in the read out electronics originate from Si-detectors, circuit components and amplifying devices. The most dominant noise is from the detector capacitance, therefore the preamplifier/shaper are optimized with respect to noise with respect to a given capacitance.

The term ENC (Equivalent Noise Charge) expresses the noise in a system. The total noise composed of detector element and the front-end's preamplifier/shaper is shown in equation 4.1:

$$ENC^2 = \alpha \ \frac{C_{in}^2}{T_p} + \beta \ T_p + \delta \ C_{in}^2 \tag{4.1}$$

$$ENC^2 = \sigma_s^2 + \sigma_p^2 + \sigma_{Flicker}^2 \tag{4.2}$$

in which:

C_{in}= The total input capacitance

T_P = The peaking time in amplifier

α, β and δ depends on the technology (Bipolar or MOS)

The lower cases s, p and Flicker in equation 4.2 stands for series, parallel and Flicker noise. They are defined as:

- Series noise. It is the equivalent noise voltage at the input of the amplifier. It is proportional to:

$$ENC_s \ \propto \ C_{in} \ and \ \frac{1}{T_P} \tag{4.3}$$

In MOSFET typically this kind of noise originates from the channels thermal noise.

- Parallel noise. This is equivalent current noise. It has the following relation:

$$ENC_p \propto \sqrt{T_p} \tag{4.4}$$

For MOSFET ENC_p typically comes from leakage current (shot noise) and thermal noise from the feedback and biasing resistor in the amplifier. The leakage current from detectors is dominant factor especially after hard radiation. A FET provides the lowest possible noise, but only for shaping times >30 ns, because their noise is reduced by increasing shaping time.

- Flicker noise. It is dominating at lower frequencies, and it increases proportional to the input capacitance.

$$ENC_{Flicker} \propto C_{in} \tag{4.5}$$

The Flicker noise have little influence in the system, because of the system's high rate.

In the following the noise creation in the FElix chip will be given. The FElix structural blocks as described in chapter 4.5.1 are a preamp./shaper, ADB and APSP.
Noise is any undesired fluctuation which appears superimposed upon a signal source. The most important sources of noise occur near the beginning of the signal chain (at the preamplifier input) where the signal level is at a minimum level. Noise generated at this stage undergoes the same amplification as the signal, whereas noise generated further along the signal chain is much smaller than the signal. Therefore it is important to reduce the noise at it's early stage, before entering the preamplifer unit of the FE-end chip.
Sources of parallel noise include fluctuation in the leakage current of the detector and in the current drawn by the input stage of the preamplifier. The series noise include the thermal noise in the FET's junctions of the preamplifier input [17].
The amount of noise added by the preamplifier is expressed in term of ENC. This is defined as the amount of charge which , if applied suddenly to the input of the system, will give rise to an output voltage equal to the RMS level of the output due only to noise.

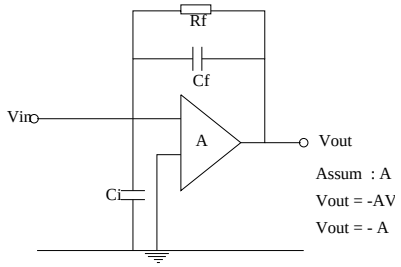


Figure 4.1: An illustrative preamplifier stage used in the FElix chip.

4.3 Analog read-out signal processing

Our main concern in this thesis is the analog readout. The output from a Si-sensor appears as charge Q, which is liberated by an incident particle. This charge is very small, therefore we need to to have a signal processing chain. The functional blocks of this signal processing will be given here. The analog read out chain for ATLAS is as follows:

- Preamplifier: It is the first element in the chain and acts as an interface between the detector and the remaining pulse processing electronics chain that follows it. As described in chapter 4.2 this unit is very sensitive to noise. In order to reduce the S/N the capacitive loading on the detector must be as low as possible. The input capacitance for Si-detector can vary due to radiation. So the preamplifier must be a charge sensitive amplifier (see fig. 4.1) in order to be almost unaffected of the input capacitance (C_{in}) variations. This design is good since the duration of input pulse received from detector is low compared to preamplifier time constant ($\tau = R_f\ C_f$). The input capacitance C_{in} arises from inherent detector capacitance. The performance of a readout depends largely on the design of the preamplifier. Ideally the preamplifier should be fast, have a good noise performance and dissipate little power. This preamplifier combind with the shaper perform a 3 $\times$ BCO time constant(τ=75 ns).

- Shaper: The shaper has been adopted to reduce noise effects through the chain. This stage is called shaper and here the pulse shaping occurs. The shaping time has been choosen to 3$\times$BCO. The reason is due to selective filtering to remove as much broad spectrum noise as possible without severely attenuating the signal components.

- Analog Delay and Buffering (ADB): The analog pipeline consists of a number of switched capacitors that can be connected for a short time period to the charge sensitive amplifier and therefore memorize the amplifier output voltage.

- Analog Pulse Shaper (APSP): At this stage the original shape of the signal will be retrieved. The method used is called deconvolution and it is explained in more details in chapter 4.4.

Electronics and computing play crucial roles in experiments like the LHC experiments. The Si-sensors used in ATLAS inner detector produce electrical signals which the electronic circuits process. These signals then can be fed into computers which are used for further data analysis.

The LHC runs at 25 ns BCO. It means that at each second there will be 40×10^6 interacting bunches. At this high rate it is impossible to process and record all out-comes due to very large amount of particle hits. To detect the out-comes from the events, we have to choose the interesting events in order to reduce the amount of data. **Triggers** are very sophisticated circuits to process signals and make fast 'decisions' as to whether the information from a collision is worth recording. These triggers set off the whole complex chain for recording data from the experiment. Last, but by no means least, computers are necessary to take the recorded information and reconstruct what happened immediately after a collision, as the newly made particles flew out through the apparatus. It is from these 'events' that the physicists can eventually build up a picture of the underlying physical processes.

4.4 The deconvolution method

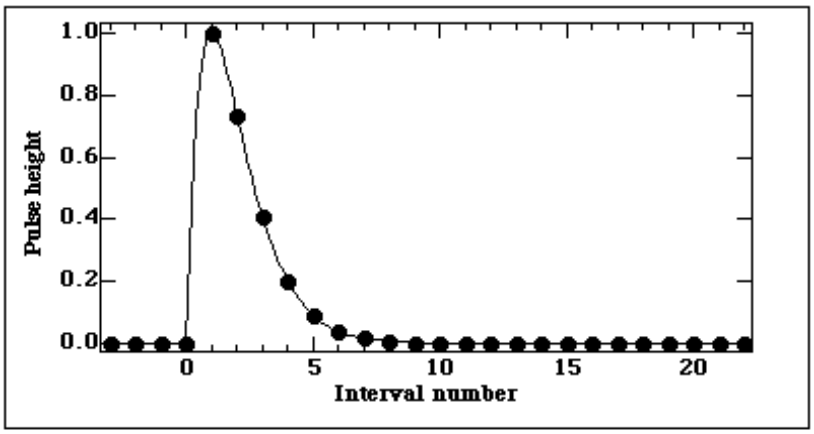
One of the most important techniques in the analog signal processing method applied here, is deconvolution. In the following some brief information about this technique applied on the ATLAS's analog read-out system will be presented. The unit inside the FE ASIC chip which corresponds to this function is called the APSP.

The detection of events after p-p collisions at LHC will require the observation of interactions at intervals of 25 ns (fig. 4.2a). To improve the S/N and reduce power consumption the FElix circuit will apply a shaping time of 75 ns (3 BCOs as shown in fig. 4.2b) and reconstruct the original input by deconvolution in the APSP. The APSP bases the deconvolution on information of the first 75 ns. The assumption is that the pulse reaches it's maximum amplitude within a single BCO. If there is no pile-up this max. hight correspond to the value of the 3rd nonzero sample i.e. 75 ns after the event.
The shaped signals can not be continuously deconvolted because of the very high speed in which would consume a lot of power. The preamplifier/shaper signals therefore are delayed in ADB. Discrete time filtering of is done by extracting data from ADB right after a first level trigger T1. If T1 comes, four delayed samples associated with this event are indicated and marked and transfered to APSP. A finite impulse response filter deconvolutes the sampled voltages of a shaped pulse to retrieve the original impulse signal with high precision. As mentioned in chapter 4.5.1 convolution takes place in CR-RC shaper after preamplifier. The basic principles of signal processing which determine the choice of amplifier time constant in a system where signal to noise is of paramount importance are described in more detail in [18] and [19]. In general analyses it can be shown that, in a system described by a time constant , the equivalent noise charge (ENC) is related to the detector capacitance in a simple way

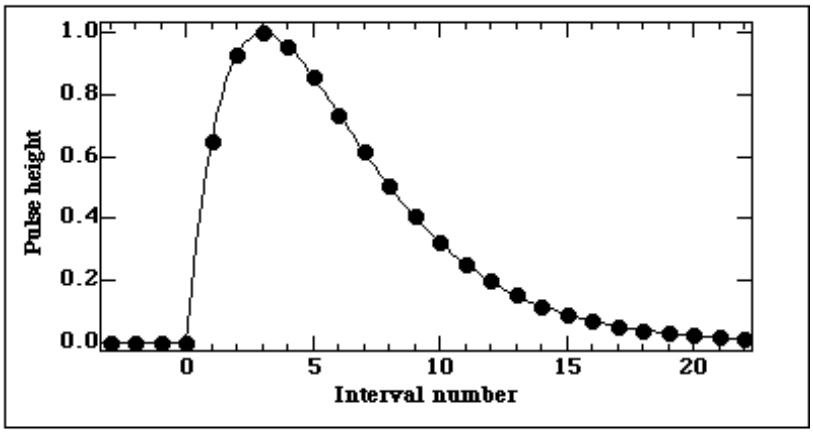
$$ENC = \frac{\alpha C^2}{\tau} + \beta_\tau + \sigma C^2. \tag{4.6}$$

In this expression C represents the total capacitance appearing at the amplifier input and is generally dominated by the detector capacitance in most systems of interest for particle detection. α , β and σ are constants determined by the choice of technology and the noise sources characteristic of the amplifying elements employed. Modern electronic circuits are realized in either bipolar, MOS or JFET form. For low noise circuits CMOS technology has become the preferred choice. CMOS has the potential for achieving simultaneously adequately low noise and low power dissipation. This is of great interest in high density applications, such as those employing silicon micro-strip detectors. However, for applications where very fast response (<25 ns) is vital, bipolar transistor circuits can offer similar noise performance and improve on the power consumption attained by CMOS designs using short time constant [20].

The possible drawbacks of slow pulse shaping are higher shot noise after radiation damage to the detectors and inferior timing resolution. Read out of detectors at high rates, with high efficiency for genuine events and excellent rejection of noise, requires the achievement of several goals simultaneously: sufficiently low noise for adequate signal discrimination, max-



(a)



(b)

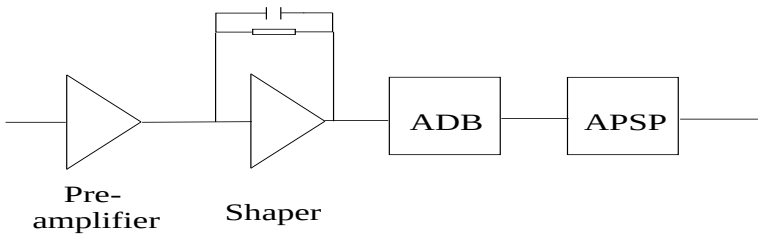
Figure 4.2: Typical amplifier pulse shapes for (a) short shaping times (τ=1)and (b) longer shaping time pulse (τ=3). Time units are in beam crossing intervals (25 ns at LHC).

imal charge collection and timing resolution which associates observed signals to a specific beam crossing. Whereas schemes with very fast shaping times and simple discriminatory threshold cuts encounter problems with full charge collection and sufficient noise rejection, the approach of using slower shaping times and time over threshold discrimination will make the timing requirements harder to realize due to inevitable time-walk.

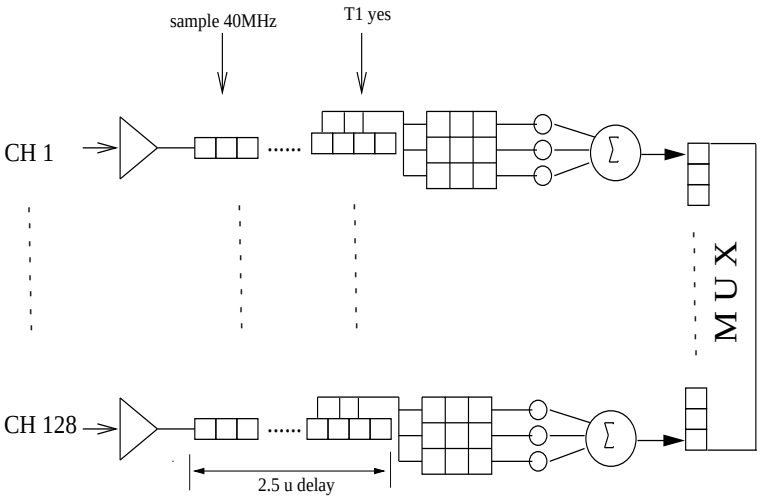
An alternative approach is to recover the original impulse-like signal which generated the pulse shape we observe. Real signal impulses occur only at beam crossing times, while noise, which can give rise to both positive and negative going impulses, occurs at random moments in time.

It is shown that better immunity to leakage current increases is provided by this method than by simply using a shorter time constant, while excellent timing resolution can simultaneously be obtained. In circumstances where leakage currents do not lead to excessive noise the advantage of full charge collection and lower noise signal measurement, obtained via slower shaping time, can be fully exploited. The technique is applied by forming a weighted sum of the sampled output voltages of the amplifier from three successive time intervals. An important consequence of the method is that it can be implemented as an elementary CMOS circuit with negligible power consumption.

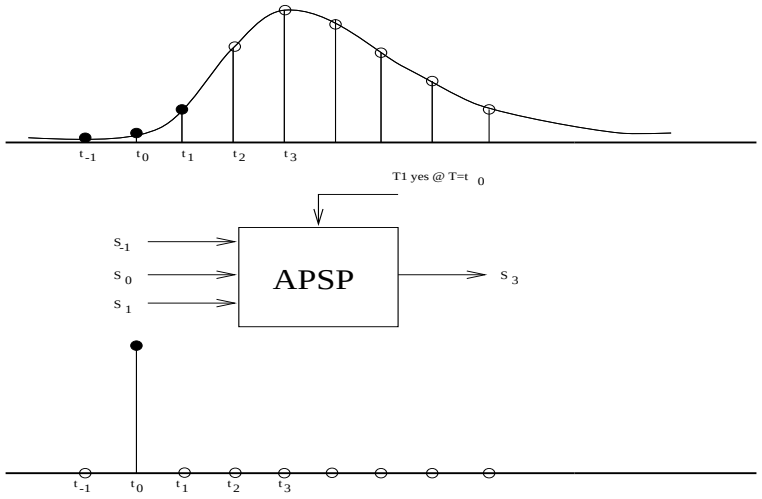
The APSP is activated on a level-1 trigger and the APSP thus consumes very little power on average. The chip has possibility to output both the deconvoluted or peak outputs. The signal out from FElix will be put on a multiplexer (MUX).



The signal path through FElix.



Peak/deconvolution mode.



Deconvolution mode.

Figure 4.3: The principle behind deconvolution. The problem is how for a given input signal s(t) and a knowledge of the impulse response of an amplifier h(t), can the the initial signal be retrieved from the the measured output of the amplifier, v(t)? The figures shows a system which is able to do it.

4.5 Front-end circuits

Every channel of the Si-detector needs a complete electronic read out chain. Since the charge pulses received from detectors (see chapter 3.1) are very small, the amplifying electronics must be placed very close to the sensor. The silicon detectors[1] and amplifier circuits will be mounted on a substrate.

By striking a high energy elementary particle to the sensor, an appearance of charge pulse is occurred in the channels which are closest to the struck point. The charge pulse then will be read by the FE circuits. The FE chips are designed according to RD20 front-end concept. The chip is put on a full CMOS implementation. A fast preamplifier circuit is combined with a slow shaper circuit to achieve full charge collection with full optimal noise and acceptable power consumption. The input stage is followed by an analog delay and buffer unit to preserve the information of a particular event until the arrival of a first level **trigger** signal.
The signals are multiplexed for further data processing. The multiplexing of FElix data are done by an analog multiplexer (AMUX). More information about this multiplexer and its signals can be found in APPENDIX C.

The charge pulses which occur are normally very small. The S/N ratio[2] in the front end electronics is therefore of great importance. Allowing a shaping time of signals long compared to the bunch crossing time necessitates a method to retrieve exact timing information. This is done by deconvoluting the sampled pulse shape with a relatively small analogue deconvolution circuit (APSP). More information about deconvolution was given in the previous section.

4.5.1 The FElix FE-chip

This chip is designed according to analogue option and follows the same principles for analog readout as described above. The chip has been made in many versions. In the following the chip's specification will be given according to the most recent version. The chip described here has 128 channels. Table 4.1 gives some of the most important features of the chip. FElix is composed of a preamplifier, an analog delay and buffer (ADB) and an analog signal processor (APSP). The FElix is designed to run with a BCO of 40 MHz and at T1 rate of 100 KHz.
The detector signal will be first amplified in a charge sensitive preamplifier, it is designed to amplify the received signal from Si-detector strip. The signal is then put through a CR-RC shaper. Here the signal will be shaped with a tunable time-constant. This time constant is choosen to be 75 ns, but there exists possibilities to change it by tuning the voltage VFP and VFS. The output from shaper will be sampled onto the ADB. The ADB is realized in the form of 84 switched capacitors that memorize the output voltage of the shaper. The samples will be delayed in ADB by 2 μs, the time required for the trigger T1 decision to arrive.
The clock rate is the same as BCO rate (40 MHz). This clock signal in our notation is

[1] I have frequently used Si-detector or sensor, these two terms means the same here.
[2] It is the relation of signal / noise.

FElix	Specification
Noise	< 1300e at 18pF input capacitance
Pulse duration	<15 BCO
Double pulse resolution	<50 ns
Power	<4.8 mW/ch
Pipeline length	2 μs
Die size	6.8×12.4 mm^2
Channels	128 channels

Table 4.1: The Felix integrated circuits, an analog read-out.

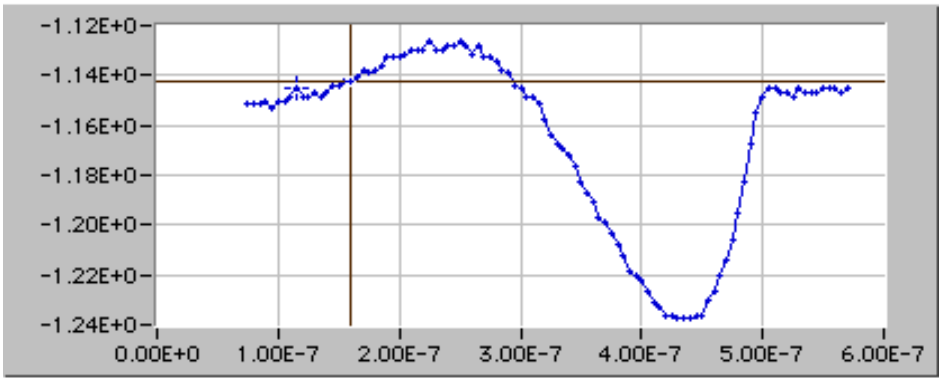


Figure 4.4: Peak pulse amplitude vs time.

labeled by BCOP. There is another clock called BCON, too. The reason for having this signal is only due to differential signal transferring. By means of clock the signal will be put from the shaper through capacitors dedicated to each channel.
On a positive T1 three of the four samples associated to the trigger are passed on to the APSP where a deconvolution filtering takes place. The fourth sample is passed directly to chip output and it represents the peak value. Thereafter the deconvoluted signal is put out. The FElix is equipped with 128 of these channels. The peak and deconvoluted signals are shown in fig. 4.4 and 4.5.

In section 6.6.3 is given information about the generation of different biasings. The prototype of FElix analog read-out chip for silicon tracker of the ATLAS detector has been fabricated by Austrian AMS in 1.2 μ CMOS technology. Table 4.2 lists the chips biasing and digital control signals. The FELix chip is constructed at SI[3] in Norway. This chip works on principles defined by the RD20 collaboration. All the functionality described here is concerned with one single channel.

[3]Center of industry research at Oslo

Pad /signal name	Nominal value	Description
CAL	0.1 V	Inject to all FElix channels
CAL10	0.1 V	Inject to every tenth channel
GND		Analog ground
VFP	-0.4 V	Voltage Preamplifier Feedback
PREB	700μA	PREamplifier Bias
VFS	0.3 V	Shaper feedback voltage
SHAB	120μA	Shaper bias current
BUFB	80μA	Preamplifier/shaper output buffer
VDC	-0.9 V	Backplane ADB storage capacitor
AVDD	+2 V	Analog power
AVSS	-2 V	Analog power
DVDD	+2 V	Digital power
DVSS	-2 V	Digital power
BCOP	ECL	Positive ECL input, 40MHz
BCON	ECL	Negative ECL input, 40MHz
RESETBP	ECL	Positive input, to RESET FElix
RESETBN	ECL	Negative input
DTAB		Open drain inverted output
DTA		Open drain output, data available
T1P	ECL	Positive ECL input, to trigger the FElix
T1N	ECL	Negative ECL input
BUSYP	ECL	Positive ECL input
BUSYN	ECL	Negative ECL input
VBP	-1.1 V	APSP backplane capacitor
APSPB	20μA	APSP bias current

Table 4.2: Biasing and digital control signals for FElix 128-channel.

4.5.2 The FElix test signals

In the following will be given some explanation about some of most used signals in our tests. Data is read from the ADB under the control of the trigger input T1P and T1N. Triggered data are retrieved from the memory automatically and output (after a processing period). To optimize timing resolution a deconvolution filter is enabled, which then enables a switched capacitor filter embedded in the chip that operates a deconvolution based on 3 weights. This then confines the signal to one beam crossing BCO.

- **Broken channel**: The FElix is equipped with a broken channel. This channel is broken between the preamplifier/shaper and ADB.
- **CAL**: It is a test signal applied to all FElix channels. The signal amplitude is 0.256 mV. Internally in the FElix it goes to separate capacitors (each of 56 fF) for each

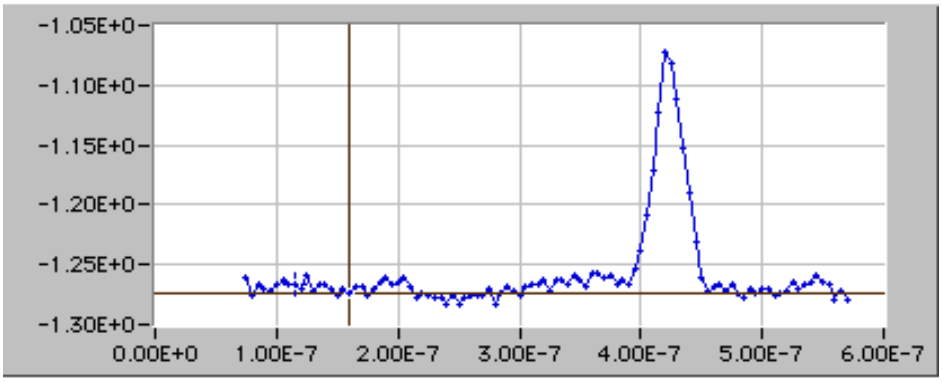


Figure 4.5: Deconvoluted pulse amplitude vs. time.

Pad name	**Description**
CAL	Calibration signal for all FElix channels
CAL10	Calibration signal for every tenth FElix channel
IAMP	Test signal to the broken channel

Table 4.3: Input test signals

channel and give rise for a charge injection near to one MIP [21]. The equivalant capacitance of these internally capacitors will be about 2pF. The following equation shows the relation between applied voltage and charge:
Q = C V = 2 pF $\times$ 0.256 V = $\frac{5.12\times10^{-13}FV}{128}$ =4 fC pr channel. It results to an equivalent electron number as : $\frac{4fC}{1.6\times10^{-19}C} \approx 25000$ e^-. Electron charge charge is $1.602 \times 10^{-19}C$.

- **CAL10**: An input function like CAL but applied to every tenth channel.
- **DTA**: The DTA signal indicates that there are valid signals out from APSP. The DTA is high for the period at which there is valid signal out. The DTA and it's invert DTAB[4] signal are brought out from FElix. These signals tell about whether the digital logic is functioning or not [21].
- **Dummy channel**: They have bonding pads on the chip. These bonding are not connected to any involved internally on the chip. The purpose of using these signals is only to reduce pick-up effects.
- **IAMP**: This signal is a test signal used for a charge injection equivalent to a MIP into a broken channel[5]. In our schematics the inputs to these broken channels are labeled as IAMP2 and IAMP3 which are arrived from the PCB through connectors U_{14} and U_{15}.

[4]The purpose of invert signal is to reduce the noise pickup.
[5]This channel is broken at the passage from the shaper to the ADB.

On the hybrid there are 1.8 pF capacitors in which release a very fast current pulse in response to an applied voltage. This is due to this relation: $V=\frac{Q}{C}$, if the applied voltage is supposed to release 22400 e^-, then we will get: $V=\frac{22400}{1.8\ pF}\approx 2$ mV. This signal arrives on a coaxial cable, and therefore we have to terminate it with a 50Ω resistor on the PCB to avoid reflections.

- **OAMP**: This signal is the output from broken channel. On the PCB it is put on a line driver OPA633 and is carried out through lemo connectors U_{10} and U_{11} to be sent to either the control room or to a local oscilloscope.

4.5.3 Design technology

In order to optimize power and noise performance, the FElix electronics is made on CMOS ASIC chip with 128 channels. This means that it is an IC unit, comprising of a number of electronic circuits which are fabricated on a single chip. This kind of design is called ASIC (Application Specific Integrated Circuits).
The MOSFET circuits are formed on the Silicon substrate by pattern of active and insulating regions [22].
The insulation region is normally silicon dioxide. In the MOS device the controlling gate voltage is applied to the channel region across an oxide insulating material.

The major advantage of a MOSFET is low power dissipation due to its insulation from source and drain. Other advantages are its process simplicity and the ease of interconnection on chip. MOSFETs are of both P-channel and N-channel types and are sometimes called "insulated gate field effect transistors (fig. 4.6).

CMOS stands for complementary metal-oxide semiconductor, in contrast to NMOS (N-channel Metal-Oxide Semiconductor) and PMOS (P-channel Metal-Oxide Semiconductor), CMOS is constructed using complementary (N- and P-) MOS field-effect transistors. CMOS has lower power consumption per gate and the highest gate densities per die.

The technique used in making chip is called planar silicon crystal wafer technique. This method combined with thin-film technology are central keys in making IC's. Planar silicon crystal technic permits active components to be defined on wafer separated by an insulating oxide layer or region.

Thin-film technology then enables us to define active components or isolating regions on the wafer by means of a photolitographic process [22].

Electronic circuits operate by the movement of charge from one circuit element to the other. Since CMOS use combinations of P-MOS and N-MOS transistors only one transistor of each pair can switch states at a time. Under DC or low frequency conditions, this logic design style allows steady state current to dissipate only through leakage. Relatively large power is dissipated only during transistor switching at mid- to high-frequencies [23].

4.6 Two module alternatives

At the present time the ATLAS experiment consider two different module concept. To some degree there is a coupling of these module designs to options in the design of the

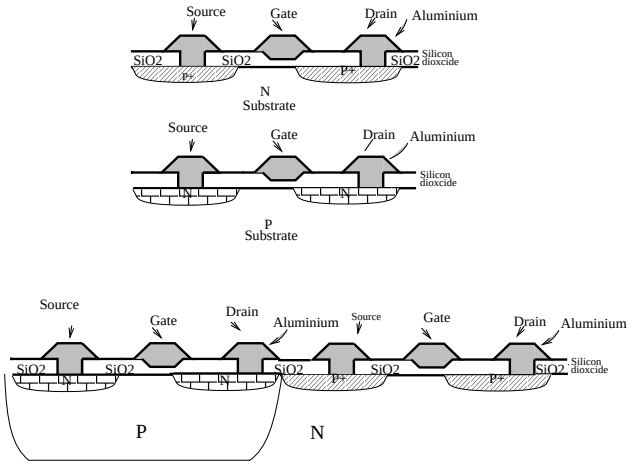


Figure 4.6: a) MOS-FET transistor: b) Silicon Gate MOS transistor.

mechanical support for the barrel layer. These two modules are rϕ and Z-module. The major considerations in choosing the best option are:

- The electrical and thermal performance.
- The ease of construction.
- Robustness and cost.

4.6.1 rϕ-Module

This module is named so because of it's FE-chips orientation which is in rϕ directions. The front-end chips are mounted on top of the silicon detectors (fig. 4.7). This is the natural configuration for the electrical connections but complicates the cooling, especially for a stave-based solution [9]. The front-end electronics are directly on the middle of the module. Reading-out signals at the middle of the strips results in the minimum noise and the maximum signal, since the input resistive-load is 1/4 of the load of reading-out at the end, and the signal dispersion through the strips will be smaller. Placing the hybrid at the middle of the module leads to keeping the vulnerable wire-bondings and hybrids away from the edges. Open edges eases the overlapping of the modules in both ϕ and Z directions. This kind of mounting the modules near the center equalizes the temperature distribution within a module. One $r\phi$-module is made of two 6cm$\times$6cm silicon micro-strip detectors. Two detectors will be butt-glued to form a 12 cm long unit and strips of two detectors are connected electrically to form a 12 cm long strips.
The area of 6cm$\times$6cm is nearly the maximum to be fabricated in the standard 300 μm thick silicon wafer. The length of one detector can be choosen to be 6.0 cm based on an arguments for pitch and a stereo angle of 40 mrad. The width of the detector varies by the choices of strip pitch, number of strips, and the required spaces around the edges for bias

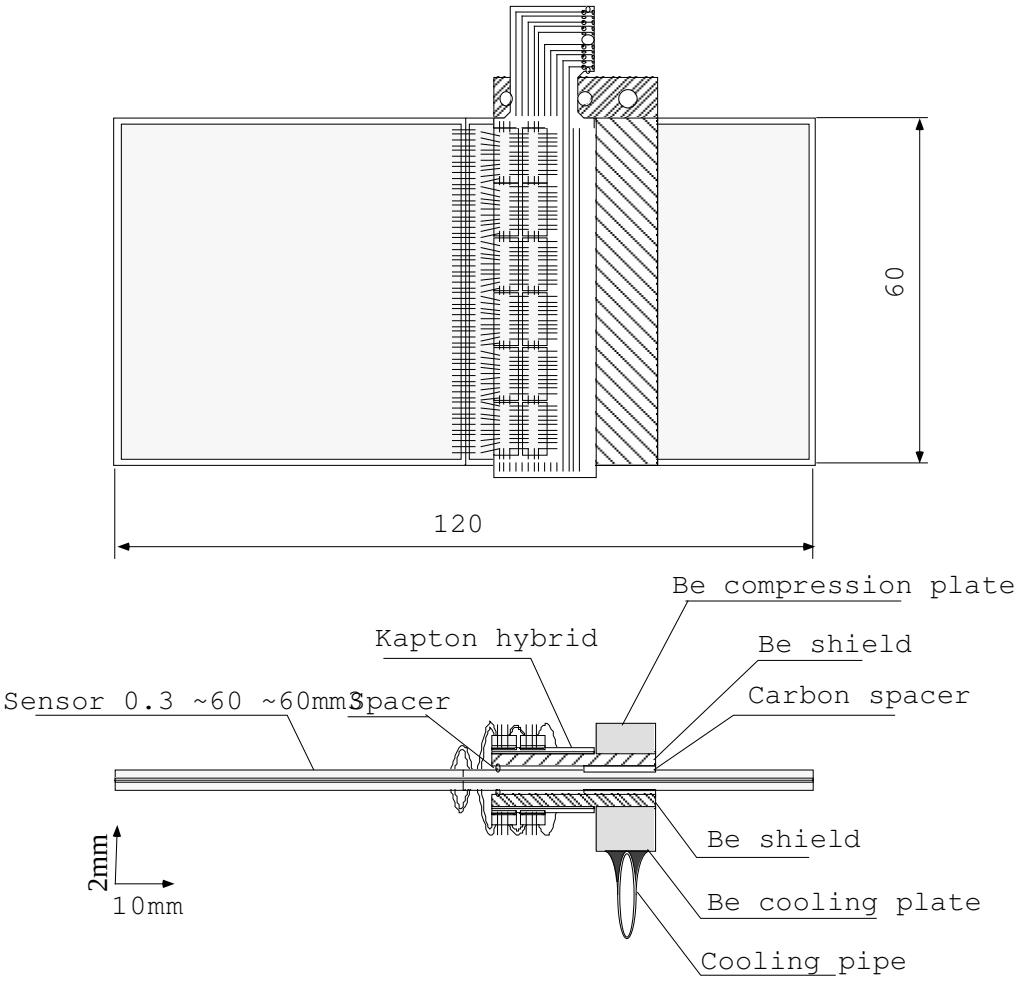


Figure 4.7: R-ϕ module

ring, guard ring[6], and edge-clearance. To measure two dimensional information in a module, two measurement planes are integrated. One plane has strips parallel to the z direction, called the axial strips, and the other has skewed strips to the axial strips by an angle of 40 mrad, called the stereo strips. These two measurement planes are to be realized by single double-sided silicon micro-strip detectors or two back-to-back glued single-sided detectors.

4.6.2 Z-module

In this module design the hybrid is placed at the side-edge and the module is equipped with fan-ins. They interconnect the strips and the FE-chips.

Fig 4.8 shows the design for Z-module. The detectors and the hybrid assembly are

[6]The aim of guard is to reduce the leakage current in the guard region when high depletion voltage is applied.

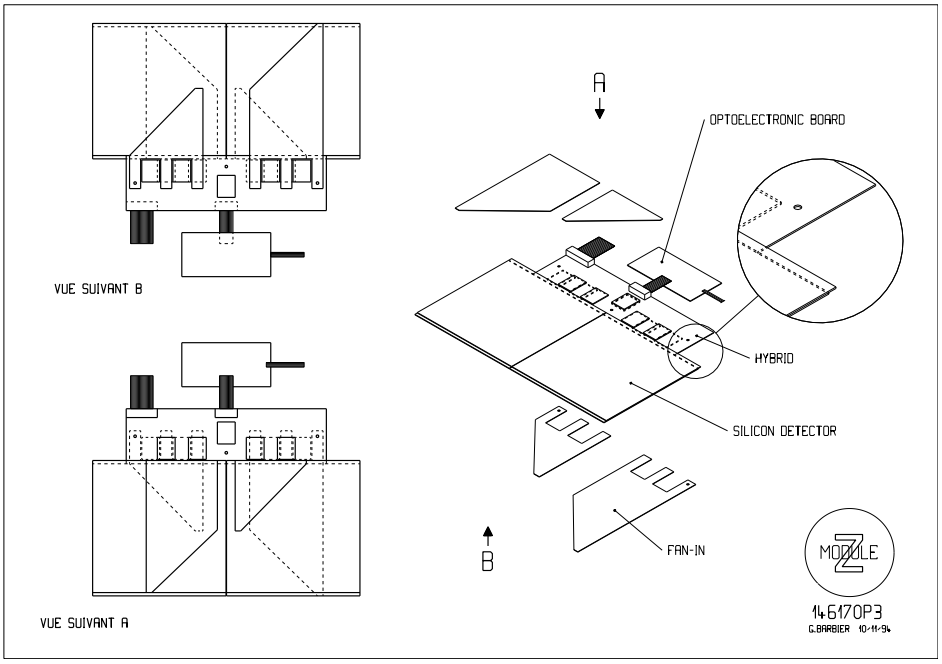


Figure 4.8: The 'Z-module' showing bottom,top and exploded views of the module.

adjacent to each other. The cooling runs along the hybrid in Z direction and makes contact between readout chips. The front-end electronics and silicon strips are interconnected by beryllia fan-ins (figure 4.8) which also serve to cool the detectors. Detectors are either back to back single sided or double sided. The hybrid supports the front-end electronics and provides the control, readout and bias lines. The front-end chips are placed on both sides of the hybrid. One advance of this design is that the front end electronics is decoupled electrically and thermally from the silicon. Another advantage is that the cooling paths are short into the detectors [9].

4.7 Modular design

The ATLAS SCT is a modular design. The module compose the fundamental sub-unit for each silicon strip SCT layer. All four barrel cylinders will be built of identical modules, each consisting of two pairs of identical detectors mounted back-to-back. The detector module will be made of two 6 $\times$ 6 cm double (single) sided silicon micro-strip detectors.
We combine 14 back to back glued Si-detector modules with their hybrid together onto a stave. These staves then will be assembled into barrels. With a modular design one achieves a number of advantages.
They give us an easier way to approach assembly, repair, testing and electrical isolation. This give us unity of design for layers in the inner-detector. Thus by a modular design, parallel production lines can be applied. Each layer will be tiled with a set of modules. A

module consists of :

- Active detectors - either one or two pairs semiconductor wafers.
- Front-end electronics.
- Read-out controllers
- Fan-ins and connectors.
- Opto-electronics for transmitting data off detector.
- Interface to permit cooling facilities.

Chapter 5

System overview

5.1 Hybrid and PCB

The Z-module is one of the options for ATLAS inner-detector. It consists of Si-detectors coupled by a fan-in geometry to readout chips. The FElix read out chips are used. The FElix is a front end chip designed to read out Si-strip detectors.
In the test phase we expose the Si-detectors to high energy particles at the H8 beam line. It is obvious that some circuitry is needed to take care after the signals left from the Si-detectors. These circuits are integrated into two separate boards. They deliver the necessary biases to Si-detectors and chips. The amplification and transmission of signals to the control room is done by these circuits. In our terminology they are called hybrid and PCB. The latter is the main subject of this thesis.

The major functionality of this board consists of interfacing the FElix chips (via hybrid) to the DAQ system, transferring control signals to FElix chips and transferring the AMUX read out signals to the DAQ system.
The PCB's functions are to supply all necessary biases to the hybrid and transferring control signals from control room. VME crates are at relatively long distances from the hybrid and the Si-detectors joined to it. The task of delivering for example the desired logic levels to the hybrid is done by the PCB bard. On this board we have mounted all circuits which are essential for transferring signals and biasing signals. In addition the PCB provides a great deal of flexibility in controlling biases. This is done by adding potentiometers to control biasings. An overview of the PCB in connection with the hybrid and it's basic functions is given in fig. 5.1. It is worth to mention that the dimensions are not the real ones in this drawing.
For simplicity at the test beam only one board was fully instrumented. A central controller VME generates the clock, trigger and control signals for the boards. The FElix test setup is a stand alone system to fully characterize the FElix chips.
In the future The PCB's functions will be implemented in ASICs i.e. they will have much smaller dimensions. It is necessary to have all the electronics close to the detectors because the signals received from detectors are very small and they will be exposed to large noise effects if we transfer them outside the barrel for amplification and processing.

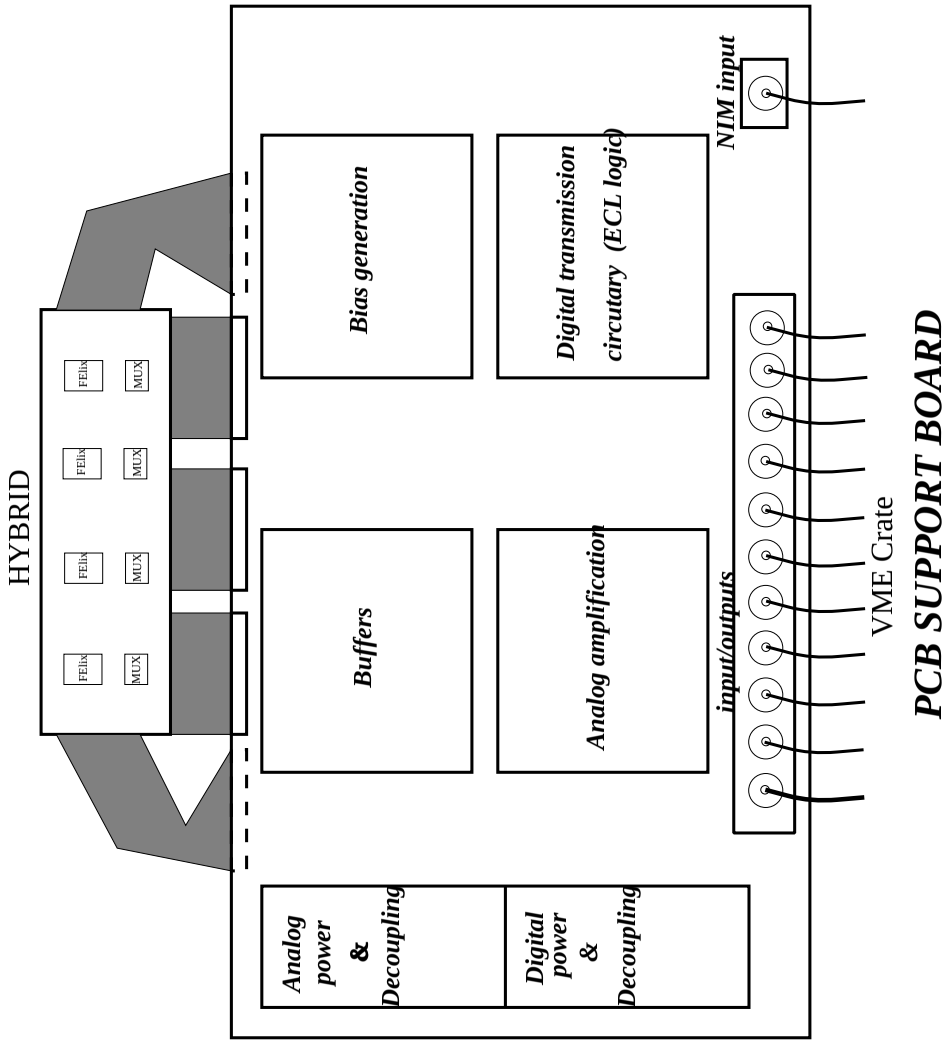


Figure 5.1: An overview of the basic functions of the PCB.

5.2 Hybrid

The signals received from each detector strip needs to be processed in the FE-chip. In order to connect the Si-detectors signals to each FElix read out channel and to supply all the FElix's 128 channels with bias and control signals we needed to have an underlying board supporting the detectors, FElixs and AMUXes. This board is called a hybrid and its main functions are the above mentioned tasks. In addition this board should have the the following properties:

- Good thermal conduction ability: Any increase in temperature has catastrophic effects in signal processing due to increased noise.
- Short radiation length: The hybrid will be a part of the final inner-detector. The inner-detector will be used mainly as a tracker, therefore the energy deposition must be as low as possible. The material used as substrate must have short radiation length.

The Z-module hybrid is constructed of alumina and patterned with thick film process. The use of fan-ins to interconnect the sensors and the electronics permits the chips and strips to be of a different pitch. The space available between chips can be used for bonding and biasing of the electronics and for the insertion of thermal fingers to improve heat extractions from the detectors. Two types of fan-ins are currently being studied, either in ceramics (e.g. beryllia) or in metallized kapton. Beryllia fan-ins are very effective for cooling the detector whilst providing additional mechanical support. These add to the overall material budget. One major concern in the design of the module is the simplicity of construction and stability of the system. Both can be enhanced by limiting the number of components used. The only active components mounted on the test hybrid are FElix and AMUX chips, the rest are capacitors, resistors and connectors.
The hybrid was designed to be used at the H8 test beam. This hybrid was made by a former HEP[1] student at Oslo University. For more detail description about the rules and process in making this hybrid refer to [21]. The hybrid design rules are listed in table 5.2, taken from [21]. Table 5.2 describes the biasing applied on the hybrid containing 4 FElix and 4 AMUX. Fig. 5.1 gives a view of the hybrid in connection with the PCB.

5.3 The PCB preparation

To make the final PCB we had been through several steps. At first we studied the signals and biasings which were foreseen to be applied on FElix and AMUX ASICs. Their digital signals are at ECL level, demanding to equip the PCB with a circuitry compatible to this logic level etc. The next steps to be followed were :

1. Schematic designs
2. Simulations

[1]High Energy Physics group at Oslo University

Specification	**Value**
Min. conductor width	100μm
hline Min. conductor distance	100μm
Min. via dimensions	200μm (diameter)
Min. via pitch	400μm
Min.	100μm
Bonding pad size	200μm x 400μm
Bonding pad size (Fodel)	100μm x 400μm

Table 5.1: **The hybrid design rules.**

Bias	**Implementation**
VBP	**Separate.** Decoupling on hybrid.
VDC	**Separate.** Decoupling on hybrid.
VFP	**Separate.** Decoupling on hybrid.
VFS	**Common.** Decoupling on hybrid.
APSPB	**Separate.**
BUFB	**Common.**
PREB	**Common.**
SHAB	**Common.**

Table 5.2: Biasing needed on the Z-module test hybrid.

3. Production

The above steps are described in detail in the subsequent chapters.

Chapter 6

The PCB schematics

6.1 Introduction

We made our schematic designs by a CAD tool called Viewdraw from Viewlogic. The active components used are line-drivers, receivers, op-amps and temperature sensors. In addition there are a large number of passive components. In order to process the schematics to make the layout and simulations, it is necessary to specify the components size, pin order and their simulating models. Most of the components with their models were available. But there were some components that I had to make myself in schematic form, and which I had to give true values and models.

6.2 Design constraints

The choice of right components is of great importance and therefore it was attempted to find the components with the right reliability. The most of resistors were choosen to be of the most reliable types i.e. 1% deviation from their stated value.
In addition there are a large number of passive components. We followed some basic rules to gain the highest possible noise immunity. These important rules are such as:

- The digital and analog signals are separate.
- Separate digital and analog power.
- Decoupling of all biasing and power.

Some other rules followed at this stage are as follows. Wires and current loops on the PCB will act as antennas, emitting electro-magnetic radiation. The same elements will act as receiver antennas for radiation. Therefore it is essential to design the system for low electro-magnetic emission [24]. To reduce these effects we used differential transmission for some signals.

- Cross talk: Small spatial separation between conductors results in capacitive and inductive coupling between the conductors and potential problems with cross talk. Cross

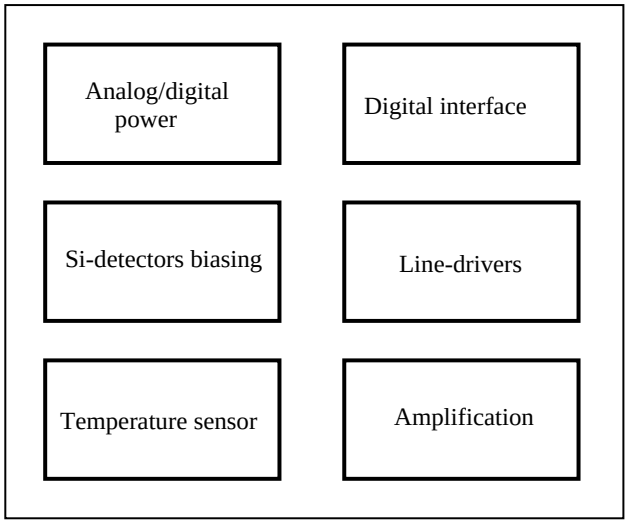


Figure 6.1: Top level design of the PCB.

talk is the main concern when defining minimal line separation for high frequency circuits. Cross talk and reflections are different types of noise. A third kind is switching noise. If the electrical current in a component is suddenly changed there will appear a transient signal on the power supply line due to the inductance in it.
It is important to reduce the crosstalk between analog and digital parts of the FElix and AMUX. This is done by separate power for analog and digital parts. It is important to ensure a high electrical conductivity in ground planes and power supply conductors. Decoupling capacitors between ground and power supply close to the critical components are also important, to absorb current spikes without corresponding voltage spikes.

The signals through long wires are degenerated by the finite bandwidth of the wires between active components on the PCB and in the VME system.

- Reflection: An unterminated signal path should be terminated by a resistor with the same resistance as the characteristic impedance of the signal carrying conductor line and as close as possible to the end of the conductor.

It is of a great importance to have impedance matching between input/outputs signals and transformation lines. The impedance matching plays an essential role in transmission, and we have impedance matching in our design everywhere signals enter a different media.

6.3 Top level schematics

The PCB design according to its functions is shown in FIG 6.1. As we can see the design is divided into six different parts. Each part has a specific function. The design is a combined

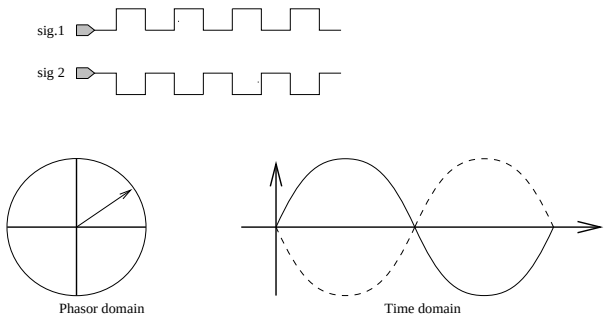


Figure 6.2: The transmission of a signal and its invert.

analog and digital. In the following sections it has been attempted to give more information about each of these functional blocks.

6.4 Digital interface

The FElix 128-channel has all its digital control signals as differential and can use signals directly from the SEQSI unit. The SEQSI unit is a VME based driving unit for the FElix-chip with ECL outputs. ECL has two negative levels, with H=-0.90 and L=-1.74. Therefore we have used ECL related ICs on the PCB to force these signals to the hybrid. The arrival signals from the sequencer are complementary, therefore we use differential mode. The distance between control rooms and the location of the PCB is about 25 m. In the test area there are a lot of electronic equipments, and they can be a source of induced noise to these lines. To reduce these effects and improving the transmission we had to supply the board with some circuitry capable to drive the signals in differential form, and retrieve the signals again. This has been made possible by using two ICs mounted on the PCB. One acts as a receiver (MC10H115) and the other (MC10H101) is a driver.
In the following will come some informations about the differential signals and some consideration which are taken into account in choosing this kind of signals. They are as follows:

- **Complementary signals:** It means that a signal and its complement are driven simultaneously.

- **Low cross-talk:** Is achieved due to low voltage swing of these devices. The swing is 850 mV. The signals are transfered in differential form on two lines, one carries the real signal and the other its invert. The advantage is noise reduction. The reason simply lies in the electromagnetic magnetic effects, if two signals have the same amplitude but with 180° phase difference, the resulting electro-magnetic effects from two path carrying signals will attempt to nullify each other. Otherwise the interference will occur and as a result noise can be introduced in our circuitry. fig. 6.2 shows a signal and its invert.

ECL logic have the advantage of low propagation delay (≈2 ns) with very low noise margin[1]. The ECL logic uses parallel transistors and series switches. The ECL is extremely high-speed. The ECL high speed comes from the fact that the transistors within the gates are never driven into saturation, eliminating the time required for the transistors to come out of saturation. fig. 6.3 shows how an ECL signal is created[2].
The digital control signals arrive at the PCB through a 34-pin connector (**CN26**). The Viewlogic schematic is given in fig. 6.4. The signals transmission in the above mentioned manner will in addition eliminate the noise peak-up on the board.
The MC10H115 receiver is used to send differential signals across the PCB. By using this chip the signals arriving in pair (signal and $\overline{signal}$) from SEQSI go through MC10H115. The output will have the same amplitude as the signal.
The MC10H101 is used as a driver from the PCB to hybrid. The signals from MC10115 are put to this chip. As the output from it we get again a pair of signals (signal and $\overline{signal}$). This chip is a good choice for transmitting signals across long lines. There are two possibilities to get signals BCON and BCOP; directly from the sequencer or via a lemo cable (NIM-level). By using lemo (U21 on schematic) we can adjust the the voltage by potentiometer, and we can use the common grounding on PCB (by means of CN18). To have impedance matching and avoiding reflections the resistor R31 is used.
As mentioned above all digital signals are taken from the sequencer. But for the BCO we have equipped the board with an additional option. This signal can be driven via a NIM[3] cable to the receiver input (MC10H115). This configuration is shown in fig. 6.4 on page 55. The signal arrive on U21. Transmission of logic pulses by NIM module is done by coaxial cable. The NIM logic levels are given in table 6.1 [17]. The fast-negative NIM is current based, with an output impedance at 50Ω. We have assumed that the current is -16 mA, this gives us a voltage about -0.8 V for logic 1 and close to 0 V for logic 0. The NIM signals swing is too low to be used as ECL logic. It is therefore necessary to convert the NIM level to ECL. The conversion is done by the circuit shown in fig. 6.3. The transistors shown in figure are a very simplified illustration of internal circuitry inside the MC10H115 receiver. For pure ECL inputs this circuit (inside the box) acts a comparator, it compares the twoinputs and puts out the one with higher voltage in ECL form. For our NIM option we have to make a DC-level (V_{DC}) as the inverting input (B input in figure), otherwise the output will stay at a constant level. The V_{DC}, the voltage across the invert signal (through pin 13 on the receiver) is choosen to be -0.4 V, this can be adjusted by trimming the potentiometer RP_{30}. Thus the the NIM input changes will be around the DC line -0.4 V. in the center of NIM signal swing. By this approach the output will become ECL levels. The digital interface is drawn in 6.4. Here all digital signals come through the PCB via CN_{26}. The signals and their invert are terminated with a 100Ω resistor before entering the ECL receiver circuit which is a MC10H115 chip. It is worth to mention that despite what we probably could expect from the schematic, all 100Ω resistors are hermetic in a single unit R_{52}. The resistors 47R on the

[1]The maximum noise voltage added to the input signal that does not cause an undesirable change in the output.

[2]As we can see from the figure this arrangement acts as Schmidt trigger.

[3]The standard Nuclear Instrument Module.

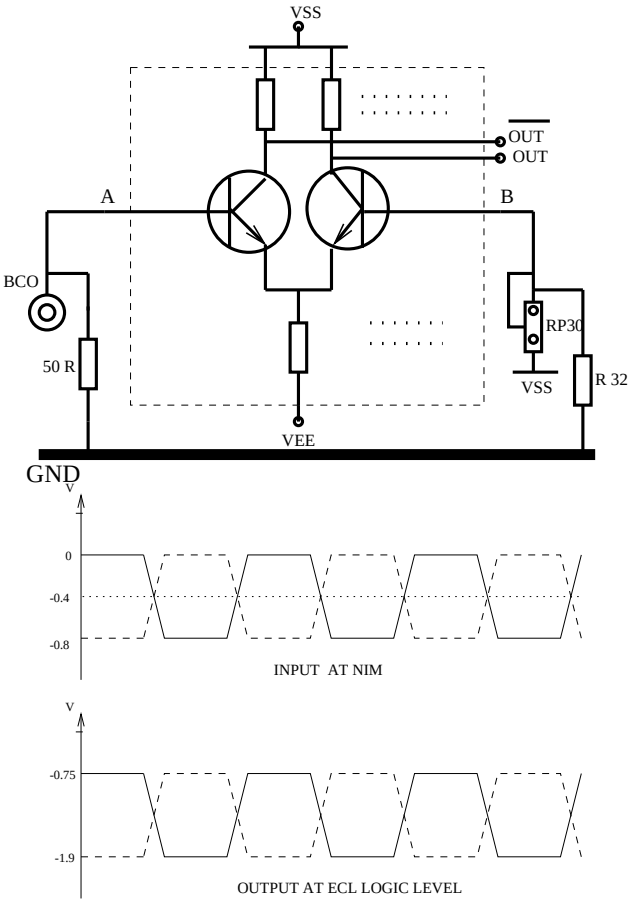


Figure 6.3: The conversion from NIM to ECL.

right hand of the schematic which are pull-up resistors, are also in one package[4]. They are labeled R_{37} and R_{38}. The same is the case for receivers, they are four equal circuits sealed in one package which in our design is labeled as U_5 and U_8. The driver circuits (labeled with U_6 and U_7) also are so. The same explanation is valid for ECL driver circuits[5] with U_5 as their label. The power named V_{EE} is adopted for ECL circuits, the required power for them is -5.2 V. There are connections between this supply and all ECL circuits.

Logic level	Value
H	-14 mA to -18 mA
L	-1 mA to +1 mA

Table 6.1: Fast-negative NIM logic

Signal name	**Description**	**#Pin CN26**	**#Pin CON5**
SAMPLE	positive ECL	31	3
SAMPLEB	negative ECL	32	2
MRESET	positive ECL	27	6
MRESETB	negative ECL	28	5
CLK	positive ECL	23	9
CLKB	negative ECL	24	8
RBIT	positive ECL	19	12
RBITB	negative ECL	20	11
BUSYN	positive ECL	15	14
BUSYP	negative ECL	16	15
T1N	negative ECL	11	17
T1P	positive ECL	12	18
RESETBN	negative ECL	7	20
RESETBP	positive ECL	8	21
BCON	negative ECL	3	23
BCOP	positive ECL	4	24

Table 6.2: Digital control signals.

6.5 Analog signals

There are some signals which are treated as analog. In the following will be given some information about these signals. The signals processed in the FElix will be put onto the

[4]Each package contains 8 resistors.

[5]This circuitry is adopted to drive ECL signals over long distances. The chip we have used here is a MC10H101 from Motorola.

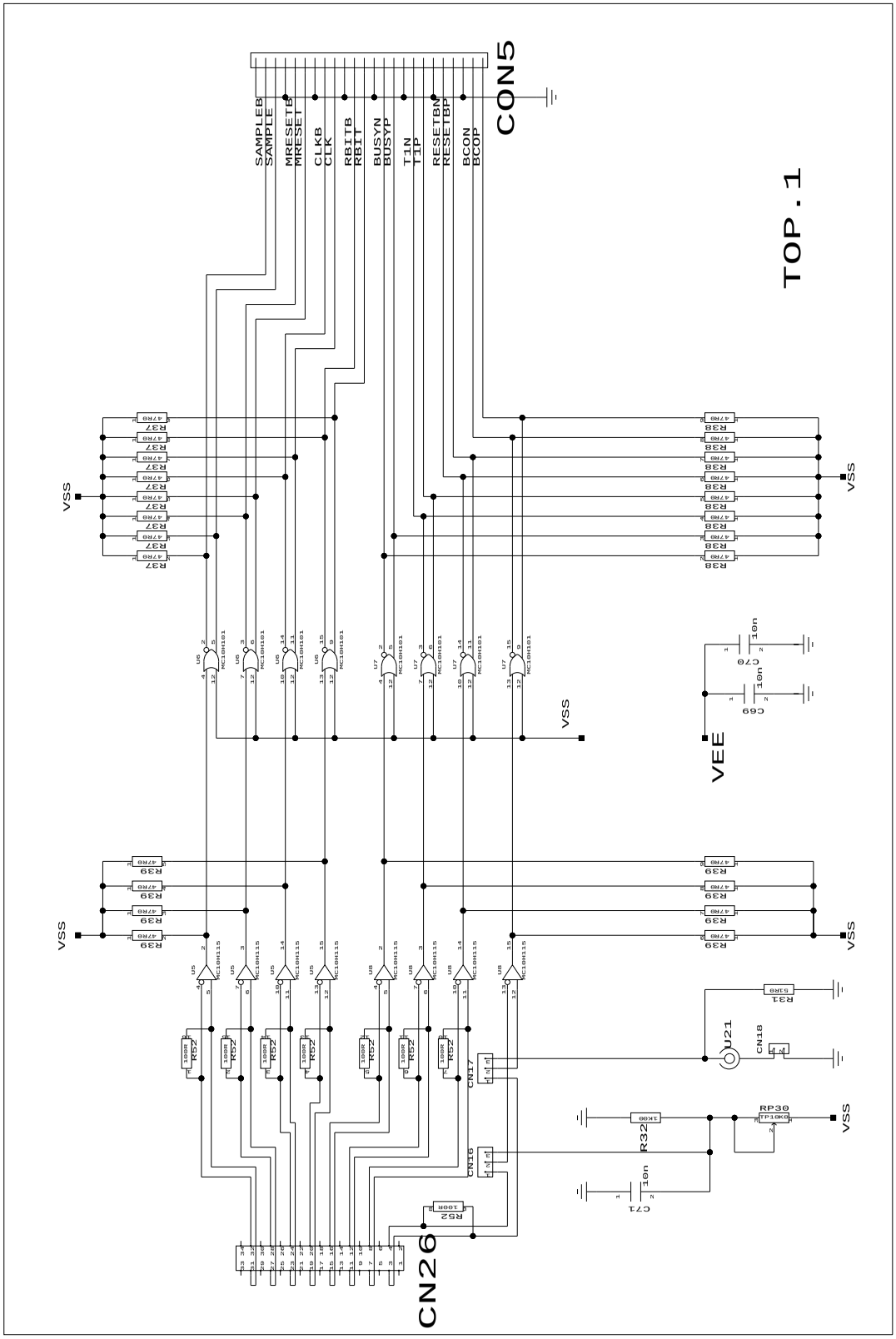


Figure 6.4: The schematic view of the digital signals.

AMUX. Then the multiplexer will put it out as an analog signal (MOUT) which represents the processed signal in the FElix and in addition provide another signal as a reference signal (OLEV). These signals are very weak, they have to be amplified before sending them to the control room (in test beam) or to the oscilloscope (in the laboratory). The amplifying task is done on the PCB board. The amplifying design has been made differential. The design is as a two stage amplification. fig. **??** gives a schematic view of this approach, used for Spice simulation. The same circuit is repeated in fig. 6.5 without Spice simulation tools.
This configuration is a **gain controlled** differential amplifier. The output from X_1 and X_2 are coupled to the inputs of X_3 which is the same type as the others. These inputs to X_3 form a differential amplifier. We call X_3 for a post-amplifier stage. The circuit prevents the gain from rising above 20 as maximum and almost 7 as the minimum. By setting (RP_1)=0 in equation 6.1, we will get the maximum gain. The equation 6.1 gives the total gain. The minimum gain is found if we set (RP_1)=5K, because the (RP_1) and (R_{42}) are in series.
This kind of design tends to suppress interfering signals from the environment. When the amplifier is connected to an external signal source through wires, those wires are subjected to fields from nearby wiring. In this situation the field from nearby wires affects both inputs to the differential amplifier equally, so the interfering signals are canceled out by the common mode rejection property of the amplifier. We must remember that this cancelation of signals is not perfect. The reason can lay in imbalances in the circuit either internal or external to the amplifier circuit [25]. When EL2244C is used in differential mode it has a CMRR=90. It gives a good suppression of the signals having the same amplitude.

$$A_v = [\frac{2R_{44}}{R_{42} + RP_1} + 1][\frac{R_{36}}{R_{18}}] \tag{6.1}$$

$$CMRR = \frac{A_{vd}}{A_{vcm}} = \frac{Differential\ voltage\ gain}{Common\ mode\ voltage\ gain} \tag{6.2}$$

The signals MOUT and OLEV are tailored to as none inverting. In this form the output signal is in-phase with the input signal. There is no need for impedance matching for EL2044C in the none-inverting design, because of it's very high input resistance. Design rules have been as the following. First we consider the voltage gain required by our amplifier. MOUT and OLEV have some difference. This difference can be amplified in a differential amplifier.
The gain for each stage is given by equation 6.3. The formula is with respect to external circuitry around X_1, but for X_2 the situation is exactly the same. The gain is choosen to be 3.

$$\frac{V_o}{V_{MOUT}} = 1 + \frac{R_{44}}{R_{10}}. \tag{6.3}$$

It is worth to note that on the PCB, we have omitted RP1 and R42 components. The reason for having them was to have a gain controlled amplifier.
We believed that a fixed gain at 3 for each none inverting stage could suffer a desired amplification, therefore we didn't equipped the board with (RP_1) and (R_{42}). The two amplifiers X_1 and X_2 form the none inverting amplification stages. They are identical i.e. the external components used to form the amplification have the same values. The magnitude of the output signal voltage is dependent on the input voltages from hybrid (MOUT and OLEV)

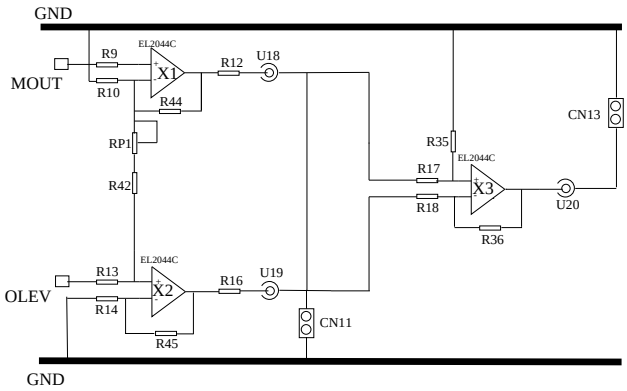


Figure 6.5: The amplifying stage

and the value of resistors around the op-amps.
In tests done at Oslo's ATLAS laboratory the goal was to measure the outputs form amplifiers X_1 and X_2 which are constrained as inverting. The amplifiers performance was tested in the configuration shown in fig. 6.6. The output impedance are matched to a coaxial cable. In the lab tests we tried to find the amplifiers time constant in single mode. It showed that it fails to amplify the signals at frequencies higher than 9 MHz. At higher frequencies it could not deliver the desired amplification. This op-amp has lower f_{3db} gain bandwidth at higher frequency inputs, but has very good performance for lower frequencies. The output for frequency range up to 9 MHz was shown to be 3 times larger than the input.

A single low voltage marked as $\pm$12 in schematics supplies all amplifiers (X units) and line receivers. These voltages can be as low as $\pm$8V without any degradation of the performance.

- EL2044C: This chip is an operational amplifier. A general purpose integrated circuit used as a basic building block for implementation of linear functions. The op-amp's gain and response characteristics are determined by external components. It captures weak signals received from the hybrid and amplify them.

6.5.1 Line drivers

The reason to use line divers is to transfer the signals over relatively long distances. There will be some dissipation of signal energy by cables due to the capacitive coupling. At high frequencies we deal with problems caused by line reflections. Here the line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false signal. The solution is to employ transmission-line practice and properly terminate each signal line with its characteristic impedance at it's end.
Therefore it is of great importance to have some kind of op-amps which are capable to transfer signals over long distances. The amplifier choosen is OPA633. This op-amp was choosen due to its low price and good performance.

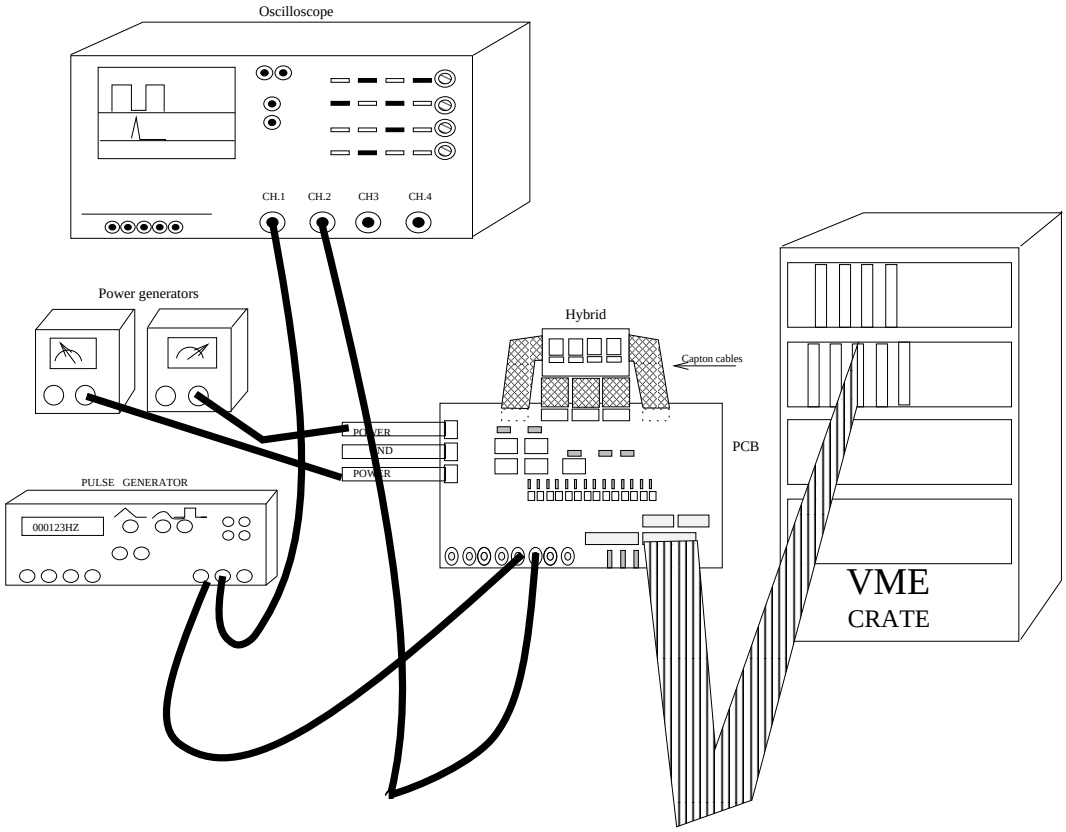


Figure 6.6: The setup used in the lab. tests.

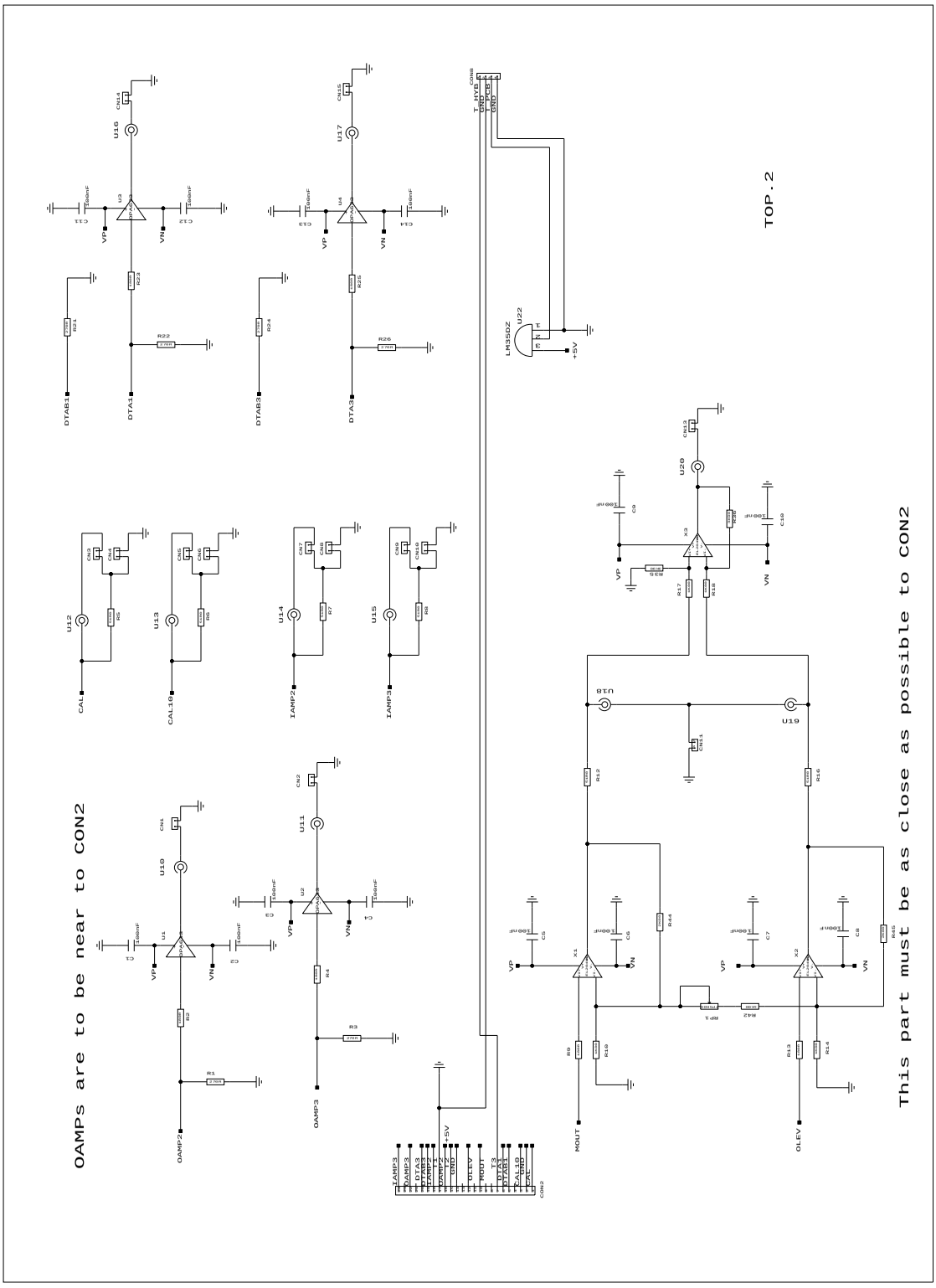
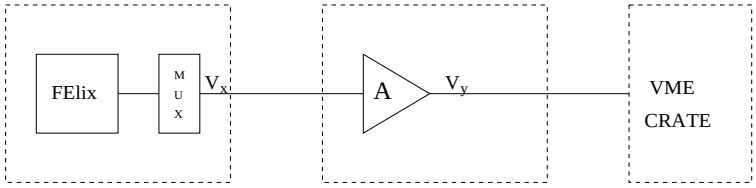


Figure 6.7: The schematic view of the buffers and differential amplifying stage.



1

Figure 6.8: The required amplification is defined by the VME-ADC operation levels and the delivered voltage from the AMUX.

6.5.2 Temperature sensor

We have used a LM35DZ as sensor. It is shown in fig. 6.7 as U_{22}. This IC is a three pin device with pin configuration as ground (pin1), power (pin3) and temperature (pin2).

6.5.3 Amplifiers

Fig. 6.7 shows the configuration which we used to get the desired gain. The required amplification factor is decided by the levels at the VME-ADC input and the voltage out from AMUX. The total amplification in differential mode is 20 and in single mode it is 3. The guidelines in choosing these gains has been the minimum voltage received at the amplifiers input[6] and operating levels of the VME-ADC[7]. For a MIP the input to the amplifiers is about 70 mV. The VME-ADC operate voltage levels are in the range between -0.6 V to +0.6 V. We predicted that a max. gain at 20 (in differential mode) and 3 (in single mode) will satisfy these requirements. Fig 6.9 shows the op-amp configuration in the single mode.

6.6 Power system

We have supplied our board with low voltages for biasing of ICs and providing necessary voltages and currents for ASICs (FElix and AMUX). There are an additional power to supply the detectors, these are high voltages. It is important to mention that the final version of the chip will provide and take care of all necessary biasings. Sofar this option is not available.
The power system applied on the PCB fall mainly into two categories. The first one are analog and digital powers which are used to feed all active elements on the PCB and hybrid and to generate internal biases of the FElix and AMUXes as shown in the schematics 6.13 and 6.14. The next power type is the biasing of Si-sensors. In chapter 6.6.2 we have more to say about them.
In the following some more description about them will be given.

[6]This corresponds to the the OLEV and MOUT outputs from the AMUX.
[7]It is an analog to digital converter.

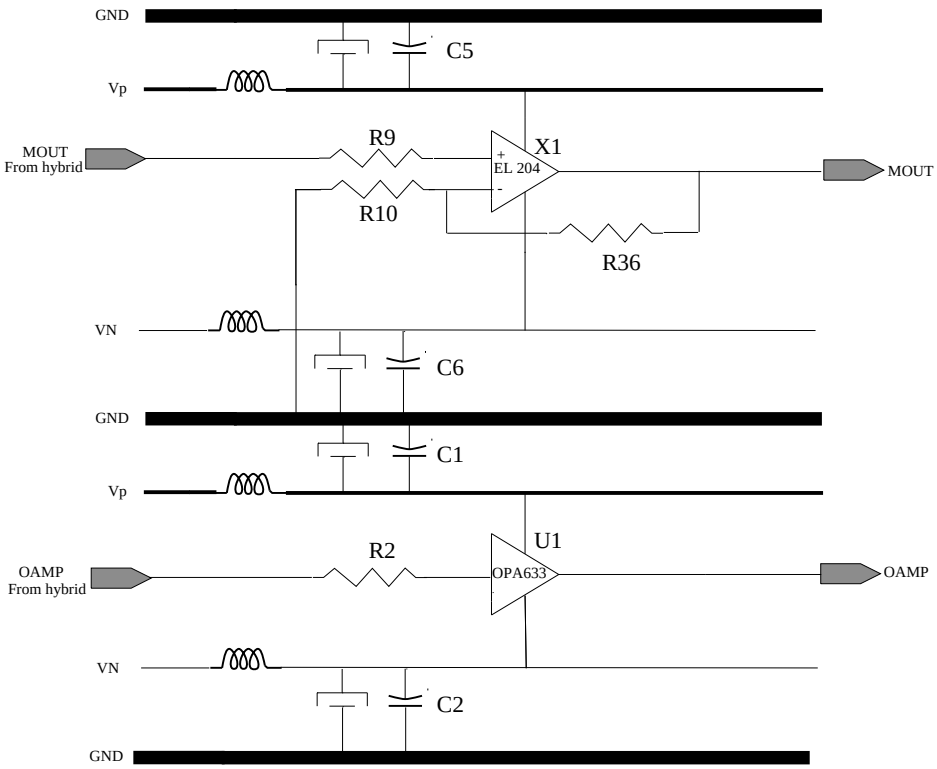


Figure 6.9: Amplifiers in single mode and buffer.

6.6.1 The analog and digital powers

All power configurations are shown in fig. 6.10. In fact there are only five different voltages arriving the PCB through connectors CN_{27} and CON_{11}. The most important design role taken into account in this design has been filtering of the input voltages. The filtering has been done by means of inductors in series and capacitors in parallel. In this way we can the suppress undesired signals which could have been carried in by the initial powers.
Our attempt to provide biases has been achieved by using traditional components such as a resistor network mounted on the PCB. The PCB for $\pm$12 V and -5.2 V. The powers labeled as $\pm$12 and VEE on schematics are used to supply the ICs on the PCB. In fact were able to run the circuits by a voltage $\pm$12 down to $\pm$8 V on lab. tests. The FElix is fed with the biases given in table 4.2. On the PCB both digital and analog powers are taken from a single $\pm$2

Signal name	Name before decoupling	Description	Nominal value
AVDD	V+2	Analogue positive supply	+2.0V
AVSS	V-2.7	Analogue negative supply	-2.7V
AGND		Analogue ground	0V
DVDD	V+2	Digital positive supply	+2
DVSS	V-2.7	Digital negative supply	-2.7V
GND		Digital ground	0V
VP	V+12	Positive supply	+12V
VN	V-12	Negative supply	-12V
VEE	V-5.2	Negative supply	-5.2V

Table 6.3: Powers available on the PCB.

power supply, and distributed later to their respective targets. Table 6.3 gives the analog and digital powers for the FElix and AMUXes. The information collected in the following tables give us overview about signals available on the board. In the following tables we use the convention that negative bias currents are drawn out of the front end chip. The nominal voltage levels used are given in table 6.3.

6.6.2 Si-detector biasing

The board is equipped with a design to bias the Si-detectors. These kind of detectors draw little current and the voltages can be set up to 300 V for heavily irradiated detectors.
The detectors have three electrical connections. In the schematics drawn by view-logic these are denoted as $GUARD_{\mathbf{1\&2}}$, $STRIPS_{\mathbf{1\&2}}$ and $BP\_CAL_{\mathbf{1\&2}}$ [8]. There is other signals for the detectors, $EXT_{\mathbf{1\&2}}$ placed on the PCB. There was no need for $EXT_{\mathbf{1\&2}}$ biases for detectors used in the test beam.
The backplane voltage supply is designed to be variable with a maximum of 300V for irradiated detectors[9]. The STRIPS and GUARD connections are at 0 V (analog ground) so that

[8]The notation $BP\_CAL_{\mathbf{1\&2}}$ stands for backplane calibration.
[9]The unirradiated detectors at test beam require the depletion voltage down to 40 V.

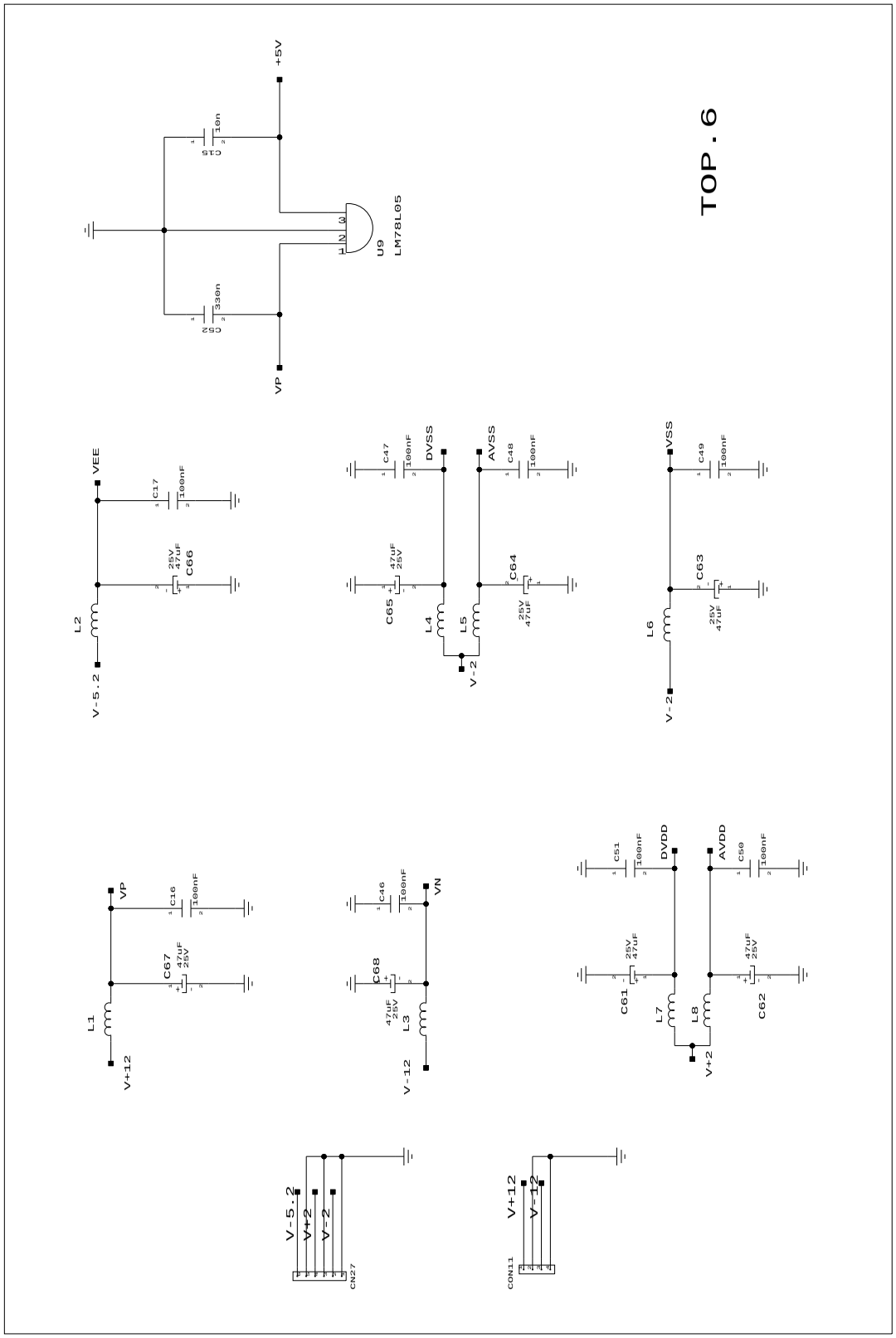


Figure 6.10: A schematic view of different power decoupling and LM78L05 voltage regulator.

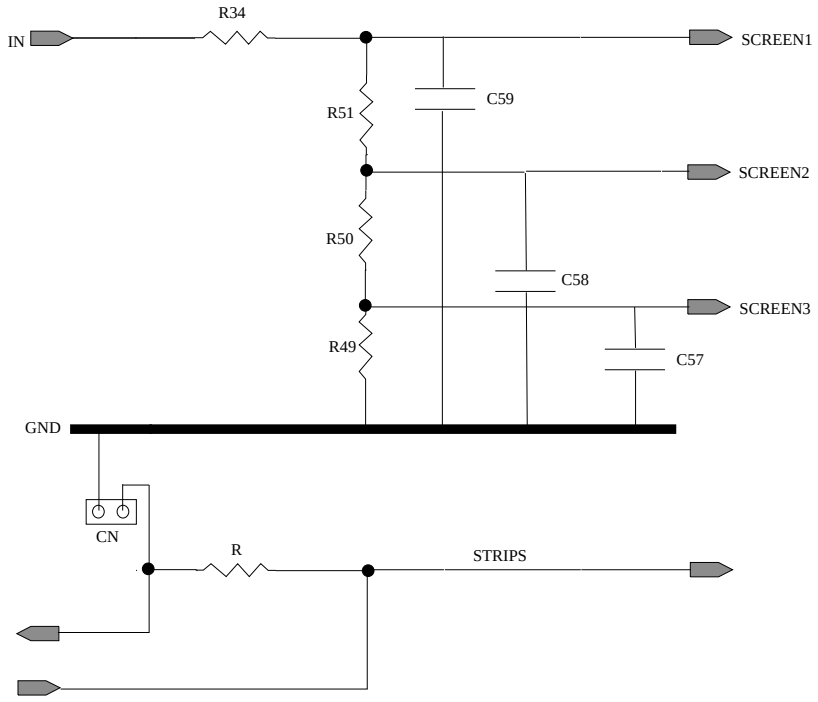


Figure 6.11: Si-detector biasing.

there is no voltage across the strip coupling capacitors. The reason to have these biases on 0V is that the amplifier inputs (in to preamplifier on the FE-chip) should be at ground level. The links are made to ground the bias BP_CAL, STRIPS, GAURD and EXT directly to the PCB's ground level or this grounding is related to the outside of the board. This is done by using jumpers. The BP_CAL is high voltage, even if we use unirradiated detector.
The thin tracks on the hybrid and kapton cables are not capable of tolerating high voltage differences to their neighbours. Thus we have to drop down this variation in a step by step manner. For BP_CAL we have adopted screening of the main high voltage track by three screens on both sides. The screens have been made by a voltage divider, in which the main voltage (the BP_CAL voltage) is broken in 1/3 units and lay on both sides. Fig. 6.11 gives a view of the coupling design.

In the figure we have drawn only the biasing for STRIPS. The GUARD and EXT follow exactly the same design as the STRIPS shown in the figure. The GND-HV is terminated by 10R resistors to limit the current so that no damage can be done to thin tracks on the hybrid and kapton cables.

6.6.3 FElix and AMUX biasing

At the design phase we were not quit sure about the exact current and voltages applied to FElix and AMUXes. The problem could be solved by making use of potentiometers to

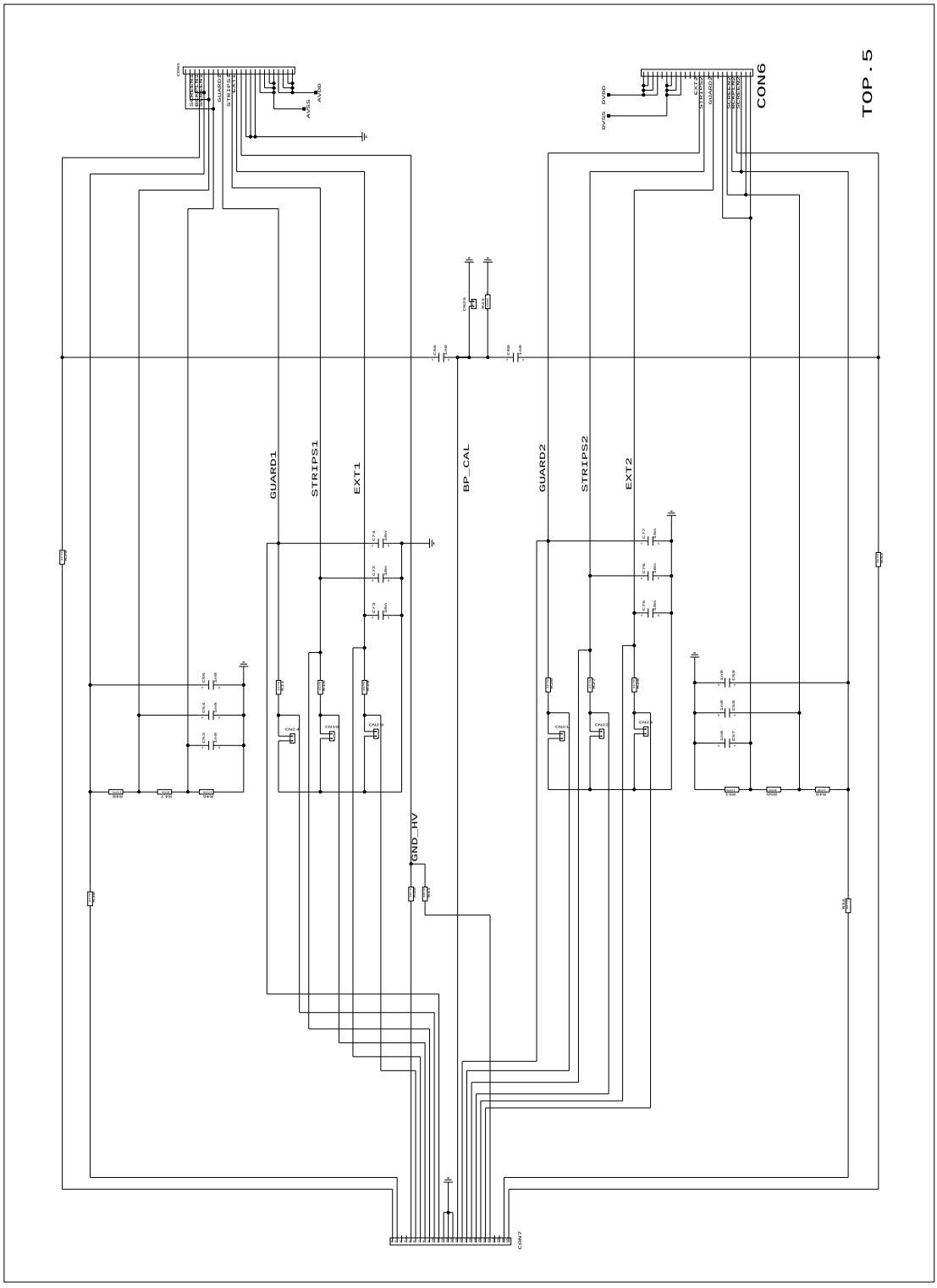


Figure 6.12: A schematic view of Si-detector biasing.

provide the required current or voltage. The design for this approach is given in fig. 6.13 and 6.14. By putting the ends of the potentiometers at ADSS and AVDD, and tuning the variable resistor inside the potentiometer, we are able to deliver voltages in the range -2 V to +2 V.
The currents all flow into the FElix and AMUXes, and they are generated by connecting a +2 V pad to a potentiometer, in series with a 1 K resistor[10]. By altering the resistance (adjusting the potentiometer) we can control the amount of current flowing into the chips.

VFS: It is a voltage across a feedback resistor in the shaper unit. In fact this resistor

Table 6.4: **FElix and MUX biasings.**

Pad name	**Nominal Value**	**Description**
SFBI1	50μA	MUX's bias of the s&h buffer
SFBI2	50μA	MUX's bias of the s&h buffer
SFBI3	50μA	MUX's bias of the s&h buffer
SFBI4	50μA	MUX's bias of the s&h buffer
APSPB1	20μA	APSP bias current
APSPB2	20μA	APSP bias current
APSPB3	20μA	APSP bias current
APSPB4	20μA	APSP bias current
BUFB12	160μA	Buffer bias current
BUFB34	1600μA	Buffer bias current
SHAB12	240μA	Shaper bias current
SHAB34	240μA	Shaper bias current
PREB12	1400μA	Preamplifier bias current
PREB34	1400μA	Preamplifier bias current

is made of a MOSFET transistor and its resulting effect is as a resistor. The two legs of the resistor are the source and drain of the MOSFET. By varying the voltage VFS on the gate terminal, one can change the resulting resistance value. This voltage is delivered by potentiometer.

VFP: It is applied internally in chip in the feedback on the preamplifier. It is made in the same way as the VFS.

[10]The purpose of such a resistor is only the ease of measuring currents or voltages.

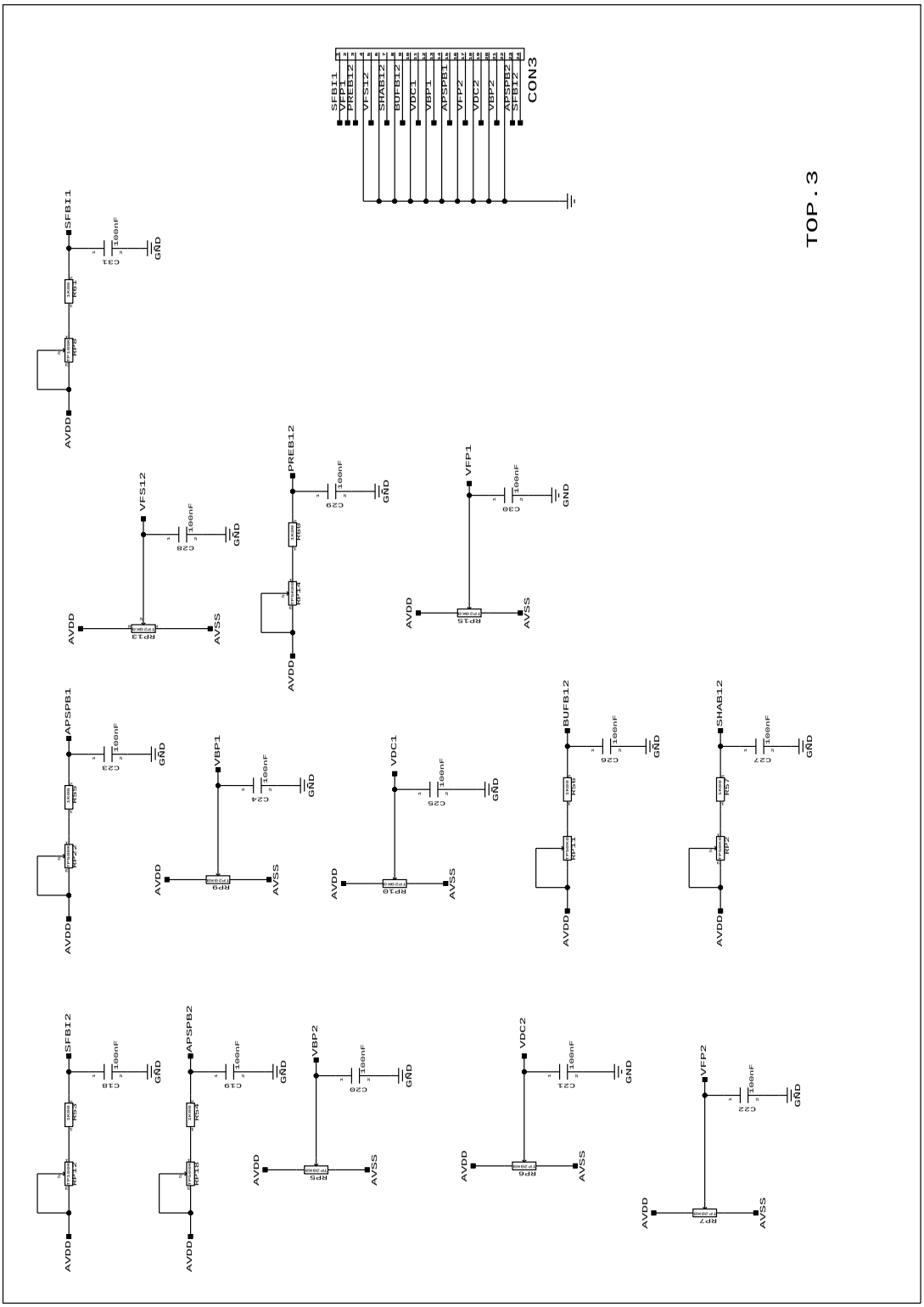


Figure 6.13: A schematic view of generation of biases applied on CON3.

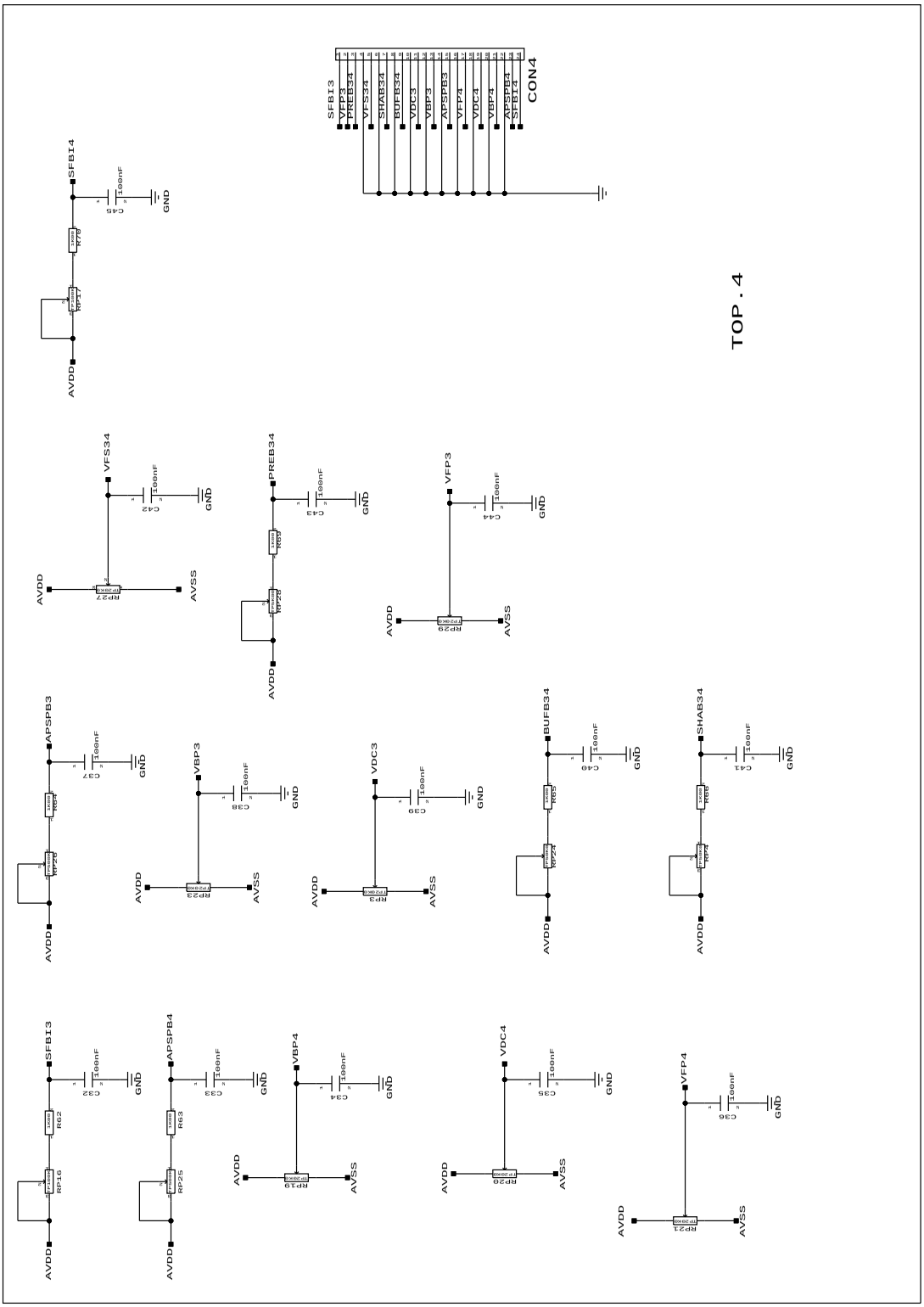


Figure 6.14: A schematic view of generation of biases applied on CON4.

Table 6.5: **Voltages to the FElix.**

Pad name	**Value**	**Description**
VFP1	-0.4V	pre. amp. feedback res.
VFP2	-0.4V	pre. amp. feedback res.
VFS12	0.6V	shaper feedback res.
VFS34	0.6V	shaper feedback res.
VDC1	-0.9V	backplane storage cap.
VDC2	-0.9V	backplane storage cap.
VDC3	-0.9V	backplane storage cap.
VDC4	-0.9V	backplane storage cap.
VBP1	-1.1V	backplane APSP cap.
VBP2	-1.1V	backplane APSP cap.
VBP3	-1.1V	backplane APSP cap.
VBP4	-1.1V	backplane APSP cap.

Chapter 7

Simulations

7.1 Introduction

A simulation tool is a very powerful help in design. It's role is as a guide in making the right decisions in the design process. We simulated the buffers by using **PSpice** simulation software. To achieve meaningful results we needed to use the accurate models for the components involved. These models enable us to predict accurate AC and transient behavior as well as DC performance of the circuits. Models alone do not guarantee accurate behavior of the circuits. The main interests in our simulations were to verify the functionality of buffers and amplifiers.
The results from the simulation needed to be checked in the laboratory. Later we did some measurements on the finished board. These tests verified the correctness of the simulations and are described in section 9. A few small deviations from the predicted results were however observed.

7.2 The OPA633 line-driver

The buffers used are OPA633 from Burr-Brown. At the simulation time we could not find the original model for OPA633. Therefore we had to use another model instead of OPA633. The search for a model for this buffer lead to a similar model made by the company "Analog Device". This model originally was written for a device called AD9630. But according to Analog Device the models could be used for OPA633. The schematic view of the circuit drawn by Viewdraw is given in 6.7. To simulate a circuit by PSpice we can equip the device combined with its external components with a configuration as shown in fig.[1] 7.1.
The schematic used for simulation of OPA633 is given in fig. 7.1. The simulation result of AC-analysis is given in fig. 7.2. It shows that for frequencies up to 40 MHz we have good performance.

[1] In fact it is not necessary to make such a schematic. We could write a source file to do the same task.

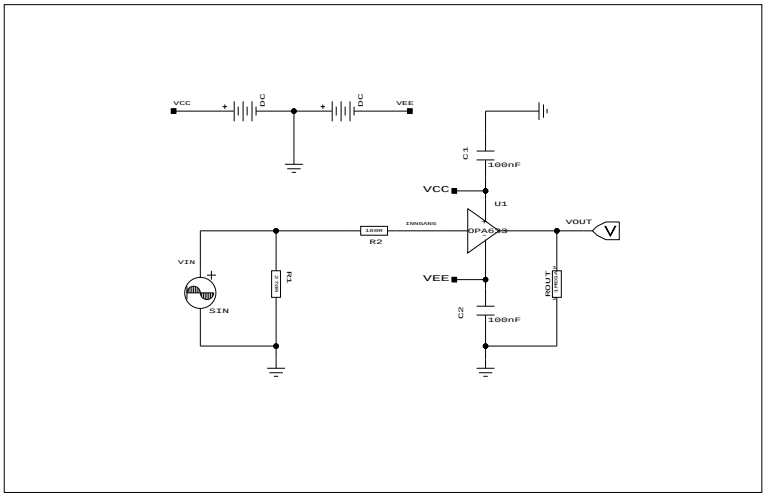


Figure 7.1: The schematic view of OPA633 used for simulation with it's external circuitry.

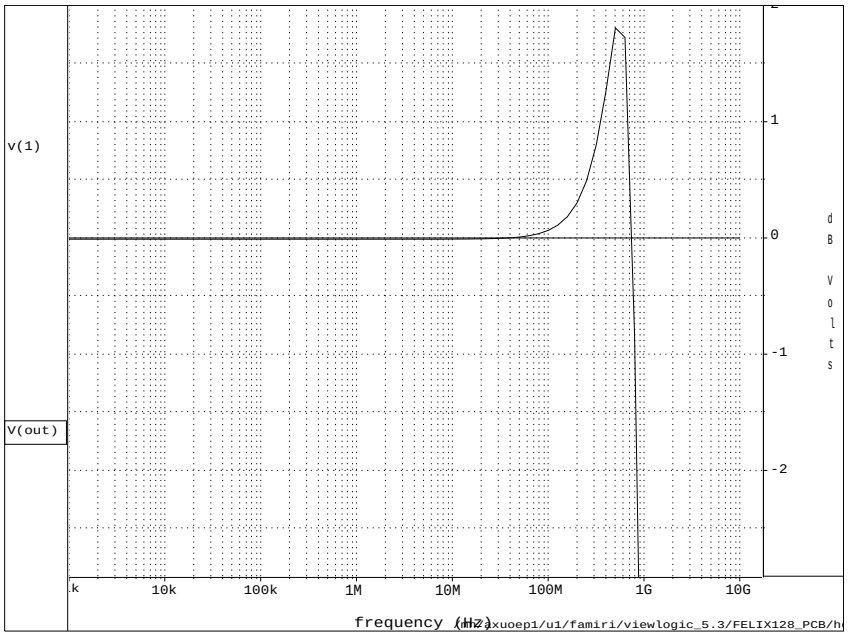


Figure 7.2: The AC response of the buffers OPA633.

7.3 The EL2044C

The EL2044C was simulated too, according to our design calculation we had 3 as the gain out from each none-inverting stage. The schematic view of the amplification stages used for simulation is shown in fig. 7.3.

The result of AC-analysis simulation is given in fig. 7.4. It shows that f_{3db} is about 20 MHz and has 6.5 dB as the gain at this frequency. The transient response is shown in fig. 7.5. The out at this frequency (100 KHZ) has the desired amplification.

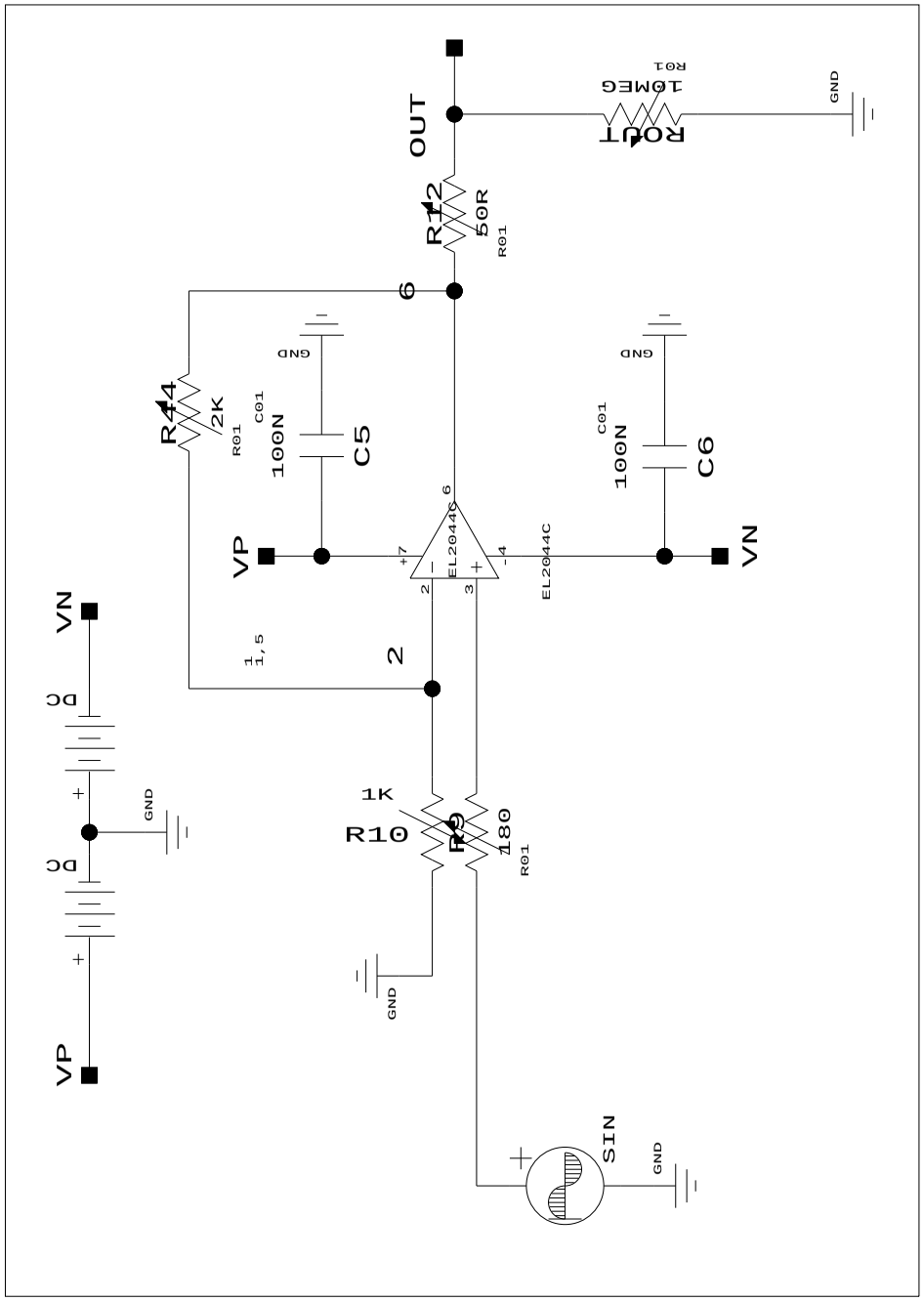


Figure 7.3: A schematic of amplifier in single mode using EL2044Cs.

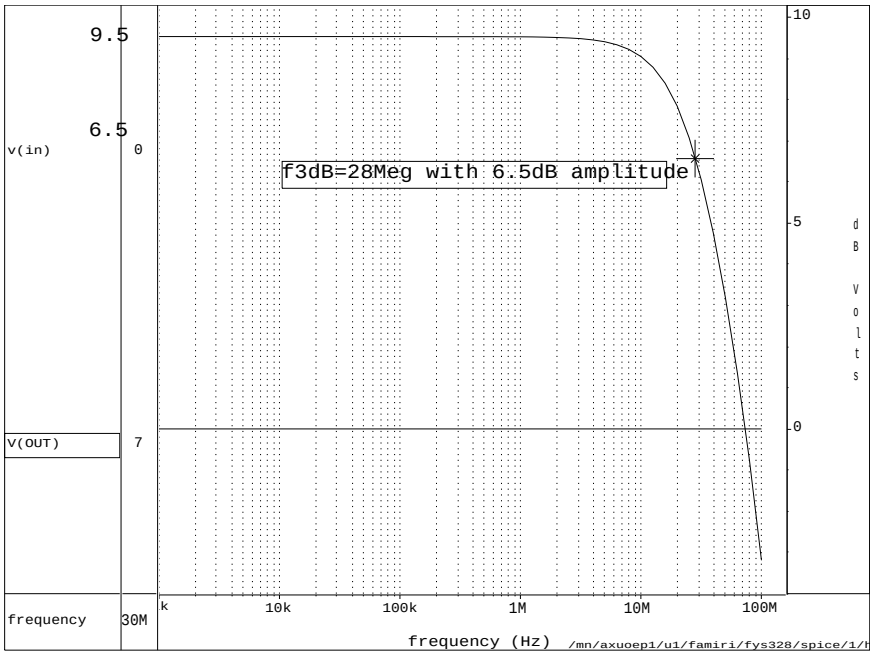


Figure 7.4: The EL2044C's AC response.

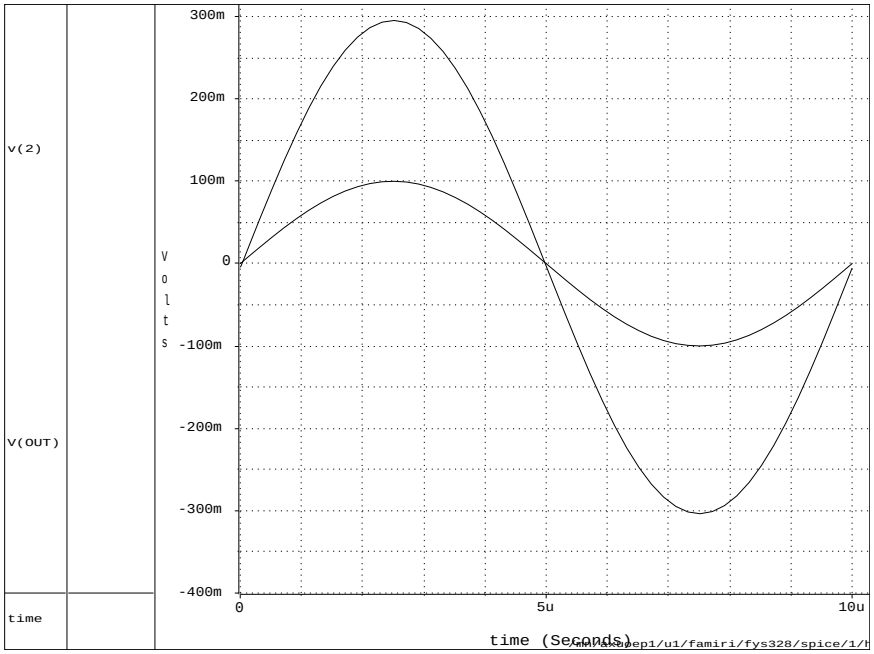


Figure 7.5: The EL2044C's transient plot as a function of Vin=100mV

Chapter 8

The PCB layout

8.1 General introduction

We made the circuit diagram and were confident that the design would work. We began the next phase, namely the layout. A combination of components and devices together will give us the desired functionality[1]. The board holds some IC units, passive components and odd[2] components.
The output from the schematic captures described in chapter 6 consists of a set of drawings and a netlist. Netlist is a list of every signal, telling about node (component pin) that it is connected to. The netlist output from schematic capture phase contains all that is necessary to construct the circuit. To make the layout from the schematic design we had to give the components some information about their pin number, actual physical size, footprints and so on. The layout of the design was made by a tool called CAD STAR tool using these informations. The board is made as a two layer PCB. The PCB layout and footprints of components used on it is shown in fig. 8.1. The layout of power, ground and signal routing are given in fig. 8.2 and 8.3.

8.2 Design consideration

The board had to satisfy specifications regarding electrical performance and reliability. The desired performance of the PCB is set by the operating parameters of the ATLAS SCT inner detector and it's prototype readout chip FElix i.e. the signals type and amplitude. It is essential to design the system for low electro-magnetic emission. The efforts done in reducing these unwanted effects are:

- Using thick ground paths.
- Using decoupling capacitors, especially at those points where power was delivered to IC devices.

[1]The Printed Circuit Board (PCB) is a technic for making boards. We have adopted this generic name for our board.

[2]These are components such as connectors in which do not fall into either passive or active ones

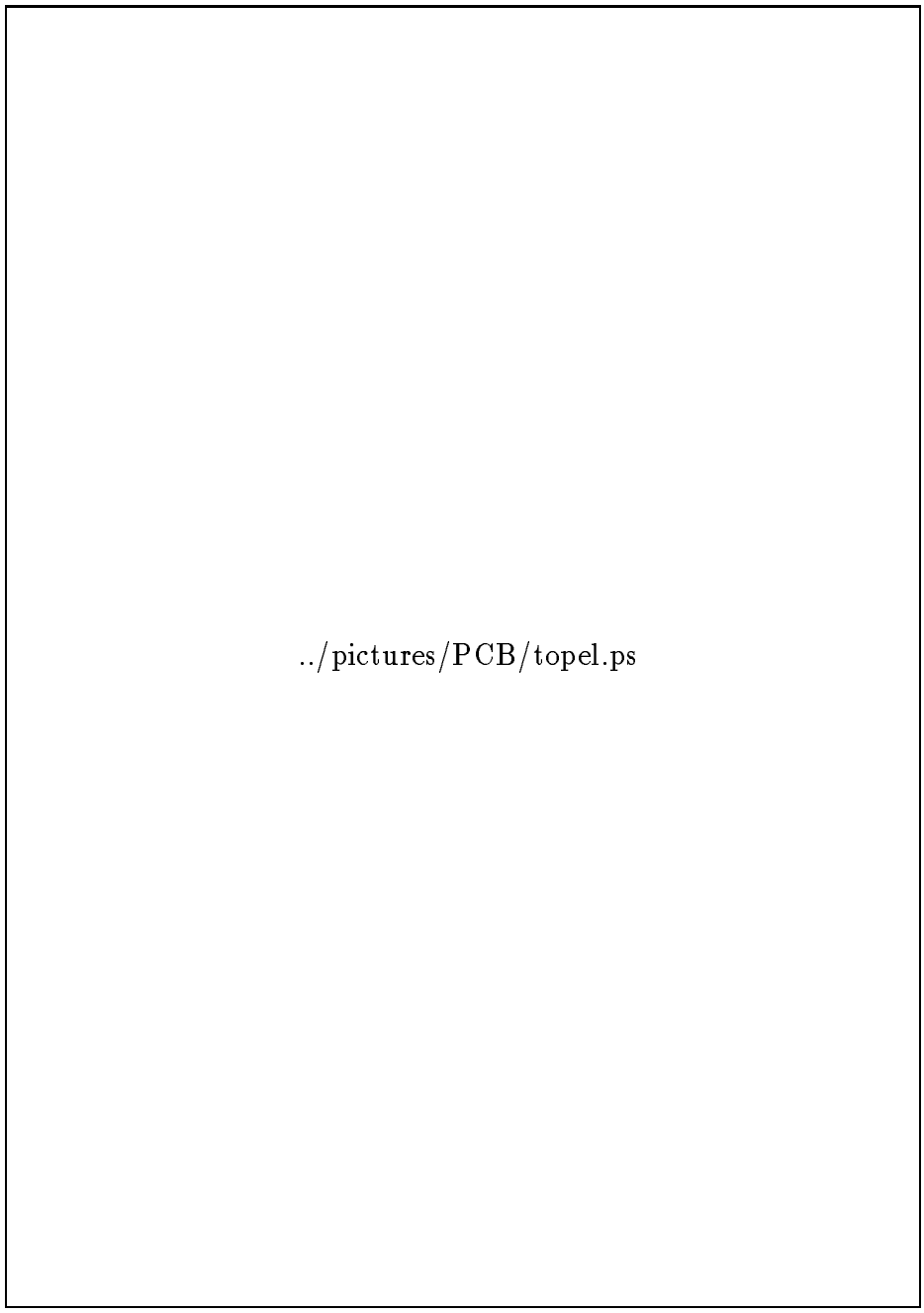


Figure 8.1: The top view with component placement.

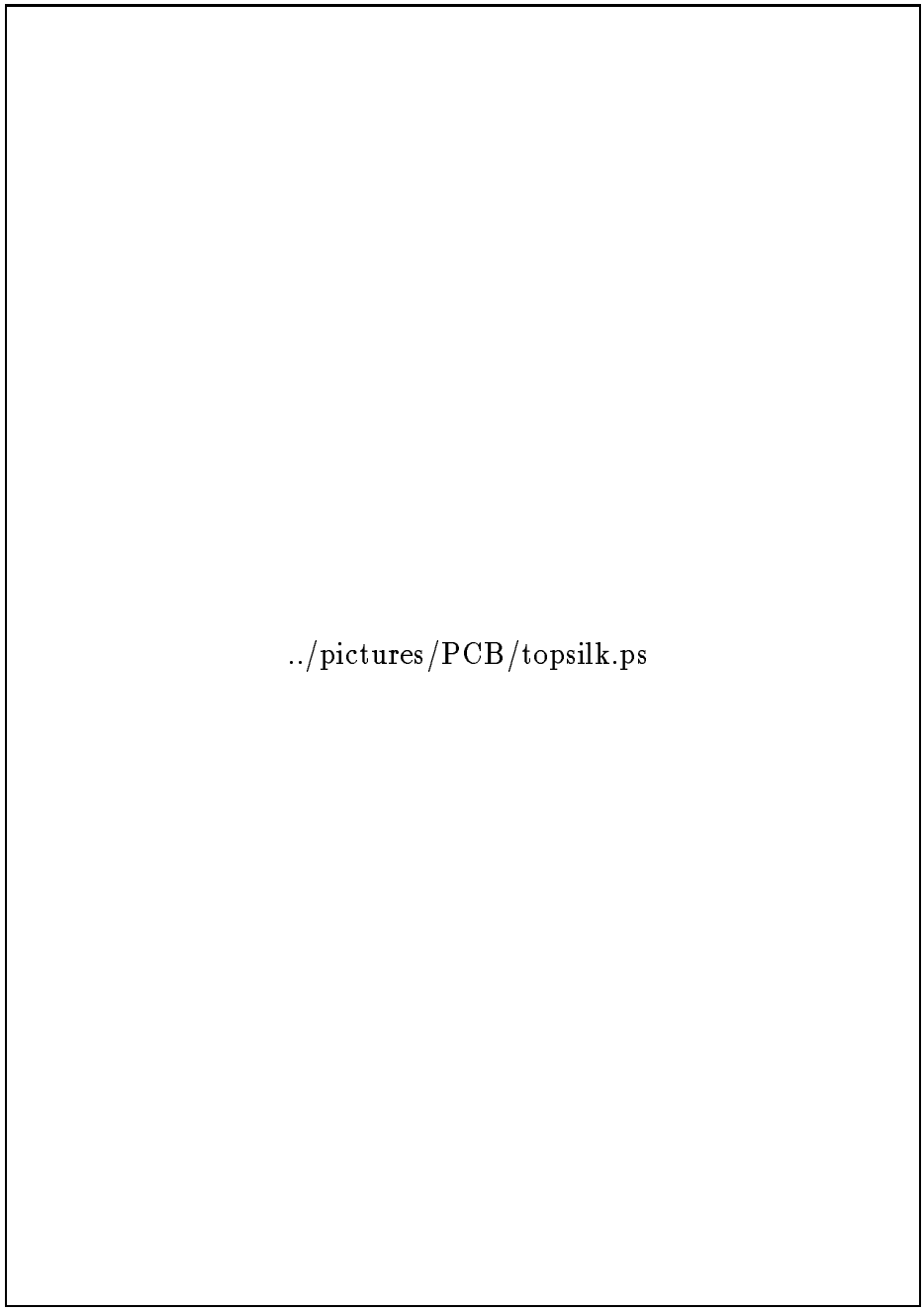


Figure 8.2: The routing pattern on top plane.

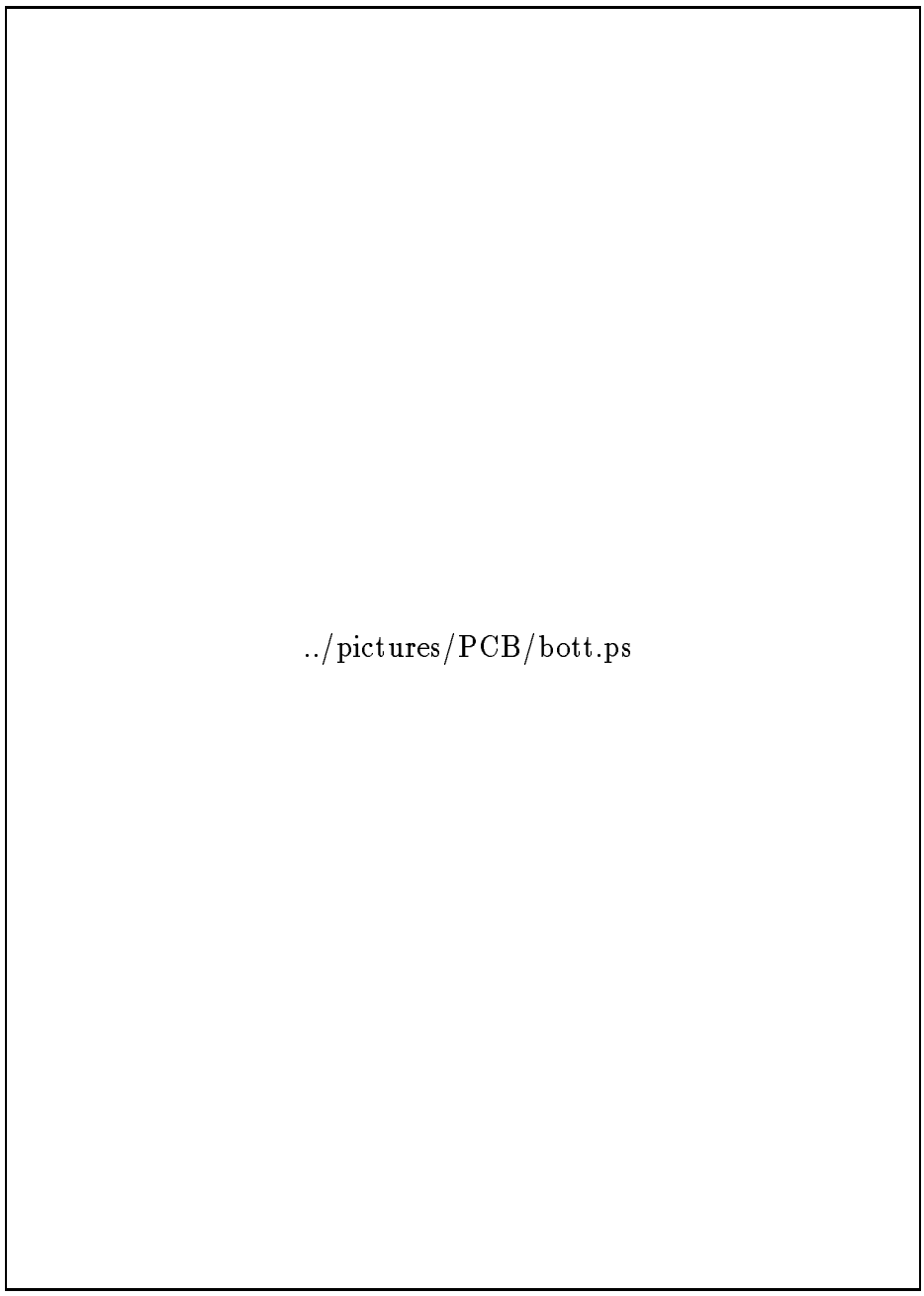


Figure 8.3: The bottom plane plus 2 connectors.

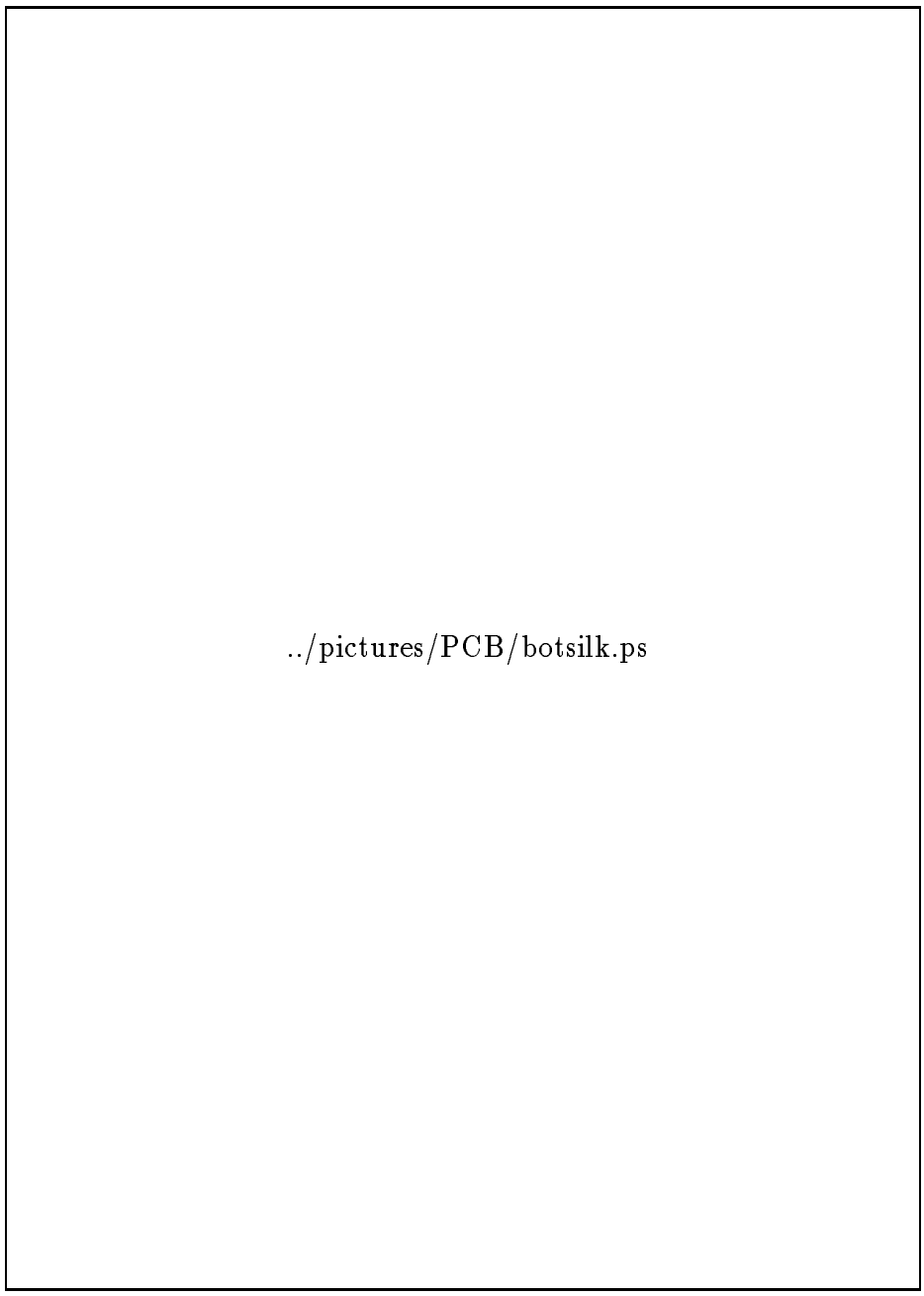


Figure 8.4: The routing on the bottom plane.

- Due to electromagnetic effects in picking noise from neighbouring signal paths we have tried to make the signal paths on the PCB as short as possible.

There are a lot of components which were going to be mounted on the PCB, and it was important to have the best possible grounding. The grounding is a compromise between good performance and available place[3].
The importance of decoupling capacitors is to provide the required current to the ICs. The PCB power distribution must provide sufficient current, in time, for the circuitry inside the device to operate. The power distribution system must provide this current without lowering the input supply voltage below its minimum acceptable threshold. Discrete capacitors are placed near the devices, connected between power and ground tracks, (fig. 6.9 on page 61) to provide this current. These capacitors provide the charge current to the device instead of the power tracks. When they discharge their current into the device they quickly recharge from power supplies prior to the next required discharging. The frequency response required by the decoupling capacitor are much higher than the clock frequency.

8.3 Components

There are a large number of passive components used on the board. These are summarized in table 8.1 and 8.2. Table 8.3 lists two kind of network resistors which are used as termination resistors. They are made in a tihck film technology. The type SIL[4] provides 8 resistors and is a 9 pin device. The 9th pin is a common input and is connected to VSS. The last resistive network is also used as termination resistor, but in despite of SIL it is a DIL[5] type with 16 pins and provides 8 resistors each of 100 Ω. In the following the components used will be explained in more detail.

- Amplifiers/Buffers: The EL2044Cs are used as amplifiers. They are used to amplify the AMUX analog signal outputs (MOUT and OLEV).

- Digital devices: C10H115P is used as receiver and MC10H101P as driver for ECL digital control signals send from the SEQSI sequencer.

- Temperatue sensor: It is important to have the temperature as low as possible on the board. By using the LM35DZ temperature sensor we are able to measure the temperature on the PCB at any time. This sensor operates with a +5V supply.

- Voltage regulator: The LM78L05 operates with +12V power supply and deliver 5V. By using this voltage regulator we are able to deliver the senor its required operating voltage.

- Connectors: We have used a variety of connectors. An overview of these connectors is given in table 8.4. Six 24 pin flat cable DuPont connectors are used to connect the

[3] We have relatively a large number of components placed on the board.
[4] Single In Line.
[5] Dual In Line package.

PCB to the hybrid. The lemo connectors are used to send in/out the signals to/from PCB. The signals carried on these connectors are f.ex. analog signals out from AMUX (MOUT and OLEV), calibration signals (CAL and CAL10), input to broken channel (IAMP) and the output from them (OAMP), and the differential signal after analog amplification.

The connectors used are for :

1. The input digital control signals through CON26.
2. Supply voltages and ground by connectors CON11, CON12 and CN27.
3. To transfer the temperature sensor signal through CON8.
4. To connect the PCB to hybrid (CON1 ->CON4) via kapton cables.
5. To supply the Si-detectors with high voltage through CON1 and CON6. The connector (CON7) receives these high voltages and their screening.

The buffers and amplifiers use 8-pin Dual In Line (DIP) packaging allowing easy stacking on the board. The chips on the PCB are stacked with a pitch of 100 mill[6].

8.4 PCB production

By the end of July the design phase was finished. The next step was to transfer the design to a CAD system which is able to produce the routing's pattern and vias. The basic idea behind the system is to figure out how to make all the interconnections the circuitry demands by running lines on the board. Transferring schematic design to a CAD tool called CAD-STAR, for preparing the layout, was done by Ole Dorholt at the electronics lab. The mentioned CAD-system converts the schematic designs to layout in which the copper-foil traces and component placement will be generated. The board is made on 140 $\times$ 280 mm glass epoxy. During a stay at CERN we did some tests with PCB and found a grounding problem on the board. Some improvements seemed to be necessary. In the autumn we made another PCB. This new one had better component insertion possibilities and grounding design. Better component insertion was made by using sockets for all buffers and EL2044 amplifiers. The board is made at the Electronic Lab at Physics Department. The board material is made of a so called FR-4 which is a fire-resrsist epoxy-bounded fiberglass. The board is clad on both sides with copper [26].
Fig. 8.5 shows the different layers on a FR-4 board. FR-4 is composed of glass/epoxy as its substrate material. It is made of several layers of woven fiberglass sheets in a matrix of epoxy. The substrate conductor (Cu) are on both sides. The next step was to print both sides of the patterns made by the CAD tool. The layout was sent to a plotter. The plotter used must have very good resolution i.e. the amount of points pr. cm^2 must be high enough to give a good picture of the pattern.

[6] 1 mill=25 μm.

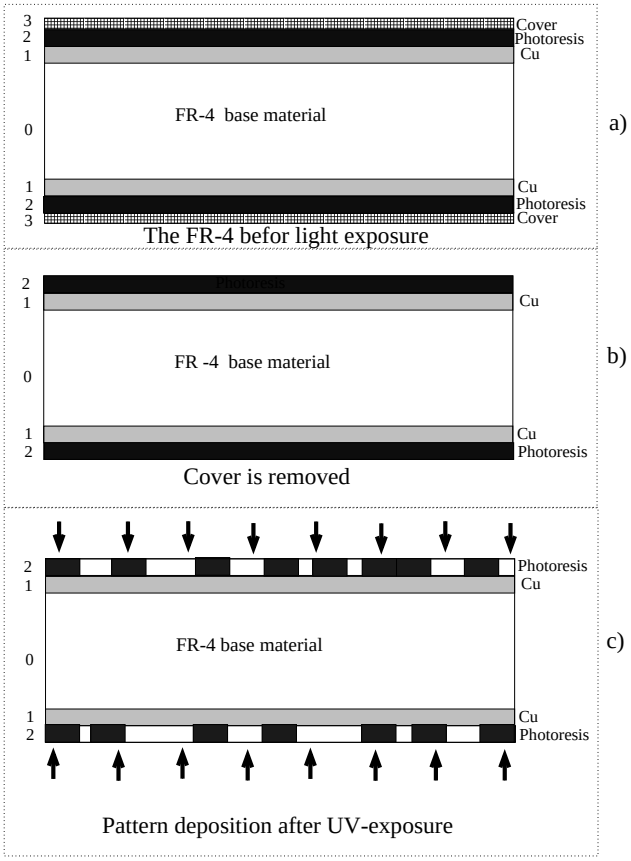


Figure 8.5: Steps in deposition of circuit pattern onto FR4.

Latter we made films from those prints, simply by copying the prints to transparent papers. Next phase is to process the naked board. The board was sprayed with a photo sensitive material. Then films were put on the board which was already cut in desired size. In this stage we were very careful in having the films exactly at the right place on the board.

The board covered with films was put in an UV instrument. The purpose was to wash away the undesired copper area by an etching process latter. The UV rays will expose the naked board which is covered by the photo-sensitive material. Those areas which are covered by film's pattern (in our case the black area on the film) will be unexposed for UV. By this method we get a positive pattern on the board. The process continued by washing the board with a solvent. This solvent etched the UV exposed areas on the board. By further washing we were left with a board with all electrically conducting paths. It remained to protect the finished board against moisture and dust with a conformal coating.

The board was now ready for drilling and component placement. We drilled all component holes and vias. The PCB is made mainly in hole mounting technic. The components are mounted by insertion through holes. The pins are soldered to the substrate on the backside. These solder joints make up both electrical contact and mechanical support.

The interconnection between sides is done by inserting a metalic stave through vias and then

soldering on both sides. The components are interconnected on the substrate by conductor patterns of copper which are made by the etching method and are on both sides. These tracks are the physical media for transmission.
The components are discrete devices R, L, C, connectors and ICs. The surface mount devices [connectors CON_1 to CON_6] were first placed on their respective solder pads with a little solder paste. The board was put into an oven. Heat causes the paste to become a solid metallic solder alloy. The next component type were hole mounted. We placed our components one after one and soldered the pins.
The board is double-sided. It means that electrical traces are on both sides. The vias (holes) are lined with metal, connecting corresponding pads on both sides . The connection between sides is achieved by means of vias. All component vias are 0.7 mm drilled. The connectors are drilled by 1.3 mm due to their pin size.
After mounting the components, the next phase was to test the board. Testing of the first prototype for shorts were done at Oslo and at CERN in the middle of August. A list of checks that we did and the results of checks are given in table 8.5. The physical tests were done by a multi-meter.

The results of these tests were good. All the signal paths seemed to be correct.

REFDES	Quantity	Device	Package	Value
C_1 -> C_{51}	50	100NF/XXV	CAP	100 nF
C_{15}, C_{69},C_{70},C_{71}	4	10NF/XXV	CAP	10 nF
C_{52}	1		CAP	330 nF
C_{53} -> C_{60}	8	1NF/500V	CAP	330 nF
C_{61} -> C_{68}	8	47UF/25V	ELYT	47 μF
C_{72} -> C_{77}	6	10NF/500V	CAP	10 nF
CN_1 -> CN_{11} CN_{13} -> CN_{15} CN_{18} -> CN_{25}	22	CONN/2PIN	MOL2	
CN_{16},CN_{17}	2	CONN/3PIN	MOL3	
CN_{26}	1	CONN/34PIN	T&B	
CN_{27}	1	CONN/6PIN	MOL3	
CON_1 -> CON_6	6	CONN/24PIN	DEPONT24	
CON_7	1	CONN/26PIN	T&B	
CON_8 -> CON_9	2	CONN/4PIN	MOL4	
L_1 -> L_8	8	RF-3B1	94Z	2.4 μH
R_{40},R_{41}	2	10R-1%	RES	10R
R_5,R_6,R_7,R_8 R_{12},R_{16}, R_{31}	7	51R0-1%	RES	51R
R_2,R_4,R_9,R_{13} R_{23},R_{25}	6	180R-1%	RES	180R
R_{21},R_{22},R_{24},R_{26}	4	2700R-1%	RES	270R
R_{10},R_{14}, R_{17}, R_{18} R_{32},R_{42}, R_{43}, R_{50} R_{51},R_{53}, R_{54}, R_{55} R_{56},R_{57}, R_{60}, R_{61} R_{62},R_{64}, R_{66}, R_{69} R_{70}	21	1K0-1%-0.2	RES	1 KΩ
R_{35},R_{36}	2	3K9-1%-0.2	RES	3.9 KΩ
R_{11},R_{15},R_{19},R_{20} R_{27},R_{28},R_{30}	7	4K7-1%-0.2	RES	4.7 KΩ
R_1,R_3,R_{46},R_{47} R_{48} -> R_{51}	8	100K/XXW	RES	100 KΩ

Table 8.1: Components used on the PCB.

REFDES	Quantity	Device	Package	Value
RP_1,RP_{14},RP_{28}	3	TRPOT		5 K
RP_3,RP_5,RP_6,RP_7 RP_9,RP_{10},RP_{13},RP_{15} RP_{19},RP_{20},RP_{21},RP_{23} RP_{27},RP_{29}	14	TRPOT		20 K
RP_4,RP_{11},RP_{24}	3	TRPOT		50 K
RP_2,RP_8,RP_{12},RP_{16} RP_{17}	5	TRPOT		100 K
RP_{18},RP_{22},RP_{25},RP_{26}	4	TRPOT		500 K

Table 8.2: Potentiometers used on the PCB.

REFDES	Quantity	Device	Package	Value	Pins	Type
R_{37},R_{38},R_{39}	3	RES	L09-1	47R0-2%	9	SIL
R_{52}	1	RES	898-3	100R-2%	16	DIL

Table 8.3: Resitive networks used as termination resistors.

Connector type	Name on PCB	Availabe pin	Total
Lemo/horiz.	U_1 toU_{21}	1	12
Molex/vertical	CON_8, CON_{11}, CON_{12}	4	3
Molex/vertical	CN_{27}	6	1
DuPont	CON_1 -> CON_6	24	6
T& B vertical	CON_7	26	1
T&B vert.	CON_{26}	34	1

Table 8.4: Different connectors used on the PCB.

check item
connection of tracks from a bond pad to connectors' pads.
shorts between combinations of power/power and ground/power.
the chips pads connected to XVXX on connectors.
signal short to either power or ground.
R and C pads connected to their right signal line.
the long digital tracks were not broken.
shorts between any neighboring digital tracks.

Table 8.5: The PCB electrical check results.

Chapter 9

Measurements

Three test inputs are applied to FElix chip to faciliate testing of the complete electronics. They are called CAL, CAL10 and IAMP. The checks are made to verify that the PCB fullfils its foreseen specifications.

9.1 Running the sequencer

At the Oslo ATLAS laboratory we did some tests to verify the functionality of the PCB and hybrid. To do tests we have to send electrical signals into the FElix and AMUX. These signals are are analogue with a size comparable to a silicon strip signal.
By feeding a sequence of such a signals into the FElix and AMUXes we are able to observe the chips response to the signals on an ocsilloscope. The program which gives the desired sequence to run the FElix was made by a former student at Oslo University [21]. The program is designed to give 32 bits at each clock edge. The clock frequency is the same as the BCO rate (40 MHz). A view of timing diagram of this program is shown in fig. 9.1 and it shows the timing realation for the most important signals. The timing can be changed by altering codes in the program source file which is written in C-programming language. The graph 9.1 shows some of bits. These bit numbers are given in table with their respective

Bit number	Signal name
6	SAMPLE
8	MRESET
10	CLK
12	RBIT
14	BUSY
16	T1
18	RESETB

Table 9.1: The conversion of sequencer bit numbers.

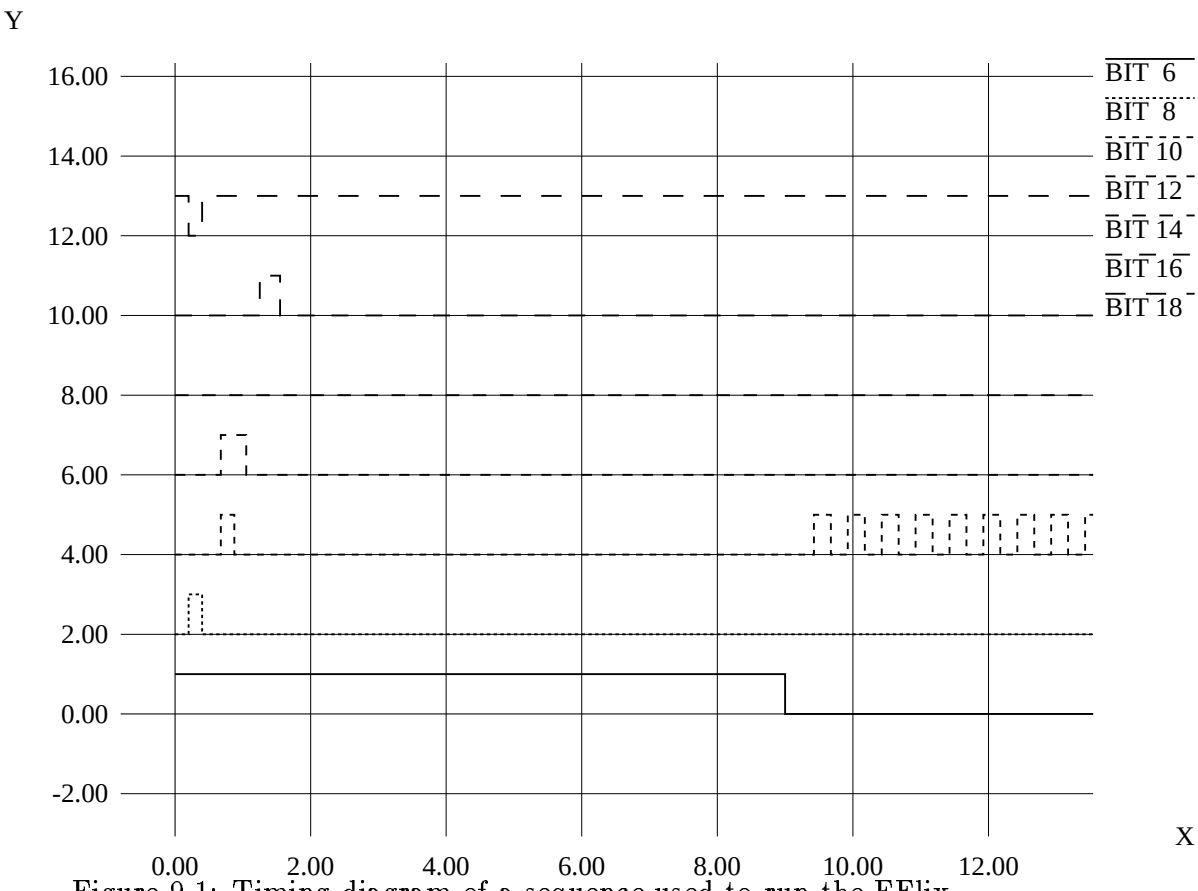


Figure 9.1: Timing diagram of a sequence used to run the FElix.

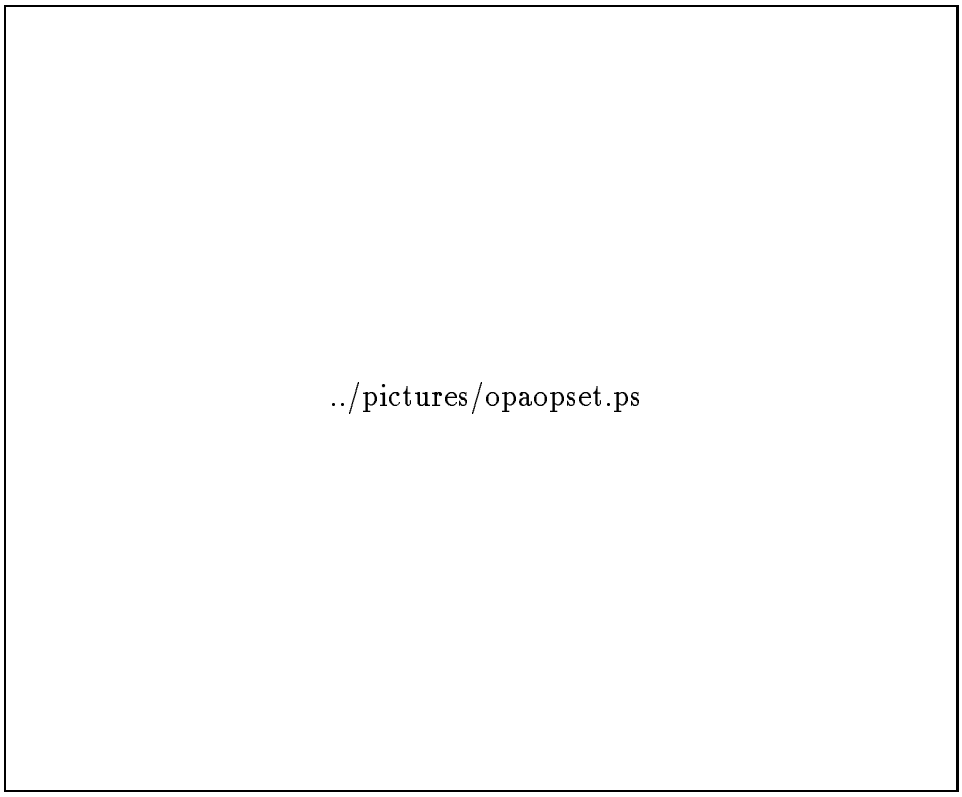


Figure 9.2: Oscilloscope view of T1, MUX clock and RBITsignals.

names according to our schematics.
The oscilloscope view of a sequence run at CERN is given in fig. 9.2 and fig. 9.3. The tests at CERN were made on FElix chip mounted on a hybrid in contact with the PCB. The program used was LabView, this program differs a little from the one used at Oslo. But the functions are the same.

As we can see the signals have passed the PCB and that the board is functioning. The signals shown at fig. 9.2 are T1, MUX clock and RBIT for the second AMUX. Those signals shown in fig. 9.3 from the top are DTA and SAMPLE. These oscilloscope views are made in the ATLAS laboratory at CERN.

9.2 Instruments used at lab

The hybrid interface board was tested with probe station for its direct performance and general functionality using a test bench setup. The used instruments at the Oslo University were:

Power supplies The operating parameters are specified with nominal values given in table 6.3. The supply voltages can be varied without seriously affecting the functionality. In fact VP and VN came down to +8 V and -8 V. For lower power supply the power

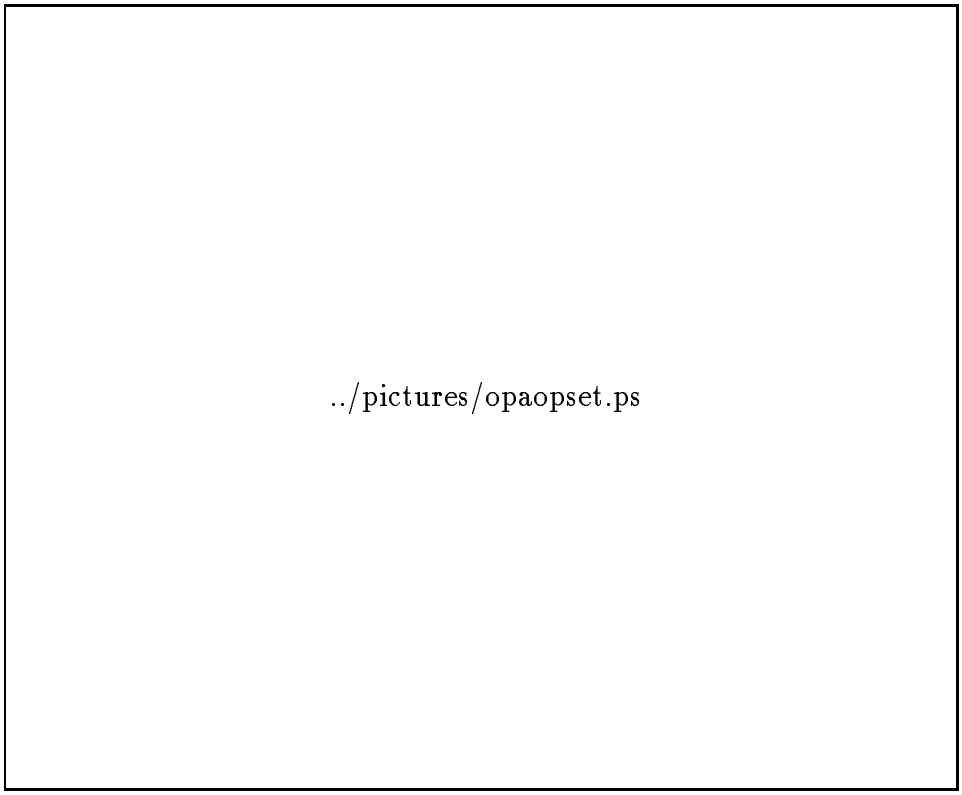


Figure 9.3: Oscilloscope view of DTA and SAMPLE signals.

dissipation will be lower. We used 4 power supplies capable of delivering voltages up to 20 V.

Oscilloscope The type used at the Oslo ATLAS lab. was a Kenwood CS-6020 digital oscilloscope and a LeCroy 9350A.

Pulse generator The pulse generator used were PHILIPS PM5786, PHILIPS PM5712 and BK PRECISIO R 3040.

9.3 Laboratory tests

Sources of both internal and external capacitance contribute to the effective total load, and we need to consider their sum. The transistors and metal interconnections generate internal parasitic-capacitance elements. These internal capacitance sources have an effect on the power dissipation similar to the external load capacitances attached to the device output pins. It is necessary to have a reasonable settling-time for the signals out from the buffers. Those two most important active devices used on PCB are those used for transmission and amplification of analog signals from the broken channel and the AMUX. These two are OPA633 and EL2044C.

OPA633: OPA633 is an op-amp which is usable as a high speed buffer amplifier. An amplifier of unity gain is called buffer because of it's isolating properties (high input impedance, low output impedance). As already mentioned the small current spike from the detector is first put through a fast charge -sensitive preamplifier. The signal then will be proccesed in the shaper to give the optimal 75 ns rise time. In order to test the FElix functionality the chip is equipped with a broken channel. The charge injection through this channel is done through the IAMP connector on the PCB. The purpose of this signal injection to the preamplifer is to find what value we will get out from the FElix preamplifier/shaper stage. This charge injected to the FElix's broken channel is equivalent to 1 MIP[1]. The preamplifier gain is 1 $\frac{mV}{fC}$. The shaper stage following the preamplifier has a substantial gain of 20 [21]. Therefore the signal out from preamplifier according to equation 9.1 will be about 71 mV.

$$OAMP = 20 \times \frac{[22400 \times 1.602 \times 10^{-19} C]mV}{10 \times^{-15} C} = 71.68 \ \ mV. \tag{9.1}$$

For testing the OPA633 a signal was generated by a signal generator. When giving an input signal and observing the output, we find that there are some ripples at the output. Some tests were made to find the time required for the output to fall to its final value, i.e the settling time. The signal which is going to be measured is the output from OAMP3 (fig. 6.9 shows its position in combination with its network arriving OPA633.) The input in the schematic is named with IAMP3, we could choose OAMP2 too.
The settling time showed to be 7 ns. The main concern of this test is to find the time constant for buffer. It is a means of a comparison between the buffer with all it's external

[1]One MIP is eqivalent to 22400 e^- in 300 μm silicone.

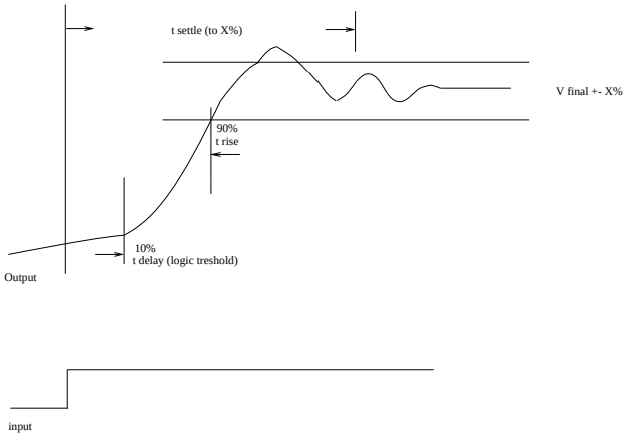


Figure 9.4: Settling time.

components and a simple low-pass RC filter. The settling time is roughly 5RC. It gives us a stop frequency at some hundred MHz. As already mentioned the FElix readout frequency is 250 KHz, therefor the FElix readout frequency will not be a problem using this chip.
Amplifiers: They also were tested with different frequencies. They showed to be functioning well according to design for frequencies up to 3 MHz.

9.4 Conclusion

We have made an interface for the ATLAS Z-module hybrid. It is a support electronics board to read out of four 128 channel FElix chips and their AMUXes placed on the hybrid. The purpose of the PCB was to generate, amplify and provide support functions for efficient testing and debugging of a first Z-module. The functionality of the interface PCB board have been proved by tests made in Oslo and at CERN. It provided all the necessary functions for the Z-module test.

Chapter 10

Glossary of acronyms

ACRONYM	EXPLANATION
ADC	Analogue to digital converter, a device for converting an ananalogue electrical signal to digital form, so it can be subseqently stored and processed on a computer.
APSP	Analogue Pulse ShaPer. A part of FE-readout chip.
ATLAS	A Toroidal LHC Apparatus, one of the proposed general purpose pp detectors for the Large Hadron Collider.
barn	It is a standard unit for nuclear reactions and it is expresed as 1 barn = $10^{-28}\ m^2$.
CAD STAR	A soft ware for making printed circuit board layout.
DAQ	Data Acquisition system, a system for reading out and storing data from a detector.
DIP	Dual In-line Package. A type of integrated-circuit package. Those which we have used are ceramic (CERDIP). Circuit leads or pins extend symmetrically downward from opposite sides of the rectangular package body.
ECL	Emitter-Coupled Logic circuit. ECL circuits use bipolar transistors biased in the active region. They are a very fast high-power digital technology commonly used in logic circuits.
EPF	Elementary Paricle Physics at the Oslo University.
Fan-in	The number of electrical loads presented by an input pin to the driving device, applies to macros within an array or to discrete devices.
FElix	A front-end circuit made according to RD20 specifications.
Fan-out	The number of components to which a signal is connected.
GEANT	A CERN library program for detector simulation.
$\mathcal{L}$	Luminosity refers to the collision rate between particles in colliding beam (a product of beam intensity).
LHC	Large Hadron Collider.
Minimum bias event	A soft inelastic proton-proton collision. In the most common type of

event in high energy p-p collisions. At LHC design luminosity, around 20 of these events will occur every bunch crossing (BCO).

MIP Minimum Ionizing Particle. In a detector element, the signal produced by a highly relativistic particles that passes straight through the sensor. Corresponds to lower value of dE/dx in the Beth-Bloch formulae.

Occupancy The number of hits pr detector element pr BCO.

Open-drain Are outputs which at any given time are either actively sinking current or are high impedance. It refers to the drain terminal of a MOS FET.

PCB It is a board made at the Oslo University to be used for the test of FElix chip. Its dimensions are 140mm$\times$280mm.

Pedestal In a detector element, a value measured when no signal is present. Must be subtracted from the raw reading to get the true signal.

Pileup Extra hits or energy deposited in the detector due to minimum bias events. This causes an irreducible 'noise' in the detector on top of any interesting event.

Pipeline An on-detector memory buffer for storing the information from each bunch crossing during the decision time of the L1 trigger.

RDn Collaborations set up to investigate and develop new detector technologies for the LHC.

Region of Interest
A region of the detector in (η,ϕ) space flagged by the level 1 trigger as containing a potentially interesting object, for further examination at level 2.

spatial resolution
The accuracy to locate a hit within the detector frame.

SIROCCO SI-strip Read Out Camac COntroller.

Stero angle Two detectors laying in such away that their strips cross each other.

TRD Transition Radiation Detector, a tracking detector consisting of an array of straw drift tubes interspread with dielectric material to generate transition radiation. It is also called TRT to emphasise the tracking function.

(X_0) Radiation length, a measure of a material's density as seen by electromagnetic interactions. The particle energy loss is about a fraction 1/e of its energy due to bremsstrahlung on average in 1 X_0.

Wafer The silicon slice (various diameter circles) upon which multiple layers of doped materials have been placed to form a number of usable component chips known as dice.

Appendix A

Radiation effects

The silicon detector must be designed to withstand the effects of hard radiator. One of the more important requirements of operating silicon detectors in LHC conditions is that, especially after several years of operation, the detectors must be kept cool (0° or below). In this appendix a brief description of the radiation effects will be given. This will cover both detectors and read out electronic on board. The physics of radiation interactions with solids, radiation effects on semiconductor devices will be discussed. Semiconductor devices are sensitive to many types of radiations. This require special design and fabrication. Parts so designed are called radiation-hardened, or rad-hard. Also many design strategies can reduce a part's susceptibility to radiation damage.

A.1 The Physics of Radiation Interactions with Solids

Radiation interactions with solids are classified into three groups:

- photons
- charged particle
- neutral interactions

Photons (X-rays and gamma rays) interact with atoms through the photo-electric effect, Compton scattering, and pair production, and in each case they generate energetic free electrons that cause secondary charged particle interactions. Those charged particles, interact through Rutherford (Coulombic) interaction or, if heavy enough, nuclear interactions. Neutrons, which interact through nuclear interactions are another problem. The charged particle interact through scattering or excitation of atomic electrons. While nuclear interactions displace atoms in crystal lattices or transmute atoms from one element to another. These two mechanisms change the state of a solid. Two effects of these mechanisms concern the solid state electronics:

- Ionization and atomic displacement.

Ionization occurs when an atom loses an excited valence electron to the conduction band. A charged particle ionizes a valence electron by liberating that electron and creating lattice vibrations that may ionize further atoms. The electron absence created by this process is called a hole. If an electric field is present, some electrons and holes immediately recombine with other atoms or become "trapped" in lattice defect sites. This phenomenon is called "initial recombination." While ionization produces electron absences, atomic displacement produces lattice defects. Atomic displacement occurs when heavy particles interact with atomic nuclei, removing them from their lattice sites to new sites. This upsets the periodicity of the lattice, thus creating lattice defects[23].

A.2 Radiation Effects on Semiconductor Devices

Radiation effects on semiconductor devices are classified into two major types: total ionizing dose **TID** and single-event effects **SEE**. TID is the accumulated effect of ionizing radiation over the lifetime of an experiment and SEEs are transient or permanent effects due to single particles.

- Total Ionizing Dose (TID)

Ionizing radiation primarily effects the oxide layer of MOS structures, silicon dioxide (SiO2). The oxide is a crystal lattice vulnerable to the build-up of injected ions. TID is measured in terms of radiation absorbed dose or rad (1 rad = 100 ergs per gram of material).
Ionizing radiation produces electron-hole pairs in SiO2 which allow holes to cause further damage. After initial recombination the gate immediately collects the mobile electrons leaving holes to transport to an interface, both via the electric field across the transistor. Holes travel to the Si-SiO2 interface if the field is positive.
These positively-charged holes can cause a catastrophic negative shift in the threshold voltage of the device. A fraction of holes are trapped at the Si-SiO2 interface. If this voltage shift is great enough in the right direction, a device which is normally "off" threshold can turn "on" (or vice-versa). Also the positive can invert p-type isolation regions, causing leakage currents between adjacent transistors. These traps remain until they are annealed (detrapped) over a period of hours to years via effects such as electron tunneling. TID depends not only upon total trapped charge, but upon the rate of incoming particles as well. The interplay between hole trapping, hole annealing and interface trap buildup causes a complex dependency[23].

- Single event effects (SEE)

Integrated circuits are susceptible to transient upsets (soft errors) and permanent damage (hard errors) when single high-energy particles impinge on a transistor. A single charged particle can traverse through a transistor's reverse-biased p-n junction and create an ionizing path along its line of trajectory. This causes excess charge along that path. The electric field across the junction is distorted along the ionizing path (this is called funneling), which increases the electric field's ability to attract the charge to one of the nodes. Eventually, the nodes collect the leftover charge through diffusion[23].

- Displacement damage

It is a concern for ASICs. High-energy particles can displace atoms in a crystal lattice, creating energy levels in the forbidden band gap. This can reduce the minority carrier lifetimes and thereby reduce gain by introducing new recombination centers.

A.3 Withstanding the Radiation Environment

Due to very high doses during the ATLAS life time we have to use rad. hard electronics. This can be achieved by minimizing the effects of radiation, shields, rad-hard parts, and fault tolerant design methods. Radiation shielding shall be an integral part of design. Low-energy particles are trivial to shield, whereas high-energy particles become much more difficult. The best shields have low atomic number, such as carbon and aluminum. Shielding can significantly reduce TID, but it can rarely affect SEEs since particles energetic enough to cause SEEs typically require shields many centimeters thick to be adequately attenuated. Rad-hard ASICs are made by hardening the fabrication process and the design. Hardening the process deals mainly with hardening the oxide layer, since it is the most sensitive to radiation. Hardening the circuit design requires conservative practices such as widening design margins for stability, gain, and noise. Fan-out, slew rate, propagation delays, and other circuit parameters must account for worst-case radiation effects[23].

Appendix B

The LHC layout

The LHC contain four experiments. The two large general purpose p-p experiments ATLAS and CMS. ALICE a heavy-ion experiment and LHCB is a spesialized experiment for b-physics. In the following will be given some information about different aspects involving the LHC:

- Rings and beams: There are two rings, one ring per beam. Beam 1 refers to the beam circulating clockwise, beam 2 refers to the beam circulating anti-clockwise.
- Right and left: Describes the position in the tunnel (observer is inside looking out), same definition as in LEP.
- Upstream/downstream: Always related to the direction of one of the two beams, if no beam (beam 1 or beam 2) is explicitly stated, beam 1 is taken as the default. This implies that stating a position as being 'upstream' without indicating any beam, is equivalent to stating that the position is to the left and vice versa.
- Arc: The part of the ring occupied by regular half-cells with three dipoles and one quadrupole; does not contain the dispersion suppressor (DS).
- Insertions (IR): An insertion is the part of a ring between two arcs. It consists of one dispersion suppressor, one full straight section, and a second dispersion suppressor.
- Straight sections: The term 'straight section' is reserved for the long quasi-straight sections between the upstream and downstream dispersion suppressors, including the separation/recombination magnets.
- Insertion Point (IP): Middle of the insertion, which is also an Interaction Point in those straight sections where the beams cross. The IPs are numbered IP1, IP2,..,IP8.
- Sector: The part of a ring between two successive insertion points is called a sector. Sector 1-2 is situated between IP1 and IP2.

- Octant: An octant starts in the center of an arc and goes to the center of the next downstream arc. An octant is constituted of an upstream and a downstream half-octant. A half-octant and a half-sector cover the same part of the collider even though they may not have the same number.

The general numbering of the elements in the LHC is closely linked to the cell numbering scheme and the numbering of the quadrupoles within the cells. There are up to 33 quadrupoles per half-sector, numbered from 1 to 33 starting from an experimental IP to the mid-arc position as shown in fig B.2 For a non-crossing insertion, the quadrupoles are numbered from 2 or 3 to 33.
The separation or recombination dipoles are numbered D_1 to D_4 starting from the IP; D_1, D_2 are close to the IP and D_3 , D_4 are close to the DS[3].

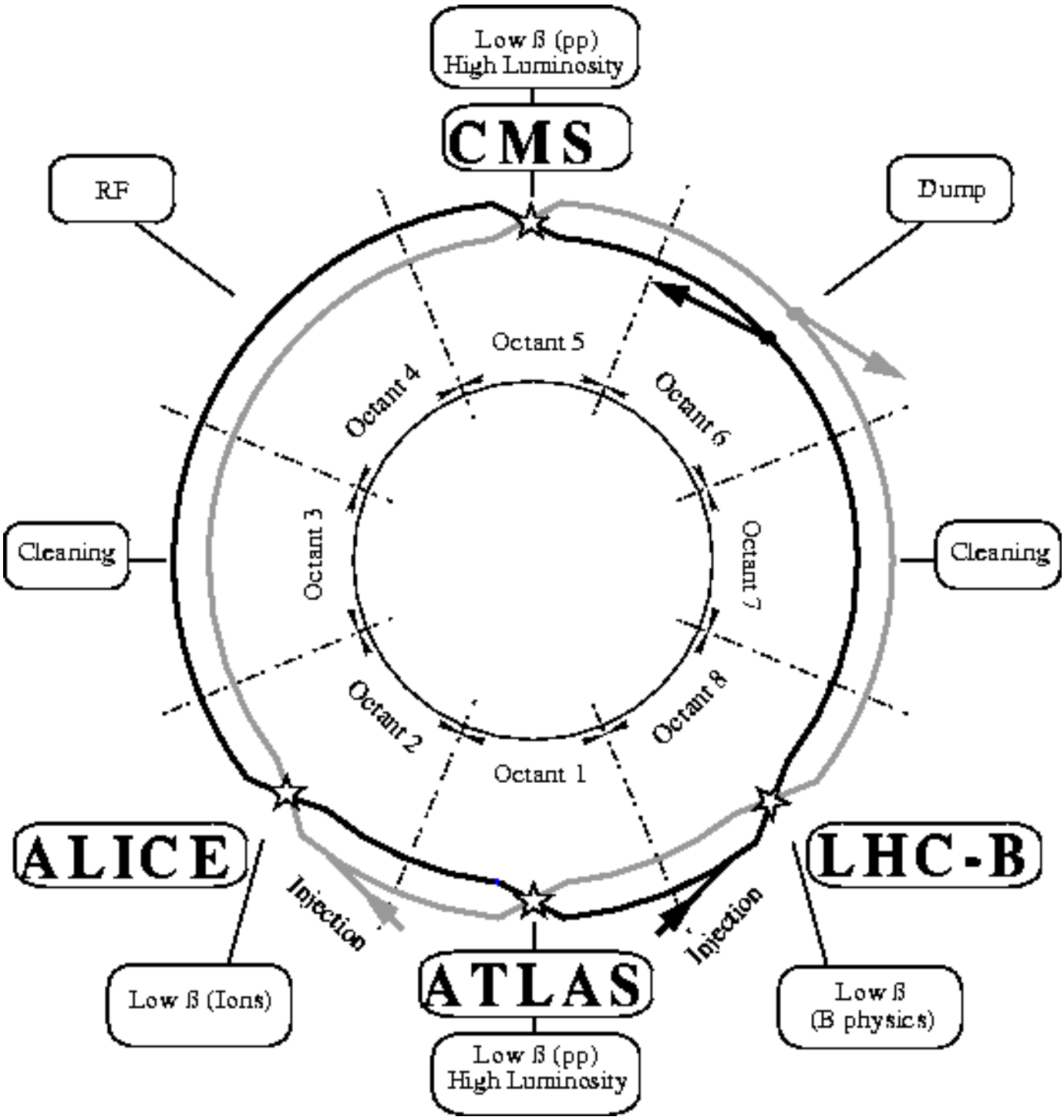


Figure B.1: The location of LHC's different experiments.

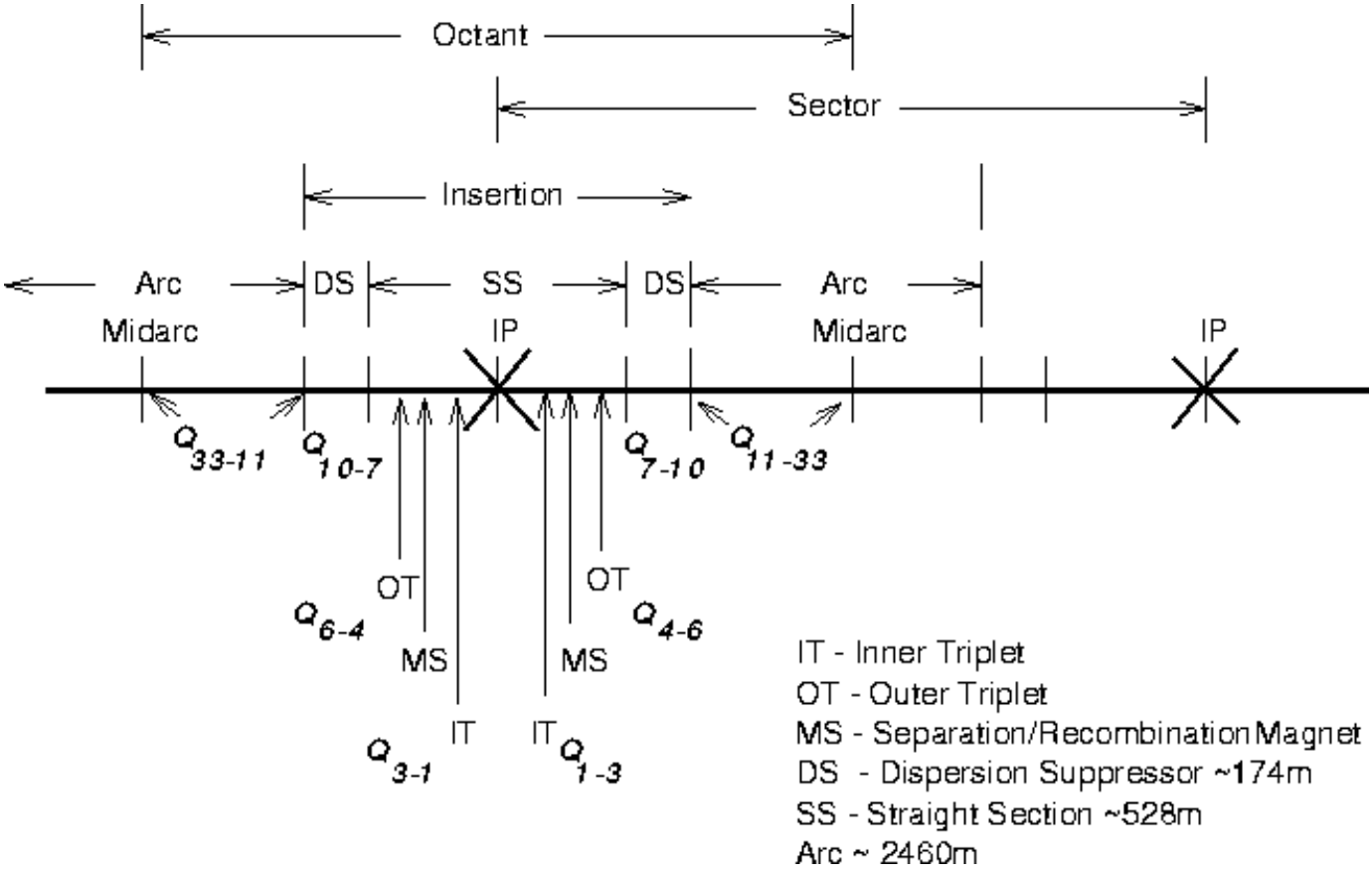


Figure B.2: The LHC definitions and conventions for quadrupole numbering

Appendix C

AMUX-128 channel

The Analog MUltipleXer 128-channel is designed by Jan Kaplon at CERN. This chip has 128 channels and in addition one dummy channel. The logic levels for digital signals used on the chip are ECL levels. It means that logic level 0 (low) is -1.8V and logic level 1 (high) is -.8V. The AMUX digital, analog signals and the its biasing is given in the following table.

The ECL control logic signals arrive at the PCB through CN_{26} and they leave the PCB toward the hybrid through connector CON_5 on the top of the PCB.

The AMUX clock can run at 20 MHz. The time required to read out each channel of FElix 128 channel with this clock frequency becomes $\frac{128}{20MHz}$= 6.4 μs. This read out time is greater than the maximum time between outputs from the FElix which is 4 μs[1]. In order to solve this problem the AMUX clock must be run at 40 MHz. In fact the next version of the FElix has been integrated with a AMUX which runs at the BCO frequency.

[1]The FElix continuous read out frequency is 250 KHz.

Pad /signal name	**Nominal Value**	**Description**
AVDD	+2V	Analog power.
AVSS	-2V	Analog power.
DVDD	+2V	Digital power.
DVSS	-2V	Digital power.
DGND	0V	Digital ground.
SFBI	50 μA	Sample and hold biasing.
MRESET	Active $H_{\mathbf{a)\&b)}}$	Shift register Reset.
MRESETB		$ECL_{\mathbf{b)}}$.
CKL		The shift register clock.
CKLB		$ECL_{\mathbf{b)}}$.
SAMPLE	$H_{\mathbf{a)}}$	Selects sample or hold. Active (sample) high.
SAMPLEB		$ECL_{\mathbf{b)}}$.
RBIT	Active $H_{\mathbf{a)}}$	Input to shift register.
RBITB		Out from shift register active $H_{\mathbf{a)}}$ $ECL_{\mathbf{b)}}$.
RBOUT		$ECL_{\mathbf{b)}}$
RBOUTB		$ECL_{\mathbf{d)}}$
MOUT		The analog output from the $MUX_{\mathbf{d)}}$.
OLEV		The reference part of AMUX.
TCLK		Test clock.
TCLKB		Inverted TCLK.
TSH		Test sample and hold.
TSHB		Inverted of TSH.
TRESET		Reset in test mode.
TRESETB		Inverted of TRESET.
ATST		Analog test input.

Table C.1: Signals available on AMUX. a) Desinations H and L refer to logic high and low. b) Differential ECL signal, these signals require their inverts applied on the board. c) The line is pulled by 470 Ω to DVSS. d) The line is pulled by 10 kΩ to AVSS.

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