Electromagnetic noise studies in a silicon strip detector, used as part of a luminosity monitor at LEP.

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Abstract

As part of the luminosity monitor, SAT, in the DELPHI [1] experiment at CERN's Large Electron Positron collider, a tracking detector constructed from silicon strip detector elements was installed in front of an electromagnetic calorimeter. The luminosity was measured by counting the number of Bhabha events at the interaction point of the electron and the positron beams. The tracking detector reconstructs tracks from the interaction point and the calorimeter measures the corresponding particles' energies.

The SAT Tracker [2] consists of 504 silicon strip detectors. The strips are DC–coupled to CMOS VLSI–chips, baptized Balder [3,4]. The chip performs amplification, zero–suppression, digitalisation, and multiplexing.

The requirements of good space resolution and high efficiency put strong requirements on noise control. A short description of the geometry and the relevant circuit layout is given. We describe the efforts made to minimise the electromagnetic noise in the detector and present some numbers of the noise level using various techniques.

Introduction

The SAT Tracker (SATT) detector consists of two planes with altogether 504 silicon strip detectors with a thickness of 300μm. The strips are arranged in circles centered on the beam. The pitch is 1mm. The geometrical acceptance is defined to about 50μm by the boarder of 100μm between the strips. The large pitch of 1mm justified digital observations only. The Balder chip therefore digitizes the signals before sending them to the data aquisition system. In this way it was hoped that the noise would be reduced. The SATT detector contains 23 112 active electronic channels.

Balder is a 48–channel device, where the first elements in each channel are a charge sensitive pre–amplifier and a shaper. After the shaper is a comparator performing zero–suppression, followed by a digital circuitry multiplexing the channel addresses from channels with signal levels above the comparator reference voltage. Balder was produced in a MIETEC 3μm n–well double poly/single metal CMOS process. The SATT was mounted in DELPHI first time in

Figure 1: The basic detector board without components.

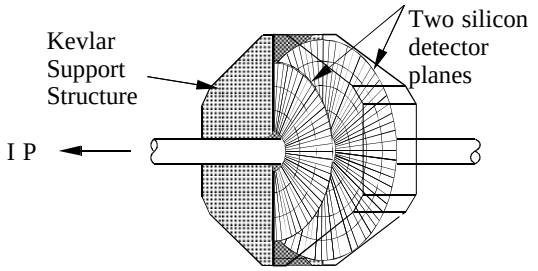

Figure 2: The SAT Tracker.

July 1990. To the authors knowledge, this was the first silicon strip based detector that performed zero–suppresion and multiplexing of digital channel addresses on the detector board.

Moving from a mainly analog domain towards a more digital domain, often require a change in the grounding and shielding configurations previously used.

The detectors and the VLSI–chips are mounted on substrates/printed circuit boards made of 0.709mm thick Kevlar [2,5]. A drawing of a Printed Circuit Board (PCB) without any components mounted, is shown in figure 1 (81% of natural size). The grid filled trapeziums are the detector sites, and their companion Balder chips are mounted on the black rectangles next to these areas. The detectors closest to the edge connector correspond to the largest radius. Radially the SATT is diveded into 3 detector rings for the smaller area plane closest to the interaction point and 4 detector rings for the larger plane.

The PCB's are supported in a barrel also made from Kevlar. Figure 2 shows the geometry of the SAT Tracker. The whole detector is mounted on the front of the electromagnetic calorimeter. The two detecting planes differ mainly in the outer radius. Figure 1 shows a board from the smallest plane. The difference between the small and the large PCB's is that the large board has a fourth ring at a larger radius, and the area of the board is correspondingly larger. The detectors in the three inner rings each have 47 channels, giving a total of 141 detector channels on the small boards. The detectors in the fourth ring have 39 channels. The large boards have a total of 180 channels. Each plane is buildt up with 72 boards of the appropriate size.

In order to minimize the radiation length the substrate was produced without a ground plane. Both detectors and readout chips were glued by conducting glue directly onto the Kevlar substrate, and connected by wire–bonding to the circuits in the substrate. In order to cover the whole plane with continuous circles of strips, two boards with the detectors shifted azimuthally 5 degrees w.r.t. each other were glued front–to–front with a 3.0mm thick Kevlar separator, making up a doublet. Next, two and two doublets were glued together, with a 5.0 degree overlap, making up a quartet. These quartets were the smallest replaceable detector units in the SATT.

The next levels of readout circuitry were mounted as two short pipes covering the outer radius of the detecting planes. With respect to signal (i.e. address of channels with data) readout, the inner of these pipes, containing the Tracker Fan Reference and Interconnect (TFRI) [6] boards, is only a routing layer. Three quartets are connected to one of these boards, which in turn are connected to the outer pipe, containing the Clock Generating and Encoding Circuitry (CGEC) boards [6], with three 40–wire flat cables. The boards in the outer pipe performed data multiplexing, before the data were sent off–detector to fastbus modules [7] in the control–room via 30m long twisted–pair cables.

In addition to being a routing level for data, the TFRI boards also did the necessary slow–control. This included generating analog references for the detector boards, and monitoring the value of these references. The fully digital communication used in the slow–control was done by two independent I^2C buses [8], one bus for each plane.

For simplicity, the TFRI and the CGEC boards are not included in figure 2. A more detailed description of the SATT can be found in [6].

The front–end circuitry

The charge liberated by a Minimum Ionizing Particle (MIP) in a 300μm thick silicon detector is at the maximum of the Landau distribution about 24 000 electron/hole pairs. This corresponds to an approximately 4fC signal. Figure 3 shows a sketch of the analog electronics in one channel. The preamplifier and shaper were specified to have a total gain of

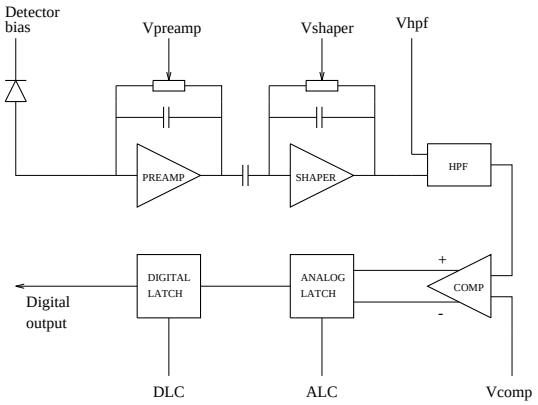

Figure 3: One measurement channel.

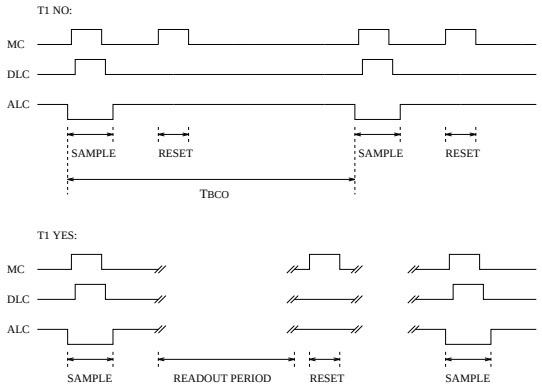

Figure 4: Timing of sample and reset signals.

2μV/electron. Neglecting signal reduction, one MIP will most probably give a 48mV signal at the output from the shaper.

The high–pass filter (HPF) following the shaper, is used to establish a stable DC–level at the signal input to the comparator. The cut–off frequency was set to 50kHz, well below the SHAPER CR–RC filter center frequency of 2MHz, corresponding to a peaking time of 500ns. Activating the digital ALC signal will close the two transmission gate inputs to the differential amplifier inside the analog latch, the output then saturates at either a logical high or low level. Next, the signal is captured in the digital latch by applying a pulse on the DLC signal, this pulse being completely encompassed by the ALC pulse.

The most important timing aspects are shown in figure 4. The upper half shows the case for a first level trigger (T1) no decision, the lower half the case for a T1 yes decision. ALC and MC are externally applied signals, DLC is internally derived from each second MC–pulse. With respect to noise problems described later, one should notice that MC has to run at twice the Beam Cross Over (BCO) frequency.

The chip uses three power–supplies:

vdd :	+5v
gnd :	0v
vss :	-5v

The analog circuitry runs between vdd and vss, and the digital circuitry uses gnd and vss. The back substrate is connected to vss.

PCB layout

Degraded performance on the printed circuit board is due to electrical parameters as resistance, capacitance and inductance. These cause signal delays and signal distortions, including unwanted appearance of signals on supposedly quiescent lines. In the application described here, it is these noise signals that will be the main concern.

Three common noise coupling mechanisms resulting from the non–ideal conductor characteristics are:

1. Coupling through time–varying magnetic fields.
2. Coupling through time–varying electric fields.
3. Coupling through common line impedance.

All circuit elements including conductors radiate electric and magnetic fields whenever charge is moved. When the circuit dimensions are small compared to the wavelength of the signals in the circuit, the noise coupling due to these fields can be represented as equivalent lumped circuit elements. On the detector board, the ALC and MC control signals are the fastest switching signals with 3ns rise (t_r) and fall times. Defining the bandwidth of a logic pulse to be at the break point where the Fourier coefficients change from -20dB/decade to -40dB/decade [9], this corresponds to a digital bandwidth:

$$\mathrm{Bw} = 1/(\pi \times t_r) \approx 106\mathrm{MHz}$$

or to a wavelength of 2.8m. For the electronics being considered, the dimensions are considerably smaller than this, and the lumped circuit element approach is valid.

When current I flows in a conductor, it produces a magnetic flux, ϕ, proportional to the current, with the inductance L being the constant of proportionality:

$$\phi = \mathrm{LI}$$

When current flowing in one circuit produces a flux, ϕ_{12}, in a second circuit, there is a mutual inductance M_{12} between circuit 1 and 2, defined as:

$$\mathrm{M}_{12} = \frac{\phi_{12}}{\mathrm{I}_1}$$

The mutual inductance relates the noise voltage induced by magnetic flux coupling between the circuits. The relation is simply:

$$\mathrm{V}_\mathrm{N} = -\mathrm{M}_{12}\frac{\mathrm{dI}_1}{\mathrm{dt}}$$

The mutual inductance is given by the geometry and the magnetic properties of the medium between the two circuits. It can be reduced by physical separation of the circuits, or by twisting the source wires in order to cancel the magnetic fields from the wires. Reducing the area of the receiver circuit will also reduce the mutual inductance. If the return current goes through a ground plane, an area reduction will be achieved by placing the conductor closer to this ground plane. If the return current is through one of a pair of conductors, the area will be reduced by twisting these conductors. Since twisted pair cables can not be processed onto a single–layer pcb, this method of shielding against magnetic radiation could not be used in the actual application.

The time–varying electric field between two conductors are represented by a capacitor connected between the two conductors. This capacitor will make up a high–pass filter together with the impedance between the noise–receiving conductor and vss. Due to the high bandwith, the control signals can be approximated with square waves. With this as input, the high–pass filter gives the well known step function with an exponential decay governed by the RC product as output.

Half of the signal lines from detector number two, figure 1, are not shielded with powerlines against the fast switching control signals. With respect to the timing diagram in figure 4, three pulses could generate potential noise problems, the ALC–sample, MC–sample, and the MC–reset pulses. However, the falling edge of the ALC–pulse will immediately block the input to the analog latch, thereby preventing possible noise coupled from the sample pulses to the signallines from corrupting the signals already in this latch. The most critical part is the interval from the MC–reset pulse to the next sample phase. If potential noise signals coupled from the reset pulse onto the signallines do not decay before the next sample phase, this could create a noise problem. The reset pulse might generate noise signals in two phases, first the pulse itself can couple to the signallines, next potential ringing on the MC–line due to imperfect termination can also couple to these lines. The interline capacitance between MC and the nearest input signal line was measured to be as much as 8.8pF. This means that a 5V step on the MC line will induce a charge of 44pC in this line. The linear range is specified to be from -48fC to +96fC. The feedback resistors and the bias circuitry are implemented with non–linear devices (transistors). Hence the channel has no simple equivalent model containing only linear devices. Without access to simulation models for the transistors, this makes it hard to do a quantitative analysis of the response to a 44pC input signal. However, some qualitative remarks can be made. The interval from the MC–reset pulse to the next sample phase is approximately 12μs. Compared to the internal timeconstants, 500ns peaking time for the shaper, it seems unlikely that MC–reset would generate significant noise during the next sample phase. Nevertheless, the CR–RC filter has a long tail compared to its peaking time. In addition, the decay time might well be prolonged due to the preamplifier and shaper being driven into the non–linear region by a large noise signal. This means that the MC–reset pulse can not be ruled out as a potential noise source. The high coupling capacitance also means that even the slightest ringing on the MC–line could become a serious noise source. For example, a 1mV pulse will inject 8.8fC into the nearest signalline. Even though lack of data, with respect to resistor, capacitor, and transistor sizes/models, has prevented a detailed analysis, comparing the 44pC injected by a 5V step and the 8.8fC injected by 1mV potential ringing to the 4fC expected from a MIP signal, gives a clear indication of possible cross coupling noise problems.

When two or more circuits share common power and/or ground lines, common conductor impedance gives rise to the switching noise (ΔI) problem. Switching circuitry inside one circuit will give a current pulse on the power and/or ground lines. This current pulse will give a voltage change across the inductance of the line, affecting also other circuitry being fed by the same powerline. The remedy for this problem be either reducing the selfinductance of the powerline, and/or incorporating decoupling capacitors as close to the power electrodes of the circuits as possible. This will shunt some of the switching current, effectively reducing ΔI through the powerline inductance and the noise generated by it.

Several surface mounted capacitors are incorporated on the detector boards. Unfortunately, due to practical limitations their placement are not ideal. This may introduce spikes and fluctuations in the powerlines and thereby fluctuations in the analog reference voltages. Fluctuations in the comparator reference voltage will clearly give rise to problems concerning signal to noise ratio, and it will also make it more difficult to predict the overall efficiency. There are also other reference voltages internal and external to the Balder chips that can be influenced by powerline fluctuations. To decrease the powerline return impedance by introducing a ground plane will help reducing the problems with switching noise, but one should have in mind that introducing extra mass will increase the radiation length. Other limitations is the choise of electrolytic gold plating on the Kevlar PCB. This reduces the layout freedom.

As stated in the introduction, the small PCB boards have 141 detector channels. The discrepancy between 141 detector channels and $3 \times 48 = 144$ Balder channels, means that each Balder chip had one input channel left unconnected. The large board had the same configuration for the three inner rings, while Balder chips in the fourth ring had 9 unconnected channels.

In connection with the modifications described later, the unconnected channels in the three inner rings were grounded. Also the corresponding channel in ring four was grounded, while the remaining 8 channels per board had to be left unconnected for practical reasons. With the values used for V_{comp} (see figure 3), no noise was observed in the grounded or unconnected channels, neither before nor after the grounding. Noise figures given in the following sections will therefore be with respect only to the Balder channels actually connected to detector strips.

The full detector contains 24 192 Balder readout channels. Subtracting the non–detector channels gives a total number of $(141 + 180) \times 72 = 23\,112$ active channels.

Common settings

The Balder chip has a gain of 2μV/electron with a shaping time of approximately 700ns. Gain and shape are controlled by V_{preamp} and V_{shaper}, as shown in figure 3, and one current, I_{bias}, that is used to generate the remaining bias voltages for preamplifiers, shapers, and comparators. Initial testing of the chip showed that the optimal signal shape was achieved with a shaping time of approximately 500ns. This requires that $V_{preamp} = V_{shaper} = -300$mV and $I_{bias} = -100\mu$A. These settings give a total gain somewhat below the specified gain of 2μV/electron. Taking into account also the signal reduction due to charge sharing between detector strips and losses due to capacitive couplings, the minimum input signal at the comparator is considerably below the ideally 48mV. A ^{106}Ru source was used to obtain a starting value for V_{comp}. To effectively capture the signals, the maximum comparator threshold voltage was found to be approximately 20mV. This was later confirmed to be an appropriate value [10] (The threshold voltage used in [10] should be diveded by 16 to obtain V_{comp} as used herein).

Noise – single detector boards

All the measurements described in this section refer to bench–tests of individual detector boards. No signal was applied to the detectors. Hence all registered hits are counted as noise. The low frequency level one trigger ($f_{T1} < 1$Hz), was generated at regular intervals by a piece of software. The noise figures for individual PCB's are averages over 5000 events. The numbers presented are these numbers averaged over all PCB's within a given plane. If nothing else is explicitly stated, the comparator reference voltage was set to 22mV.

The initial PCB configuration as described in the previous sections, will henceforth be referenced as version 1. Testing of this version clearly showed that the noise level was too high at the intended operational speed with a sampling frequency ($1/T_{BCO}$) of $1/21.0\mu$s. The acceptable noise level is determined by the number of ambiguities in the track reconstruction. This was studied in simulations. The noise figures averaged over all the small detector boards are given in table 1. 100% corresponds to all detector channels containing data in all triggered events. Numbers for $T_{BCO} > 60\mu$s have also been included, as these clearly show that the noise is highly dependent upon the sampling frequency.

sampling frequency	noise [%]		
	ver.1	ver.2	ver.3
$T_{BCO} > 60\mu$s	0.0113	0.0416	0.000005
$T_{BCO} = 21\mu$s	1.2009	0.3012	0.0009

Table 1: Noise figures for small detector boards for three different shielding configurations, as described in the text.

As a first step to improve the noise figures, a aluminium foil was glued as a ground plane to the back of all detector boards. The foil was measured to be less than 10μm thick. With the overlap structure within a plane, and two planes in the detector, this meant adding 80μm of Al, corresponding to 0.09% of a radiation length. This was considered to be negligible compared to the contribution from the silicon detectors, the printed circuits, the Kevlar material and the readout ASIC's.

Next, the flat–cables from the detector boards were put into flexible copper screens. These screens were connected to ground at the TFRI end, at the opposite end they were soldered to the Al shields. The PCB's with the modifications described, gave the results listed under version 2 in table 1.

Version 2 reduced the noise level with approximately a factor of four. However, this was considered still not to be acceptable. As mentioned in the section describing PCB layout, detector channel no. 1 in the second ring had a significant capacitive coupling to the MC–line. It also turned out to be the most noisy channel on the detector board. Therefore the bonding between this channel and the PCB board was cut. The floating PCB lead was connected to ground. Since channel no. 1 in ring 2, overlaps with channel no. 47 in ring 1 on the other board in a doublet, this could be done without loosing space resolution. As expected, the noisy channel turned out to be completely quiet, and in addition the noise level went down for all channels in the second ring.

sampling frequency	noise [%]		
	ver.1	ver.2	ver.3
$T_{BCO} = 21\mu$s	1.303	0.014	0.0007

Table 2: Noise figures for large detector boards.

Also the unconnected channels that could be bonded were grounded. The PCB's with these modifications are called version 3. The noise level was now at an acceptable level.

Table 2 shows the corresponding noise figures for the large PCB's. Since the comparator reference voltage was reduced from 22mV to 19mV between the measurements on version 1 and 2, the actual noise reduction is not directly comparable.

Noise – full detector

The figures given in this section correspond to measurements on the full detector after installation in the DELPHI experiment.

sampling frequency	noise [%]		
	ver.1	ver.2	ver.3
$T_{BCO} = 27.0\mu$s	2.847	–	–
$T_{BCO} = 20.5\mu$s	4.729	0.1988	0.0172
$T_{BCO} = 16.8\mu$s	–	0.1668	0.0762

Table 3: Noise figures after installation in the experiment.

Even with the quite encouraging results from bench–tests of individual detector boards, we now expected a higher noise level due to increased switching transients on the power supplies and possible unnoticed ground loops. This turned out to be true. The noise level when operating the full detector is given in table 3. Comparable data only exists for $T_{BCO} = 20.5\mu$s, but a few more entries have been included as these again show the tendency of increased noise with increased sampling frequency.

The three versions are as described for single detector boards. V_{comp} was 22mV, 20mV, and 19mV during the measurements on ver. 1, ver. 2, and ver. 3 respectively. The relative noise reduction is therefore somewhat better than shown in the table.

Discussion

If all detector boards had had one channel firing in each trigged event, this channel would give a noise level of 0.71%, 0.56%, and 0.62% on the small PCB's, the large PCB's, and the full detector respectively. These numbers are higher than the noise measured for version 2. This suggests that the noise reduction achieved with version 3 could have been due to the grounding of channel 1 in ring 2 only, making it meaningless to describe it as a noise reduction. However in [11] it is shown that this is not the case. That paper describes a test where the noisy channel was filtered out by software, giving noise reduction factors of 1.5 and 2.5 for large and small pcb's respectively. In comparison, the hardware filtering (i.e. grounding) described herein, gave noise reduction factors of 20 and 335 for large and small pcb's. This clearly shows that grounding this channel not only removed it from the set of active detector channels, but also reduced the noise level in other channels.

Prior to the grounding of detector channel 1 in the second ring, the most noisy channels on the board were this channel and its nearest neighbours. Now neigbouring detector channels do not map to neighbouring channels on the Balder chip. This means that the cross–talk is on the PCB–board, and not internally in the Balder chip. The most significant noise reduction in other channels due to grounding of channel 1, occured in the second ring itself. This suggests that the noise reduction achieved was mainly due to the grounded signal lead acting as a ground shield between the MC–lead and the remaining signal–leads in the second ring.

Summary/Conclusions

This paper presented significant electromagnetic noise reductions achieved with fairly simple hardware modifications. The noise reduction factors are summarized in table 4, where $T_{BCO} = 21\mu s$ for individual detector boards and $20.5\mu s$ for the fully installed detector.

item measured	noise reduction factor		
	$\frac{\text{ver.1}}{\text{ver.2}}$	$\frac{\text{ver.2}}{\text{ver.3}}$	$\frac{\text{ver.1}}{\text{ver.3}}$
small pcb's	4	335	1334
large pcb's	93	20	1861
full detector	24	12	275

Table 4: Noise reduction factors for the various hardware configurations.

Figure 5 shows the noise versus samplingfrequency for the three versions of the small detector boards. The test configuration used to sample these curves was slightly different from the setup used to sample the data already given in the tables, and the curves are not directly comparable to the data in these tables.

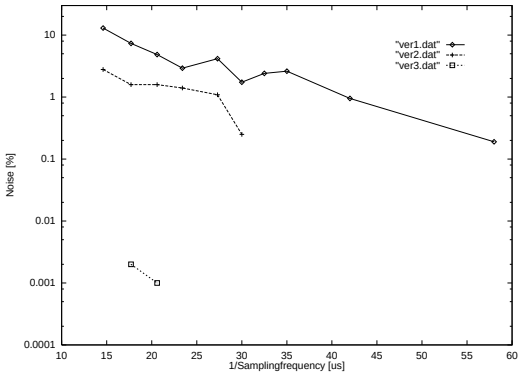

Figure 5: Noise versus samplingfrequency for small detector boards.

The SATT detector was used in DELPHI for five periods between July 1990 and December 1993. In [10] a method to use the SAT Tracker for monitoring the internal geometry of the SAT Calorimeter and thereby improving the luminosity measurements for DELPHI is described. A reduction from 0.35% to 0.05% in the experimental uncertainty due to acceptance cuts is reported. [10] is based on data taken during 1991, this corresponds mainly to version 1 of the SATT. Version 2 was installed in Aug.–91. During 1993 version 3 of the Tracker was used. Preliminary results indicate an experimental precision on the luminosity measurements of 0.2%. 1993 was the final operating year of the SAT detector.

Acknowledgments

The SAT Tracker is the result of many years of development work at the workshops at The Dept. of Physics Univ. of Oslo, where ing. Bjørn Fjeld played a crucial role in the design and construction of the printed circuit boards and the support structure. The Balder chip was designed by Einar Nygård and Alf Olsen at Univ. of Oslo and Centre for Industrial Research[1] in Oslo. Nygård also gave important advices when analysing the noise problems in the detector. The surrounding readout electronics was designed and constructed at the Univ. of Oslo by B. Skaali, J. Wikne, and D. Wormald.

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