UNIVERSITY OF OSLO

Faculty of Mathematics and Natural Sciences

Exam in:	FYS4260 Microsystems and Electronic Packaging & Interconnection Technologies
Exam date:	Monday, June 2nd, 2008
Time for exam:	14:30 – 17:30 (3 hours)
The examination test set consists of:	3 pages including this front page
Attachments:	No attachments
Allowed examination aids:	None except the general allowed aids as for instance approved electronic calculators. For instance, tables and programmed data in calculators not allowed.

The student should check that the test set is complete before you start answering the questions.

Miscellaneous:

Course responsible Per Øhlckers will not be present at University of Oslo on June 2nd, but can be reached on cell phone 95 90 39 89.

The test questions are given in English only, but can be answered in either Norwegian or English. Use maximum 1 page for each question; that is for the sum of both the a) and the b) answers.

Question 1: Technology Trends

a) Discuss the specific challenges for electronic interconnection and packaging technology for automotive electronics, assuming a car lifetime of more than 10 years. Give some recommendations to the automotive manufacturers how they should design and build the electronics to assure that today's new cars after 10 years have well functioning automotive electronics on operation functions as well as safety issues.

b) We have seen and will probably still see dramatic improvements of the performance/price ratio for electronic products. Describe and explain what you consider to be the 3 most important reasons for this development.

Question 2: Green Electronics and Adhesives in Electronics

a) Which environmental challenges are specific to electronics? Describe 2 environmental harmful materials or chemicals that are used or have been used in electronic products and their manufacture. Give examples where these are used or have been used. Explain shortly the concepts "Life cycle perspective" and "Producer responsibility" and explain shortly how these influence design and production of electronic products.

b) Describe the constitution and principle of operation of one kind of anisotropic conductive adhesive, and describe how such an adhesive can be used for electronic interconnections in an electronic system containing a Liquid Crystal Display (LCD) panel, for instance a Global positioning System (GPS) system.

Question 3: Components

a) Describe the principal construction and a common used manufacturing technology for multilayer ceramic capacitors. This is best done by graphics with a supplemental text.

b) Explain different ways to achieve different capacitance values for multilayer ceramic capacitors with the same outer dimensions.

Question 4: Printed Circuit Boards

a) Explain a common used manufacturing technology for double sided printed circuit boards with surface mount devices (SMD) on both sides of the board. This is best done by outlining a flow chart with a supplemental text for each process step.

b) Explain the wave soldering process for a printed circuit board. Describe the two most important solder defects when using wave soldering, and how they best can be minimised.

Question 5: Micromachined Devices/Microsystems MultiProject Wafer (MPW) foundry services

a) Tronics in France is offering microsystems MPW foundry services based upon their Silicon On Insulator High Aspect Ratio Micromachining (SOI HARM) technology. A cross-sectioned view of the process is shown in Figure 5.1 below.

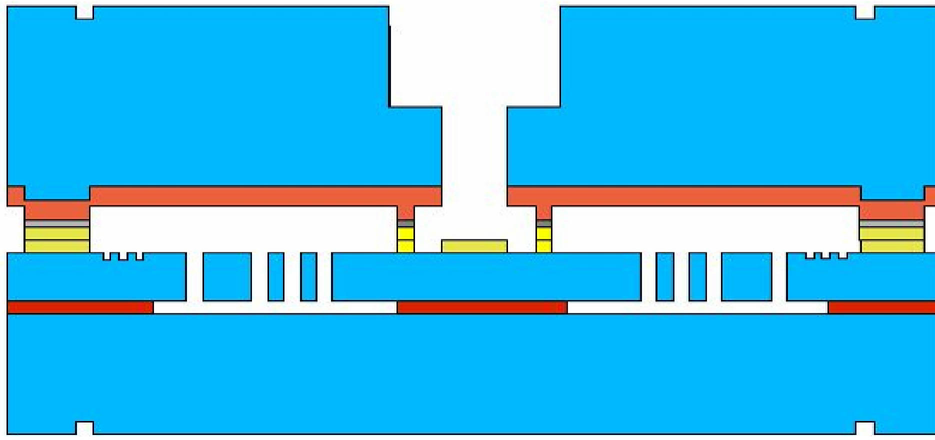

Figure 5.1: Cross section view of the Tronics' SOI HARM MPW process technology

Explain the basic features of the Tronics' SOI HARM process by explaining how a 2-axis accelerometer can be designed and manufactured in this process. This is best done by combining text and graphic presentation.

b) Describe how the Bosch process is included in the Tronics' MPW process to make vertical etch geometries with high aspect ratio. Explain specifically the principles used in the Bosch process to achieve high aspect ratio by minimising underetching. This is best done by combining text and graphic presentation.

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